

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4044B

### MSI

## Quadruple R/S latch with 3-state outputs

Product specification  
File under Integrated Circuits, IC04

January 1995

Quadruple R/S latch with 3-state outputs

HEF4044B  
MSI

The HEF4044B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active LOW set input ( $\bar{S}_0$  to  $\bar{S}_3$ ), an active LOW reset input ( $\bar{R}_0$  to  $\bar{R}_3$ ) and an active HIGH 3-state output ( $O_0$  to  $O_3$ ).

When EO is HIGH, the state of the latch output ( $O_n$ ) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.

The high impedance off-state feature allows common bussing of the outputs.

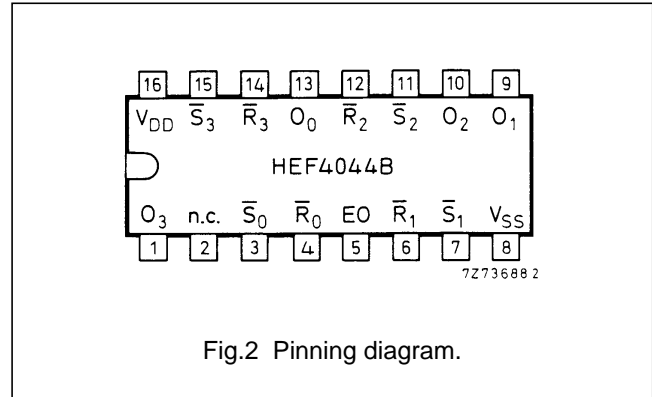


Fig.2 Pinning diagram.

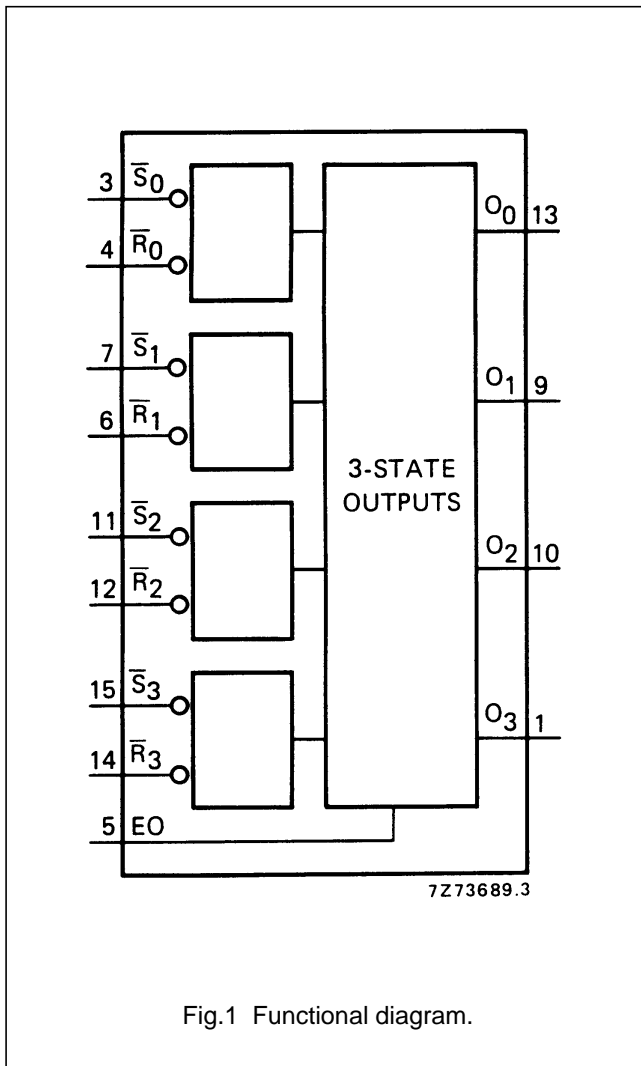


Fig.1 Functional diagram.

- HEF4044BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4044BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4044BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

PINNING

- EO common output enable input
- $\bar{S}_0$  to  $\bar{S}_3$  set inputs (active LOW)
- $\bar{R}_0$  to  $\bar{R}_3$  reset inputs (active LOW)
- $O_0$  to  $O_3$  3-state buffered latch outputs

FUNCTION TABLE

INPUTS			OUTPUT $O_n$
EO	$\bar{S}_n$	$\bar{R}_n$	
L	X	X	Z
H	L	H	H
H	X	L	L
H	H	H	latched

Notes

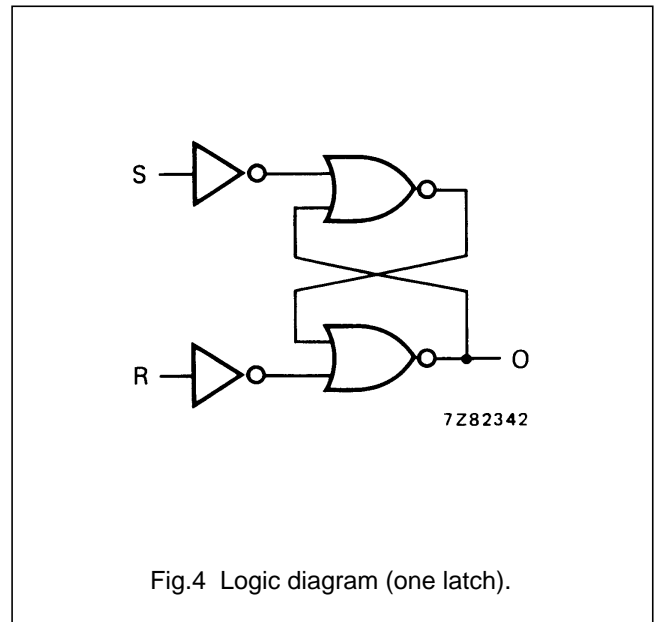
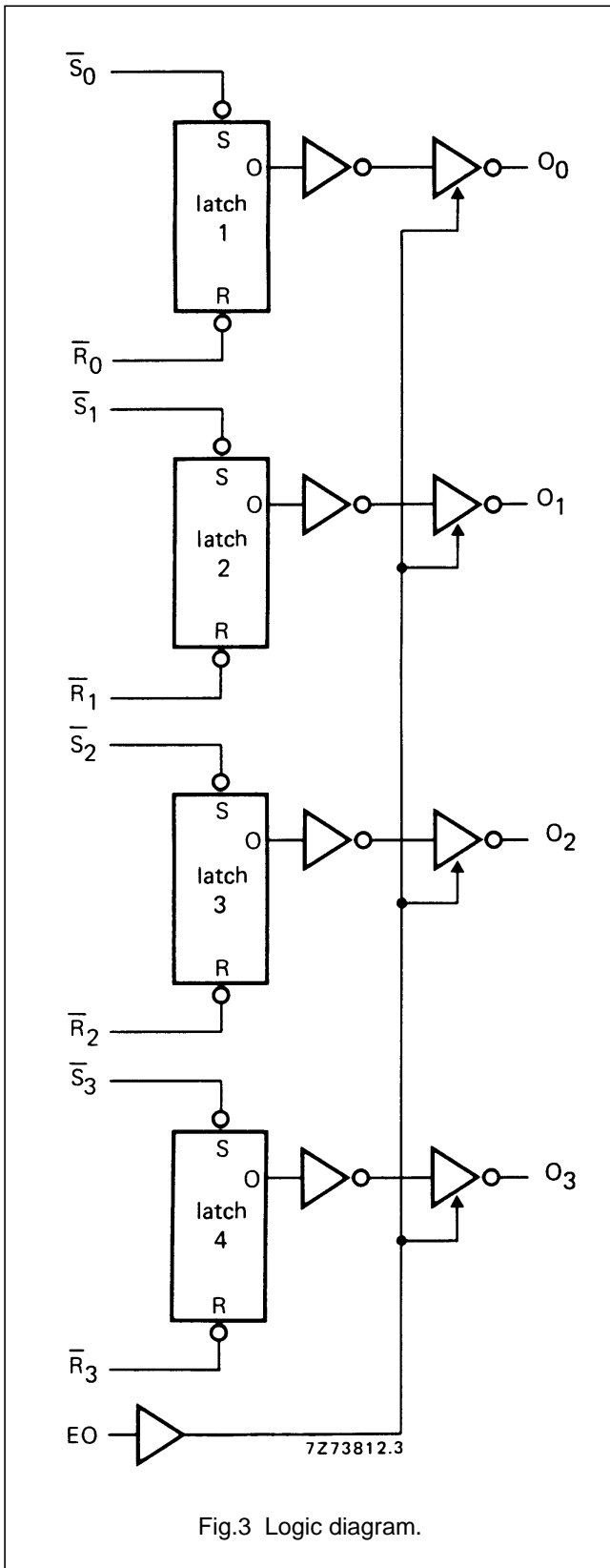
1. H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state immaterial
- Z = high impedance OFF-state

FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

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### AC CHARACTERISTICS

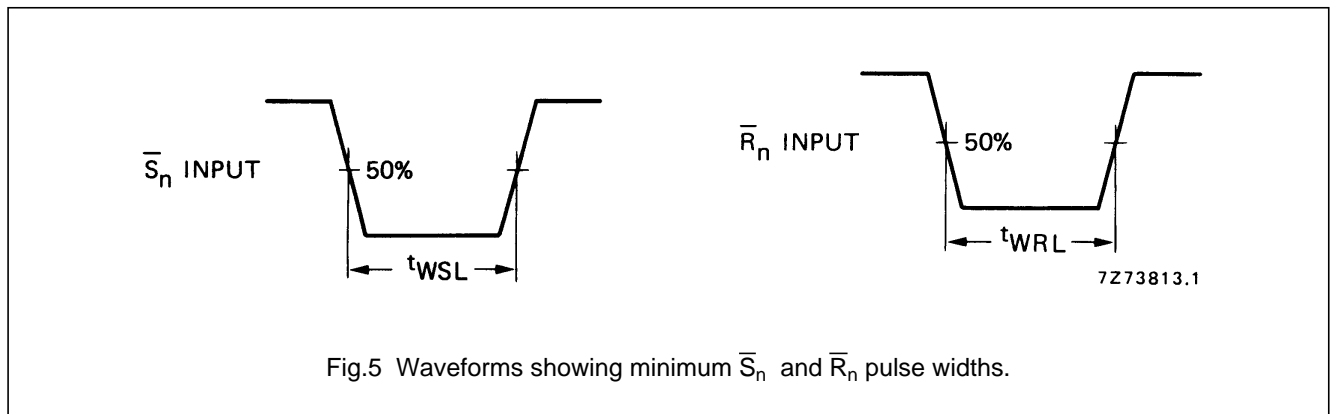
$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $\bar{R}_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	90	185	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	$\bar{S}_n \rightarrow O_n$ LOW to HIGH	5	$t_{PLH}$	90	180	ns	$63\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
3-state propagation delays Output disable times $EO \rightarrow O_n$ HIGH	5	$t_{PHZ}$	50	100	ns		
	10		30	60	ns		
	15		25	50	ns		
	LOW	5	$t_{PLZ}$	30	60		ns
		10		25	45		ns
		15		20	40		ns
Output enable times $EO \rightarrow O_n$ HIGH	5	$t_{PZH}$	50	100	ns		
	10		25	50	ns		
	15		20	40	ns		
	LOW	5	$t_{PZL}$	50	95		ns
		10		25	45		ns
		15		20	35		ns
Minimum $\bar{S}_n$ pulse width; LOW	5	$t_{WSL}$	30	15	ns	see also waveforms Fig.5	
	10		20	10	ns		
	15		16	8	ns		
Minimum $\bar{R}_n$ pulse width; LOW	5	$t_{WRL}$	30	15	ns		
	10		20	10	ns		
	15		16	8	ns		

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	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1300 f <sub>i</sub> + ∑ (f <sub>o</sub> CL) × V <sub>DD</sub> <sup>2</sup> 5200 f <sub>i</sub> + ∑ (f <sub>o</sub> CL) × V <sub>DD</sub> <sup>2</sup> 12 900 f <sub>i</sub> + ∑ (f <sub>o</sub> CL) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = total load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)



**APPLICATION INFORMATION**

An example of application for the HEF4044B is:

- Four-bit storage with output enable