

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4067B

MSI

**16-channel analogue
multiplexer/demultiplexer**

Product specification
File under Integrated Circuits, IC04

January 1995

16-channel analogue multiplexer/demultiplexer

HEF4067B MSI

DESCRIPTION

The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input (\bar{E}), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With \bar{E} LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3 . All unselected switches are in the high impedance OFF-state. With \bar{E} HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3 .

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. V_{DD} to V_{SS} may not exceed 15 V.

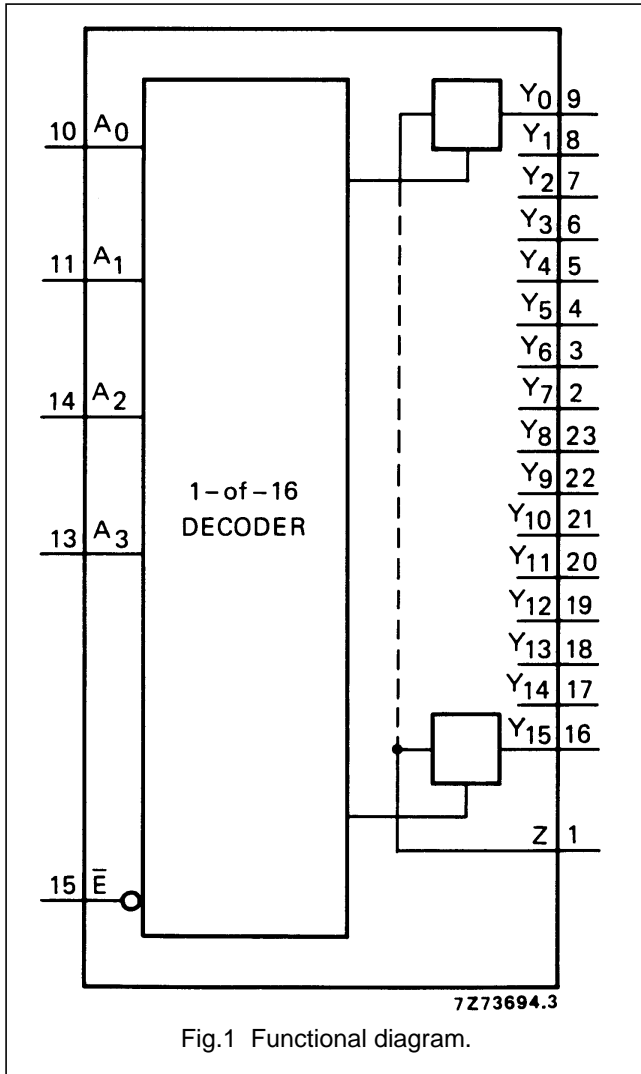


Fig.1 Functional diagram.

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4067BP(N): 24-lead DIL; plastic (SOT101-1)
 - HEF4067BD(F): 24-lead DIL; ceramic (cerdip) (SOT94)
 - HEF4067BT(D): 24-lead SO; plastic (SOT137-1)
- (): Package Designator North America

PINNING

- Y_0 to Y_{15} independent inputs/outputs
- A_0 to A_3 address inputs
- \bar{E} enable input (active LOW)
- Z common input/output

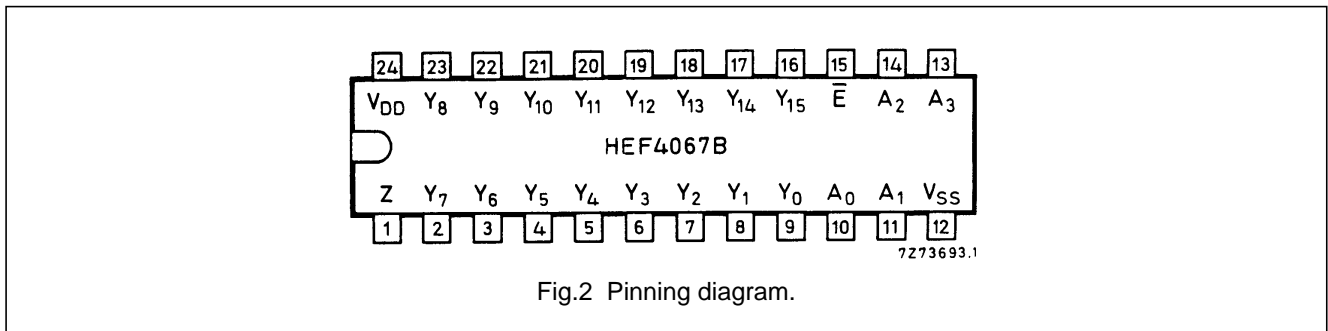


Fig.2 Pinning diagram.

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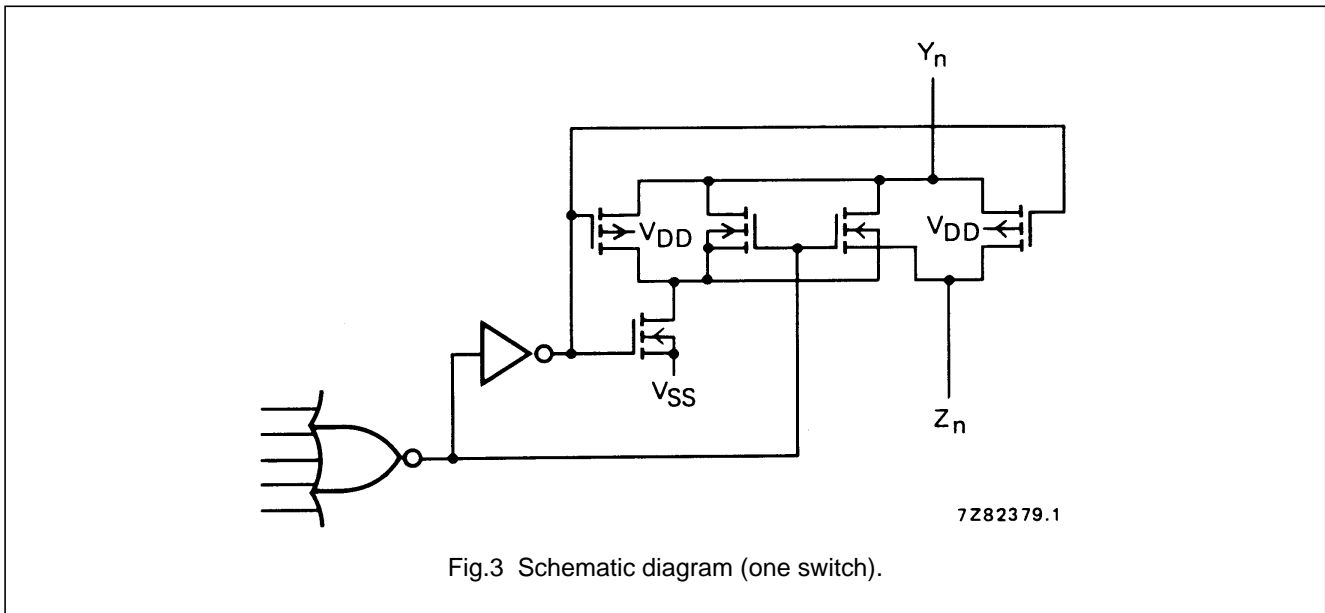


Fig.3 Schematic diagram (one switch).

FUNCTION TABLE

INPUTS					CHANNEL
\bar{E}	A ₃	A ₂	A ₁	A ₀	ON
L	L	L	L	L	Y ₀ - Z
L	L	L	L	H	Y ₁ - Z
L	L	L	H	L	Y ₂ - Z
L	L	L	H	H	Y ₃ - Z
L	L	H	L	L	Y ₄ - Z
L	L	H	L	H	Y ₅ - Z
L	L	H	H	L	Y ₆ - Z
L	L	H	H	H	Y ₇ - Z
L	H	L	L	L	Y ₈ - Z
L	H	L	L	H	Y ₉ - Z
L	H	L	H	L	Y ₁₀ - Z
L	H	L	H	H	Y ₁₁ - Z
L	H	H	L	L	Y ₁₂ - Z
L	H	H	L	H	Y ₁₃ - Z
L	H	H	H	L	Y ₁₄ - Z
L	H	H	H	H	Y ₁₅ - Z
H	X	X	X	X	none

Note

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

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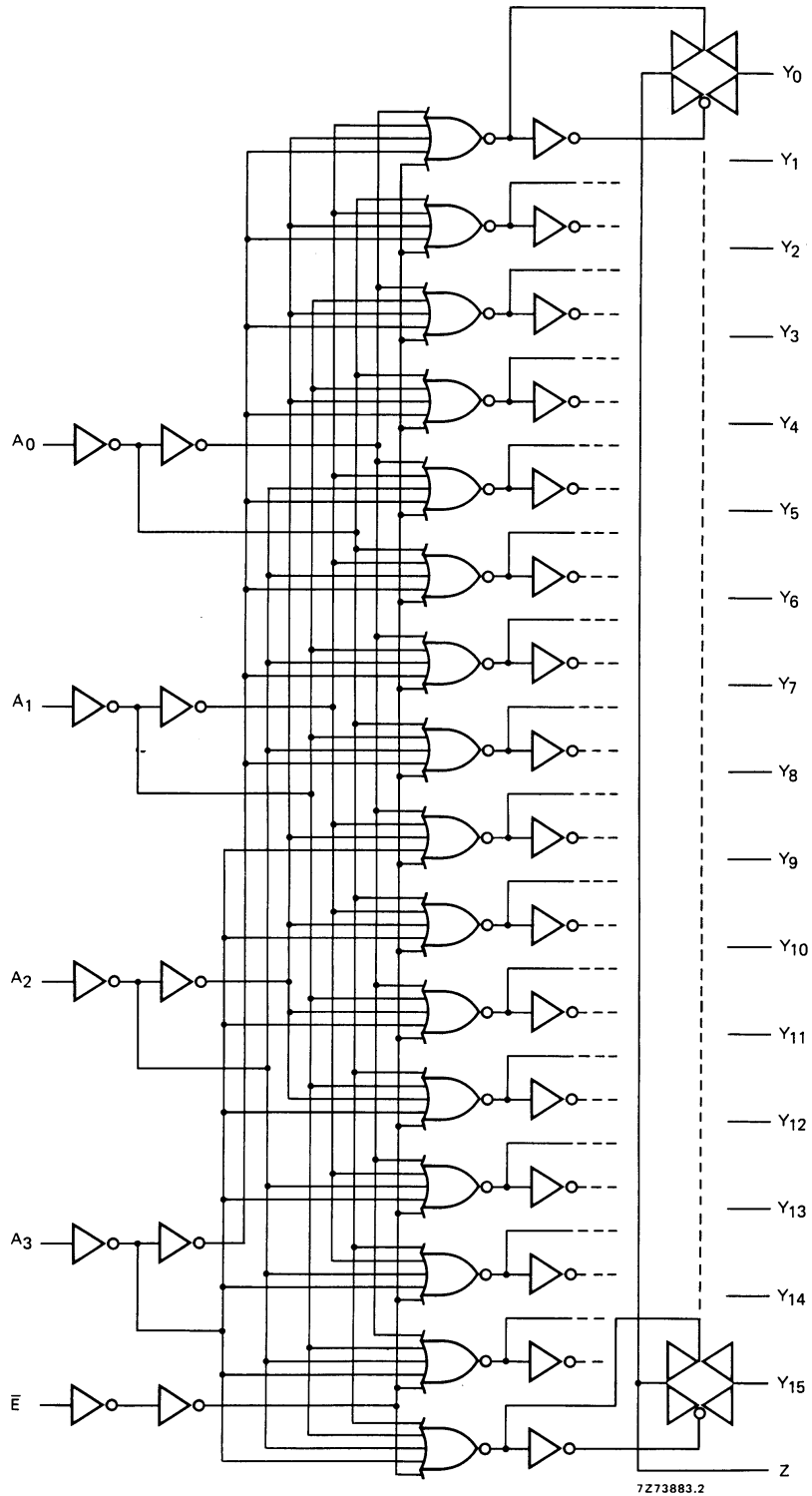


Fig.4 Logic diagram.

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DC CHARACTERISTICS

T_{amb} = 25 °C

	V _{DD} V	SYMBOL	TYP.	MAX.		CONDITIONS
ON resistance	5	R _{ON}	350	2500	Ω	V _{is} = V _{SS} to V _{DD} see Fig.5
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R _{ON}	115	340	Ω	V _{is} = V _{SS} see Fig.5
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R _{ON}	120	365	Ω	V _{is} = V _{DD} see Fig.5
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	25	–	Ω	V _{is} = V _{SS} to V _{DD} see Fig.5
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I _{oZZ}	–	–	nA	E̅ at V _{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I _{oZY}	–	–	nA	E̅ at V _{SS}
	10		–	–	nA	
	15		–	200	nA	

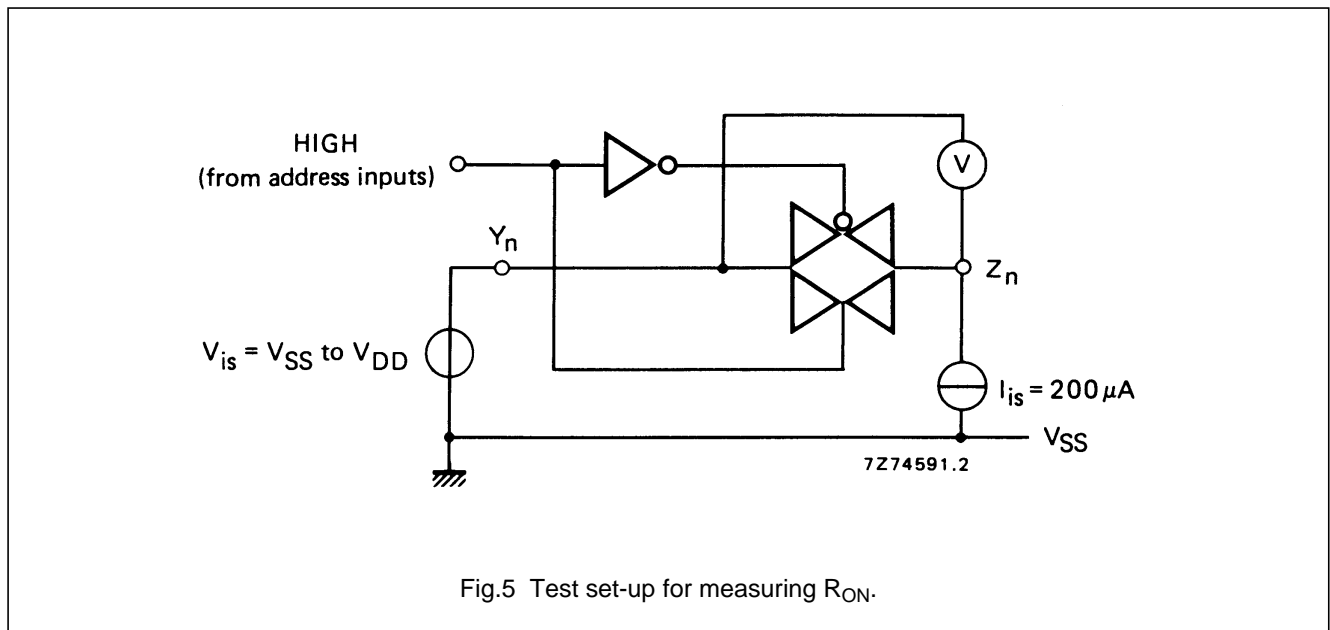
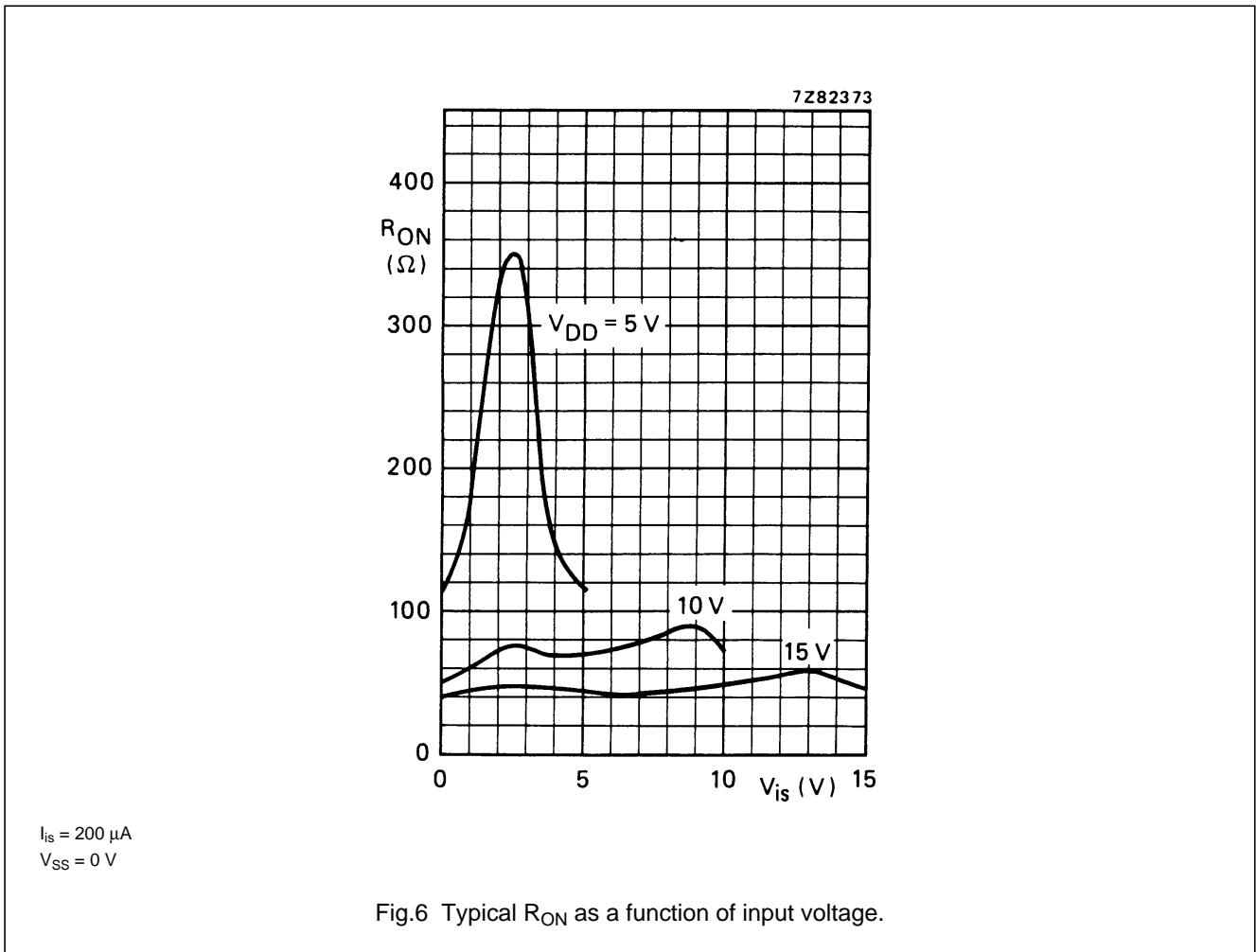


Fig.5 Test set-up for measuring R_{ON}.

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NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 100 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	5 000 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	13 300 f _i + ∑ (f _o C _L) × V _{DD} ²	

AC CHARACTERISTICS (1), (2)

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	TYP.	MAX.			
Propagation delays	5 10 15	t _{PHL}	30 15 10	60 25 20	ns	note 3	
							HIGH to LOW
	LOW to HIGH						
		5 10 15	t _{PHL}	190 70 50	380 145 100	ns	note 4
	HIGH to LOW						
		5 10 15	t _{PLH}	175 70 50	345 140 100	ns	note 4
	5 10 15						
		Output disable times					
			HIGH				
5 10 15	t _{PLZ}			215 180 170	435 355 340	ns	note 5
		LOW					
			5 10 15				
Output enable times							
	HIGH						
		5 10 15	t _{PZL}	170 70 50	340 140 100	ns	note 5
LOW							
	5 10 15						

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AC CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.	
Distortion, sine-wave response	5		0,25	%	note 6
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 8
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 9
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 10
	10		40	MHz	
	15		70	MHz	

Notes

- V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
- V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.
- $R_L = 10$ k Ω to V_{SS} ; $C_L = 50$ pF to V_{SS} ; $\bar{E} = V_{SS}$; $V_{is} = V_{DD}$ (square-wave); see Fig.7.
- $R_L = 10$ k Ω ; $C_L = 50$ pF to V_{SS} ; $\bar{E} = V_{SS}$; $A_n = V_{DD}$ (square-wave); $V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PLH} ; $V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PHL} ; see Fig.7.
- $R_L = 10$ k Ω ; $C_L = 50$ pF to V_{SS} ; $\bar{E} = V_{DD}$ (square-wave);
 $V_{is} = V_{DD}$ and R_L to V_{SS} for t_{PHZ} and t_{PZH} ;
 $V_{is} = V_{SS}$ and R_L to V_{DD} for t_{PLZ} and t_{PZL} ; see Fig.7.
- $R_L = 10$ k Ω ; $C_L = 15$ pF; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
 $f_{is} = 1$ kHz; see Fig.8.
- $R_L = 1$ k Ω ; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig.9.}$$

- $R_L = 10$ k Ω to V_{SS} ; $C_L = 15$ pF to V_{SS} ; \bar{E} or $A_n = V_{DD}$ (square-wave); crosstalk is $|V_{os}|$ (peak value); see Fig.7.

- $R_L = 1$ k Ω ; $C_L = 5$ pF; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

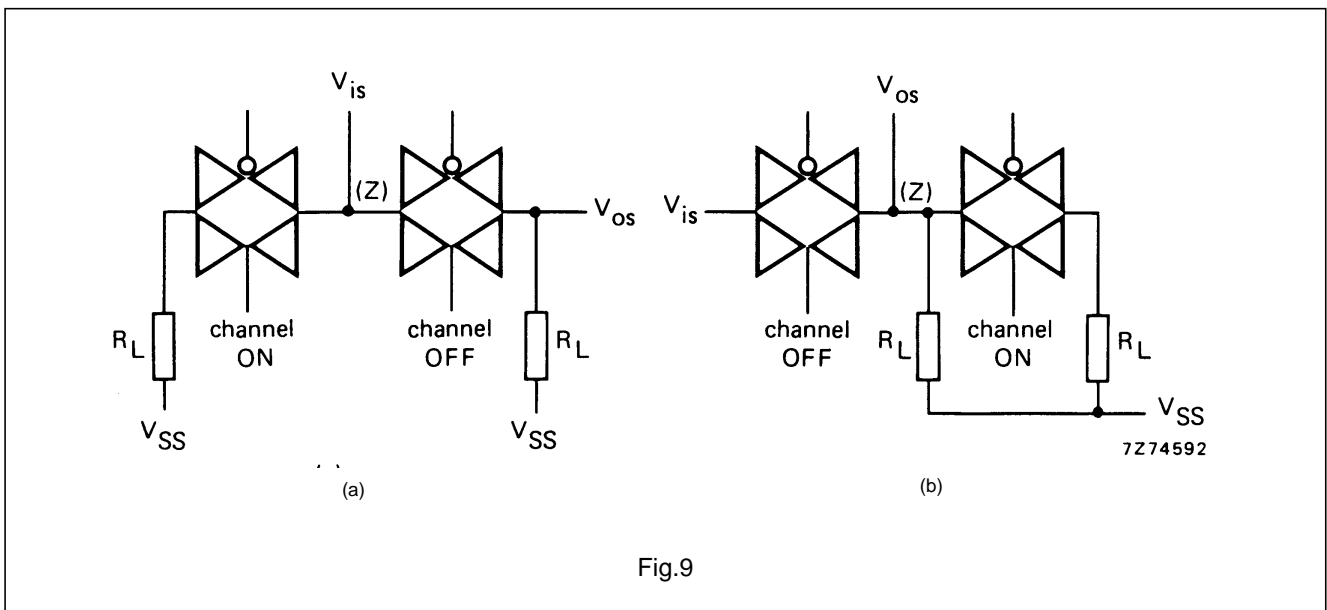
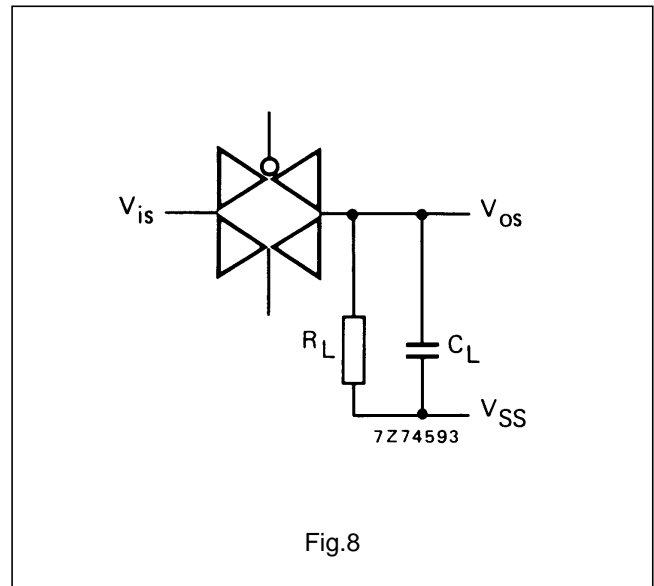
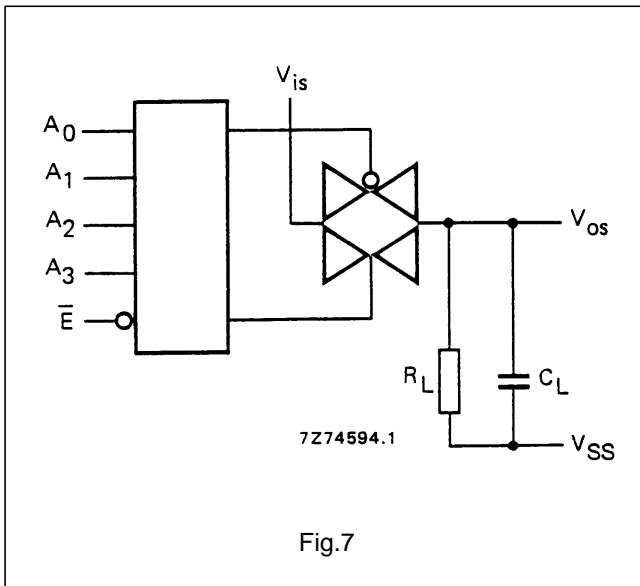
$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB; see Fig.8.}$$

- $R_L = 1$ k Ω ; $C_L = 5$ pF; channel ON; $V_{is} = \frac{1}{2} V_{DD(p-p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);

$$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB; see Fig.8.}$$

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APPLICATION INFORMATION

Some examples of applications for the HEF4067B are:

- Analogue multiplexing and demultiplexing.
- Digital multiplexing and demultiplexing.
- Signal gating.

NOTE

If break before make is needed, then it is necessary to use the enable input.