

# DATA SHEET

**74ALVCH16952**

**16-bit registered transceiver (3-State)**

Preliminary specification  
Supersedes data of 1994 Jul  
IC24 Data Handbook

1998 Sep 01

## 16-bit registered transceiver (3-State)

## 74ALVCH16952

## FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through pin-out architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50Ω transmission lines @ 85°C

## DESCRIPTION

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the clock (CP<sub>XX</sub>, where X is AB or BA) provided that the clock enable ( $\overline{CE}_{XX}$ ) is LOW. The data is then present at the 3-State output buffers, but is only accessible when the output enable input ( $\overline{OE}_{XX}$ ) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

## QUICK REFERENCE DATA

GND = 0V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> = 2.5ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay CP <sub>n</sub> , to A <sub>n</sub> , B <sub>n</sub>	V <sub>CC</sub> = 3.3V, C <sub>L</sub> = 50pF V <sub>CC</sub> = 2.5V, C <sub>L</sub> = 30pF	3.2	ns
f <sub>MAX</sub>	Maximum clock frequency		350	MHz
C <sub>I</sub>	Input capacitance		3.0	pF
C <sub>PD</sub>	Power dissipation capacitance per buffer	V <sub>I</sub> = GND to V <sub>CC</sub> <sup>1</sup>	30	pF

## NOTES:

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF;

f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16952 DGG	ACH16952 DGG	SOT364-1

FUNCTION TABLE for register A<sub>n</sub> or B<sub>n</sub>

INPUTS			INTERNAL Q	OPERATING MODE
A <sub>n</sub> or B <sub>n</sub>	CP <sub>XX</sub>	$\overline{CE}_{XX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

H = HIGH voltage level

L = LOW voltage level

↑ = LOW-to-HIGH transition

## FUNCTION TABLE for output enable

INPUTS	INTERNAL Q	A <sub>n</sub> or B <sub>n</sub> OUTPUTS	OPERATING MODE
$\overline{OE}_{nn}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

NC = no change

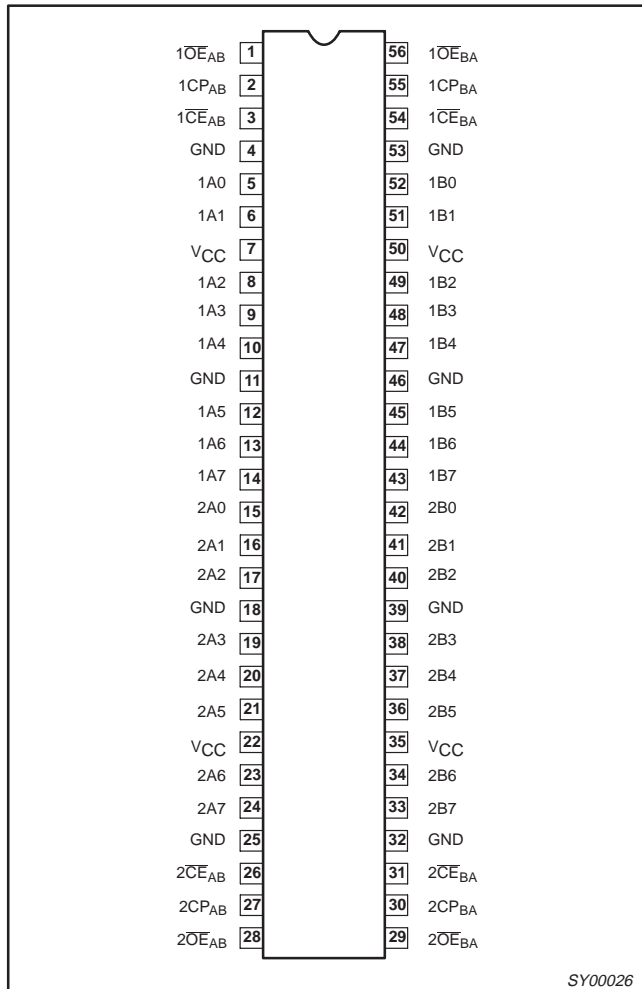
X = don't care

Z = high impedance OFF-state

# 16-bit registered transceiver (3-State)

# 74ALVCH16952

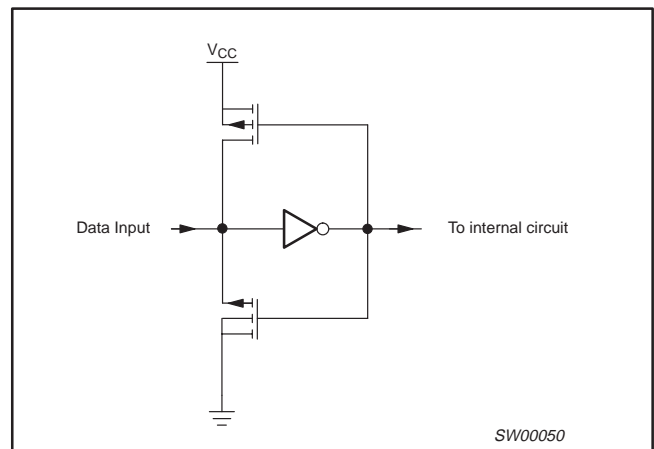
## PIN CONFIGURATION



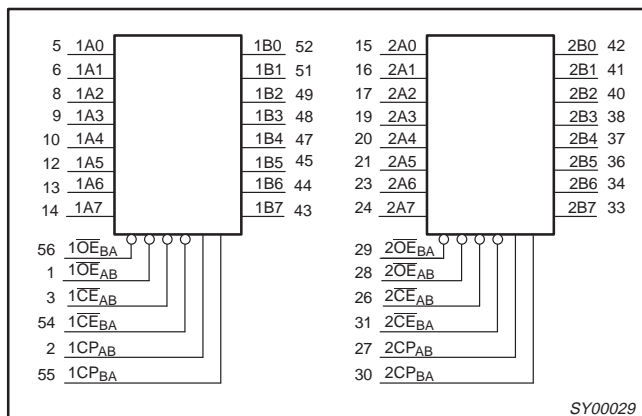
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 28	$\overline{nOE}_{AB}$	Output enable A-to-B
2, 27	$\overline{nCP}_{AB}$	Clock input A-to-B
3, 26	$\overline{nCE}_{AB}$	A-to-B enable
5, 6, 8, 9, 10, 12, 13, 14	1A0 to 1A7	Data inputs/outputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage
15, 16, 17, 19, 20, 21, 23, 24	2B0 to 2B7	Data inputs/outputs
29, 56	$\overline{nOE}_{BA}$	Output enable B-to-A
30, 55	$\overline{nCP}_{BA}$	Clock input B-to-A
31, 54	$\overline{nCE}_{BA}$	B-to-A enable
42, 41, 40, 38, 37, 36, 34, 33	2B0 to 2B7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43	1B0 to 1B7	Data inputs/outputs

## BUSHOLD CIRCUIT



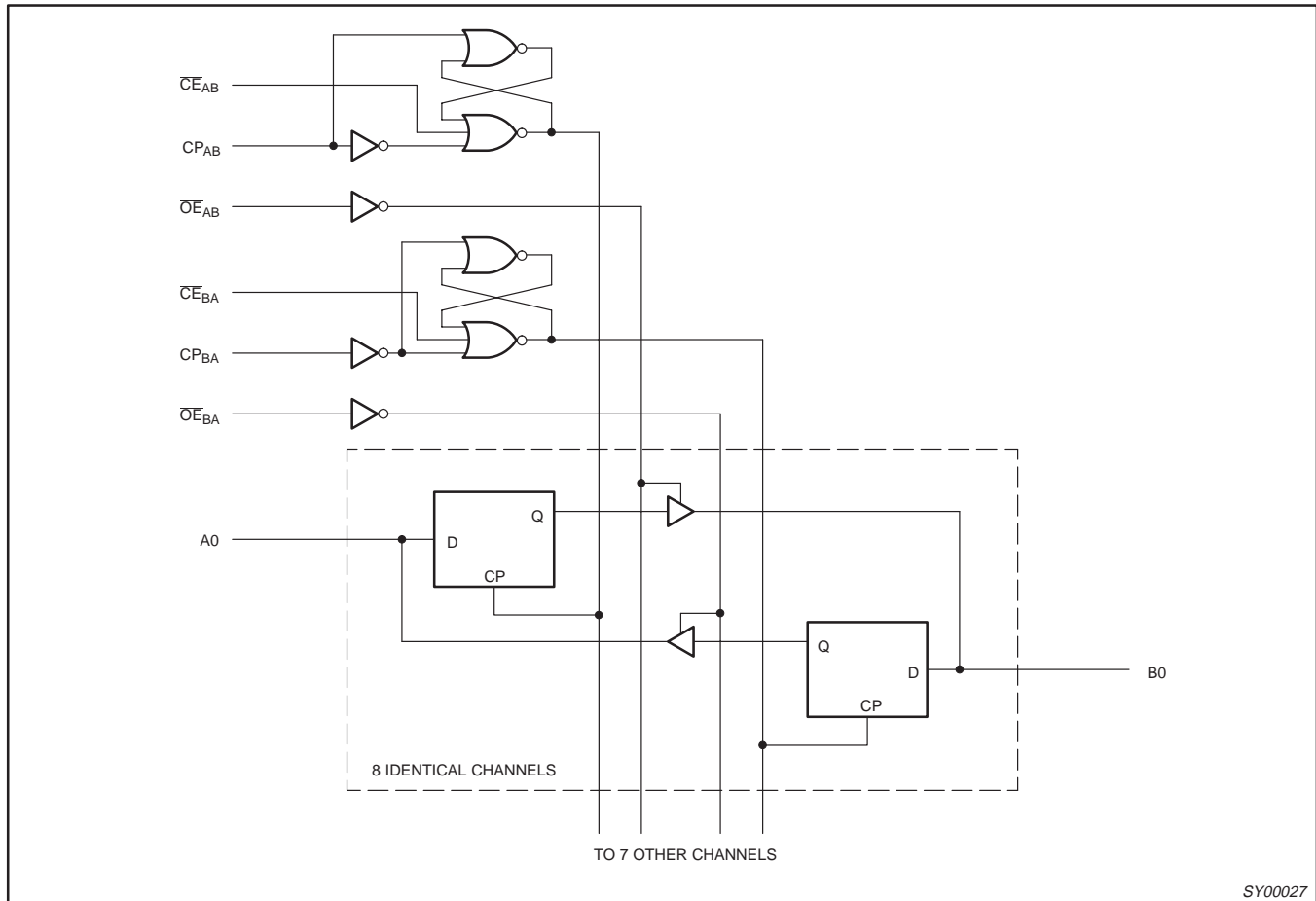
## LOGIC SYMBOL



# 16-bit registered transceiver (3-State)

74ALVCH16952

## LOGIC SYMBOL (one section)

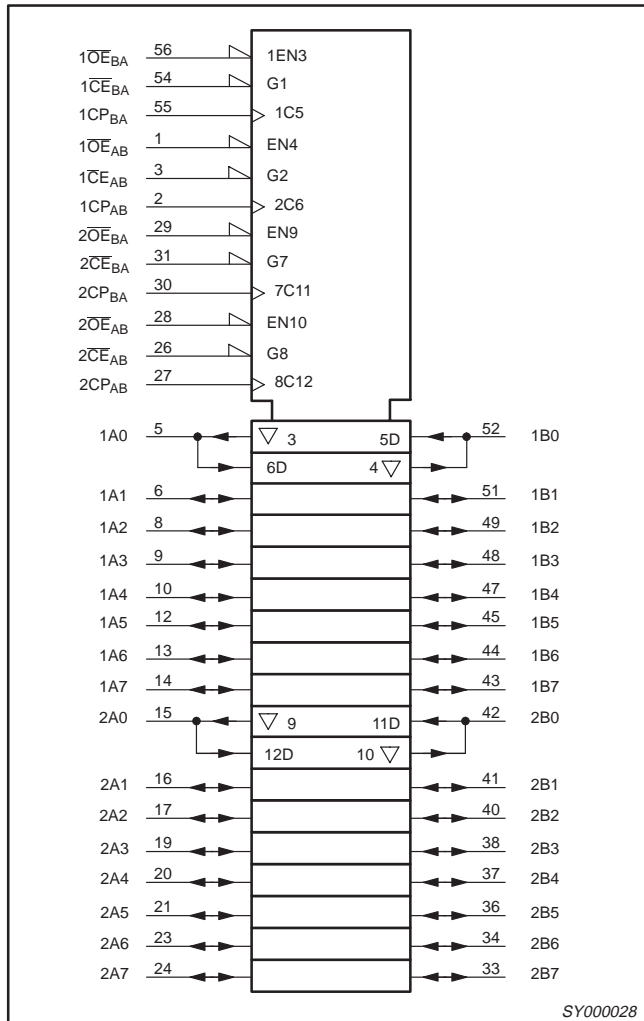


SY00027

# 16-bit registered transceiver (3-State)

74ALVCH16952

## LOGIC SYMBOL (IEEE/IEC)



## 16-bit registered transceiver (3-State)

74ALVCH16952

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
$V_I$	DC Input voltage range		0	$V_{CC}$	V
$V_O$	DC output voltage range		0	$V_{CC}$	V
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 2.3$ to $3.0V$ $V_{CC} = 3.0$ to $3.6V$	0 0	20 10	ns/V

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	For control pins <sup>1</sup>	-0.5 to +4.6	V
		For data inputs <sup>1</sup>	-0.5 to $V_{CC} + 0.5$	
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage	Note 1	-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: -40 to +125 °C	850	mW
		above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	600	

## NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 16-bit registered transceiver (3-State)

74ALVCH16952

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V	1.7	1.2		V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0	1.5		
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.3 to 2.7V		1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6V		1.5	0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -6mA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08		
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26		
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28		
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA		0.07	0.40	V
		V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.15	0.70	V
		V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA		0.14	0.40	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA		0.27	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		0.1	5	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND		0.1	10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 2.3 to 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.2	40	μA
ΔI <sub>CC</sub>	Additional quiescent supply current	V <sub>CC</sub> = 2.3V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		150	750	μA
I <sub>BHL</sub>	Bus hold LOW sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V <sup>2</sup>	45	-		μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2</sup>	75	150		
I <sub>BHH</sub>	Bus hold HIGH sustaining current	V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V <sup>2</sup>	-45			μA
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2</sup>	-75	-175		
I <sub>BHLO</sub>	Bus hold LOW overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	500			μA
I <sub>BHHO</sub>	Bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6V <sup>2</sup>	-500			μA

**NOTES:**

1. All typical values are at T<sub>amb</sub> = 25°C.
2. Valid for data inputs of bus hold parts.

## 16-bit registered transceiver (3-State)

74ALVCH16952

**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE**GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 2.5V \pm 0.2V$			
			MIN	TYP	MAX	
$t_{PLH}/t_{PHL}$	Propagation delay nCP <sub>AB</sub> to nBn, nCP <sub>BA</sub> to nAn	3	1.0		4.1	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE to nAn, nBn	4	1.0		5.4	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE to nAn, nBn	4	1.0		5.3	ns
$t_W$	Pulse width HIGH or LOW nCP <sub>AB</sub> , nCP <sub>BA</sub>	3	3.3			ns
$t_{SU}$	Set up time An or Bn before CP <sub>AB</sub>	3	1.7			ns
	Set up time CE <sub>AB</sub> or CE <sub>BA</sub> before CP <sub>AB</sub>	3	1.2			
$t_h$	Hold time An or Bn after CP <sub>AB</sub>	3	0.6			ns
	Hold time An or Bn after CP <sub>AB</sub>	3	1.1			
$F_{max}$	Maximum clock pulse frequency	3	150			MHz

**NOTE:**1. All typical values are at  $V_{CC} = 2.5V$  and  $T_{amb} = 25^\circ C$ .**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$** GND = 0V;  $t_r = t_f = 2.5ns$ ;  $C_L = 50pF$ 

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$			
			MIN	TYP <sup>1, 2</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay nCP <sub>AB</sub> to nBn, nCP <sub>BA</sub> to nAn	1, 4	1.0		3.9	1.0		4.6	ns
$t_{PZH}/t_{PZL}$	3-State output enable time nOE to nAn, nBn	2, 4	1.0		4.4	1.0		5.3	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time nOE to nAn, nBn	2, 4	1.1		4	1.4		4.4	ns
$t_W$	Pulse width HIGH or LOW nCP <sub>AB</sub> , nCP <sub>BA</sub>	3, 4	3.3			3.3			ns
$t_{SU}$	Set up time An or Bn before CP <sub>AB</sub>	3, 4	1.5			1.9			ns
	Set up time CE <sub>AB</sub> or CE <sub>BA</sub> before CP <sub>AB</sub>	3, 4	1			1			
$t_h$	Hold time An or Bn after CP <sub>AB</sub>	3, 4	0.8			0.6			ns
	Hold time An or Bn after CP <sub>AB</sub>	3, 4	1.1			0.9			
$F_{max}$	Maximum clock pulse frequency	1, 4	150			150			MHz

**NOTES:**1. All typical values are at  $T_{amb} = 25^\circ C$ .2.  $V_{CC} = 3.3V$



# 16-bit registered transceiver (3-State)

74ALVCH16952

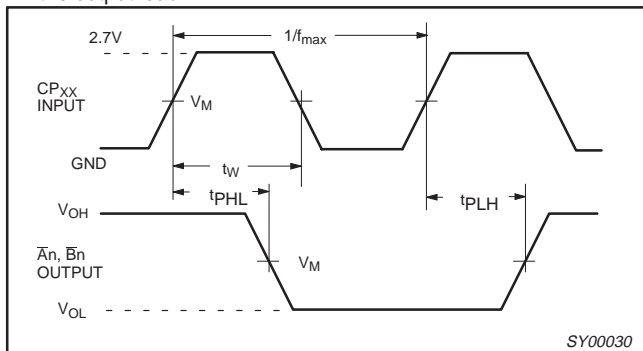
## AC WAVEFORMS

### V<sub>CC</sub> = 2.3 TO 2.7 V RANGE

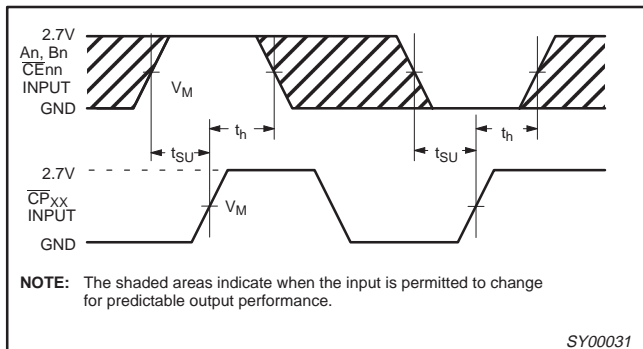
1. V<sub>M</sub> = 0.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.15V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.15V
4. V<sub>I</sub> = V<sub>CC</sub>
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.

### V<sub>CC</sub> = 3.0 TO 3.6 V RANGE AND V<sub>CC</sub> = 2.7 V

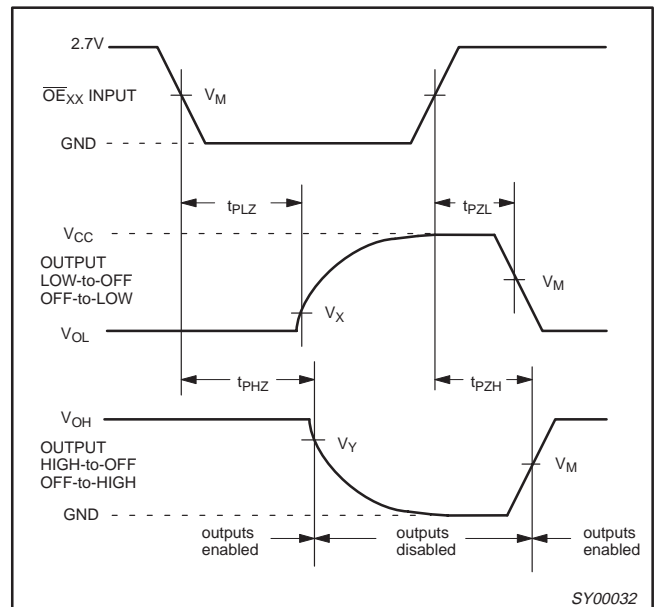
1. V<sub>M</sub> = 1.5 V
2. V<sub>X</sub> = V<sub>OL</sub> + 0.3V
3. V<sub>Y</sub> = V<sub>OH</sub> - 0.3V
4. V<sub>I</sub> = 2.7 V
5. V<sub>OL</sub> and V<sub>OH</sub> are the typical output voltage drop that occur with the output load.



**Waveform 1. Clock input (CP<sub>BA</sub>, CP<sub>AB</sub>) to output (B<sub>n</sub>, A<sub>n</sub>) propagation delays, the clock pulse width and the maximum clock pulse frequency.**

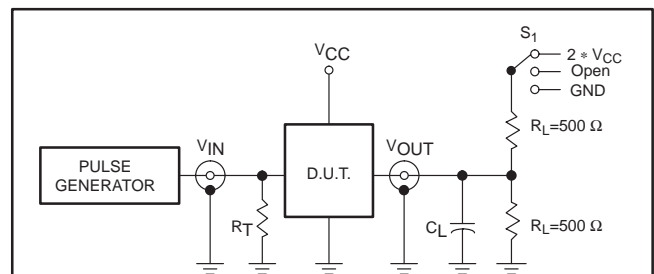


**Waveform 2. Set-up and hold times for the A<sub>n</sub>, B<sub>n</sub> and CE<sub>XX</sub> inputs.**



**Waveform 3. 3-State enable and disable times**

## TEST CIRCUIT



**Test Circuit for 3-State Outputs**

### SWITCH POSITION

TEST	SWITCH
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	2 * V <sub>CC</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

V <sub>CC</sub>	V <sub>IN</sub>
< 2.7V	V <sub>CC</sub>
2.7 – 3.6V	2.7V

### DEFINITIONS

- R<sub>L</sub> = Load resistor
- C<sub>L</sub> = Load capacitance includes jig and probe capacitance
- R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

SW00047

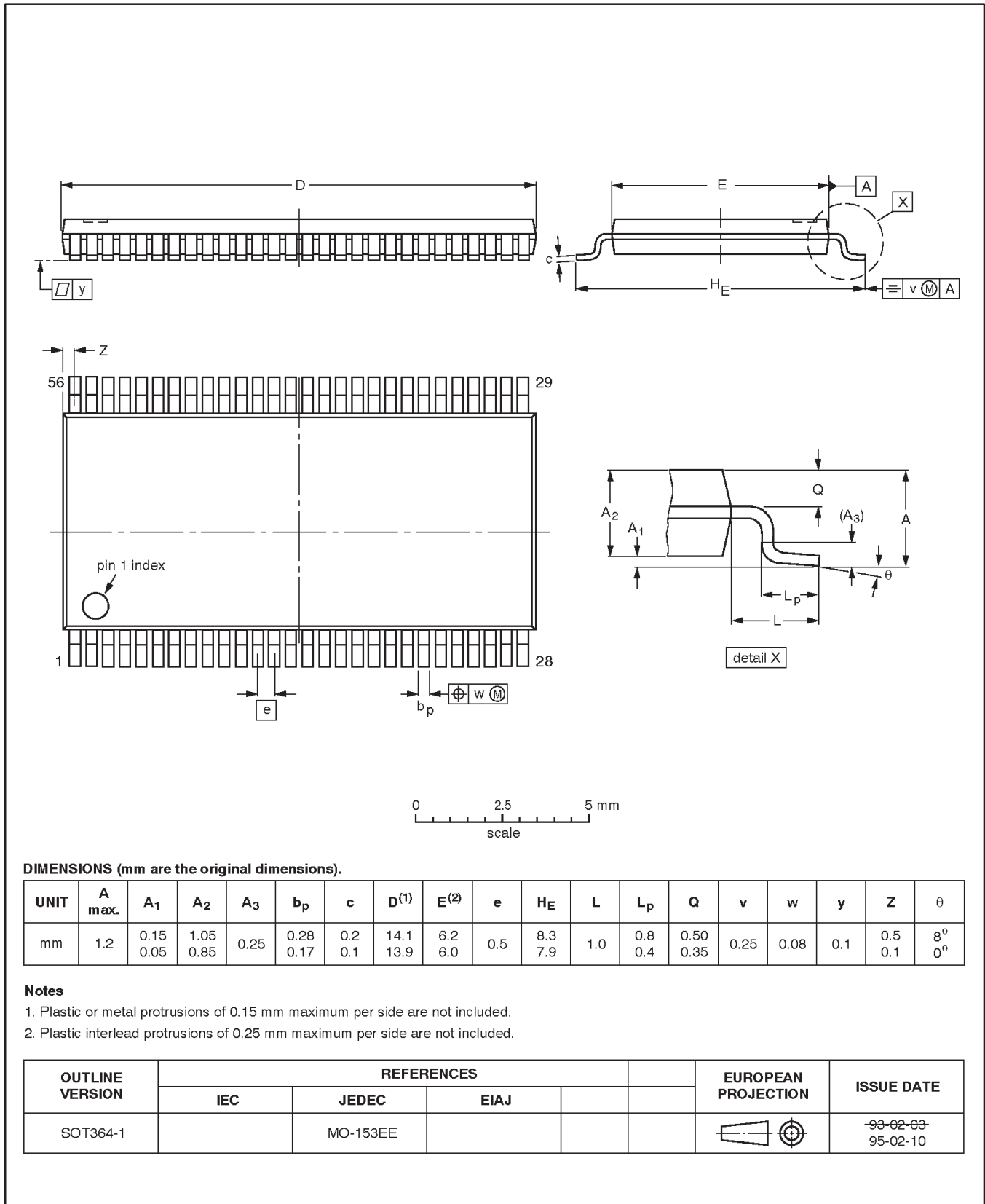
**Load circuitry for switching times**

# 16-bit registered transceiver (3-State)

# 74ALVCH16952

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm**

**SOT364-1**



---

16-bit registered transceiver (3-State)

74ALVCH16952

---

**NOTES**

## 16-bit registered transceiver (3-State)

74ALVCH16952

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
<i>Product Specification</i>	<b>Full Production</b>	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## LIFE SUPPORT APPLICATIONS

Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

**Philips Semiconductors**  
**811 East Arques Avenue**  
**P.O. Box 3409**  
**Sunnyvale, California 94088-3409**  
**Telephone 800-234-7381**

© Copyright Philips Electronics North America Corporation 1998  
 All rights reserved. Printed in U.S.A.

Date of release: 06-98

Document order number:

9397-750-04563

*Let's make things better.*