

# DATA SHEET

## **74ALVCH32501**

**36-bit universal bus transceiver with  
direction pin; 5 V tolerant; 3-state**

Product specification  
File under Integrated Circuits, IC24

2000 Mar 16

## 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

# 74ALVCH32501

### FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Wide supply voltage range of 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A
- Current drive  $\pm 24$  mA at 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- CMOS low power consumption
- Direct interface with TTL levels
- All inputs have bus-hold circuitry
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Plastic fine-pitch ball grid array package.

### DESCRIPTION

The 74ALVCH32501 is a high-performance CMOS product designed for  $V_{CC}$  operation at 2.5 and 3.3 V with I/O compatibility up to 5 V.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### QUICK REFERENCE DATA

$GND = 0$  V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 30$ pF; $V_{CC} = 2.5$ V	2.8	ns
		$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.0	ns
$C_I$	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		8.0	pF
$C_{PD}$	power dissipation capacitance per latch	$V_I = GND$ to $V_{CC}$ ; note 1		
		outputs enabled	21	pF
		outputs disabled	3	pF

### Note

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

The 74ALVCH32501 can be used as two 18-bit transceivers or one 36-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $OE_{AB}$  and  $\overline{OE}_{BA}$ ), latch enable ( $LE_{AB}$  and  $LE_{BA}$ ), and clock inputs ( $CP_{AB}$  and  $CP_{BA}$ ). For A-to-B data flow, the device operates in the transparent mode when  $LE_{AB}$  is HIGH. When input  $LE_{AB}$  is LOW, the A data is latched if input  $CP_{AB}$  is held at a HIGH or LOW level. If input  $LE_{AB}$  is LOW, the A data is stored in the latch/flip-flop on the LOW-to-HIGH transition of  $CP_{AB}$ . When input  $OE_{AB}$  is HIGH, the outputs are active. When input  $OE_{AB}$  is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B, but uses inputs  $\overline{OE}_{BA}$ ,  $LE_{BA}$  and  $CP_{BA}$ . The output enables are complementary ( $OE_{AB}$  is active HIGH, and  $\overline{OE}_{BA}$  is active LOW).

To ensure the high-impedance state during power-up or power-down, pin  $\overline{OE}_{BA}$  should be tied to  $V_{CC}$  through a pull-up resistor and pin  $OE_{AB}$  should be tied to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking or current-sourcing capability of the driver.

**36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state**

74ALVCH32501

**FUNCTION TABLE**

See notes 1 and 2.

INPUT				INTERNAL REGISTERS	OUTPUT	OPERATING MODE
nOE <sub>AB</sub>	nLE <sub>AB</sub>	nCP <sub>AB</sub>	nA <sub>n</sub>		nB <sub>n</sub>	
L	H	X	X	X	Z	disabled
L	↓	X	h	H	Z	disabled; latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	disabled; hold data
L	L	↑	h	H	Z	disabled; clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	latch data and display
H	↓	X	l	L	L	
H	L	↑	h	H	H	clock data and display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	hold data and display
H	L	H or L	X	L	L	

**Notes**

- A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{nOE}_{BA}$ ,  $nLE_{BA}$  and  $nCP_{BA}$ .
- H = HIGH voltage level;  
h = HIGH voltage level on set-up time prior to the enable or clock transition;  
L = LOW voltage level;  
l = LOW voltage level on set-up time prior to the enable or clock transition;  
NC = no change;  
X = don't care;  
↑ = LOW-to-HIGH enable or clock transition;  
↓ = HIGH-to-LOW enable or clock transition;  
Z = high impedance OFF-state.

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

74ALVCH32501

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH32501EC	-40 to +85 °C	114	LFBGA114	plastic	SOT537-1

PINNING

SYMBOL	DESCRIPTION
nA <sub>n</sub>	data inputs
nB <sub>n</sub>	data outputs
GND	ground (0 V)
V <sub>CC</sub>	DC supply voltage
nOE <sub>AB</sub>	output enable inputs A to B (active HIGH)
n $\overline{O}E_{BA}$	output enable inputs B to A (active LOW)
nLE <sub>AB</sub>	latch enable inputs A to B
nLE <sub>BA</sub>	latch enable inputs B to A
nCP <sub>AB</sub>	clock input A to B
nCP <sub>BA</sub>	clock input B to A

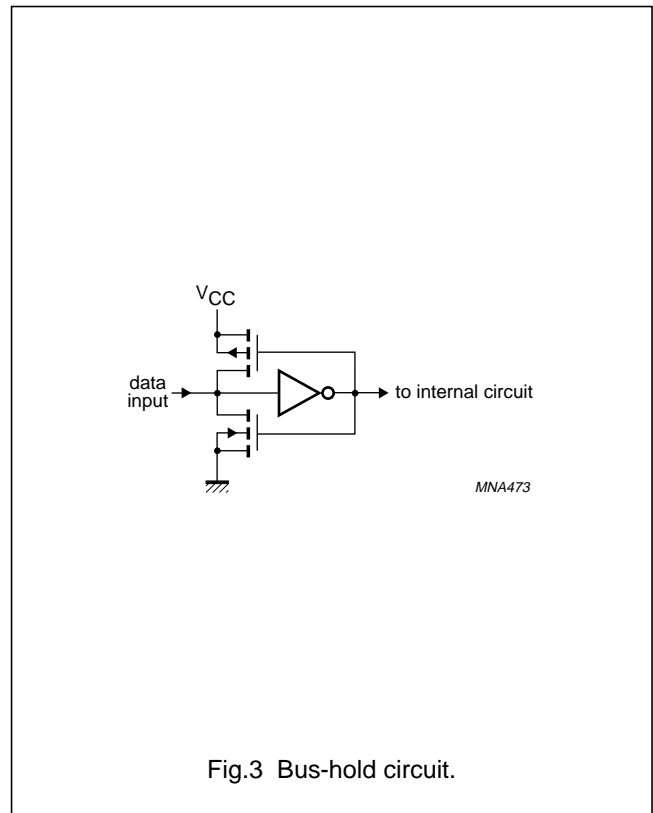
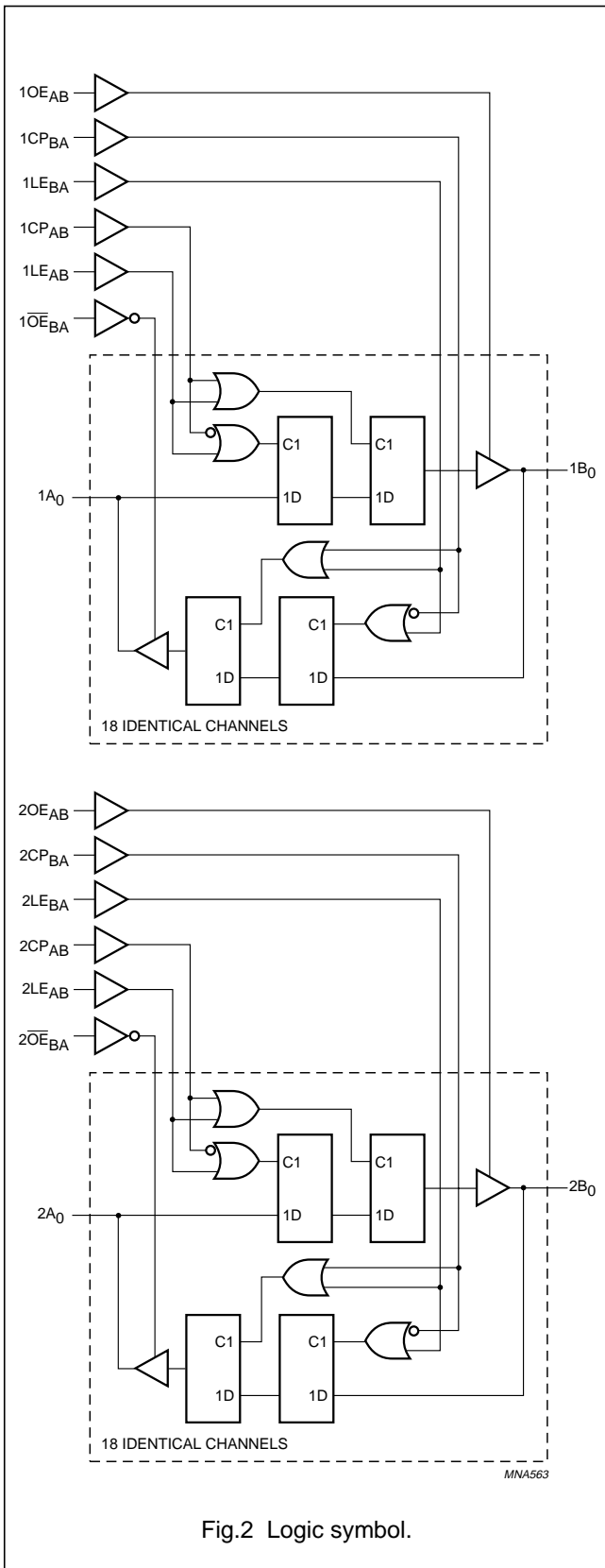
6	1B <sub>1</sub>	1B <sub>3</sub>	1B <sub>5</sub>	1B <sub>7</sub>	1B <sub>9</sub>	1B <sub>11</sub>	1B <sub>13</sub>	1B <sub>14</sub>	1B <sub>16</sub>	n.c.	2B <sub>1</sub>	2B <sub>3</sub>	2B <sub>5</sub>	2B <sub>7</sub>	2B <sub>9</sub>	2B <sub>11</sub>	2B <sub>13</sub>	2B <sub>14</sub>	2B <sub>16</sub>
5	1B <sub>0</sub>	1B <sub>2</sub>	1B <sub>4</sub>	1B <sub>6</sub>	1B <sub>8</sub>	1B <sub>10</sub>	1B <sub>12</sub>	1B <sub>15</sub>	1B <sub>17</sub>	2CP <sub>AB</sub>	2B <sub>0</sub>	2B <sub>2</sub>	2B <sub>4</sub>	2B <sub>6</sub>	2B <sub>8</sub>	2B <sub>10</sub>	2B <sub>12</sub>	2B <sub>15</sub>	2B <sub>17</sub>
4	1CP <sub>AB</sub>	GND	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1CP <sub>BA</sub>	GND	GND	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2CP <sub>BA</sub>	GND
3	1LE <sub>AB</sub>	1OE <sub>AB</sub>	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1 $\overline{O}E_{BA}$	1LE <sub>BA</sub>	2OE <sub>AB</sub>	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2 $\overline{O}E_{BA}$	2LE <sub>BA</sub>
2	1A <sub>0</sub>	1A <sub>2</sub>	1A <sub>4</sub>	1A <sub>6</sub>	1A <sub>8</sub>	1A <sub>10</sub>	1A <sub>12</sub>	1A <sub>15</sub>	1A <sub>17</sub>	2LE <sub>AB</sub>	2A <sub>0</sub>	2A <sub>2</sub>	2A <sub>4</sub>	2A <sub>6</sub>	2A <sub>8</sub>	2A <sub>10</sub>	2A <sub>12</sub>	2A <sub>15</sub>	2A <sub>17</sub>
1	1A <sub>1</sub>	1A <sub>3</sub>	1A <sub>5</sub>	1A <sub>7</sub>	1A <sub>9</sub>	1A <sub>11</sub>	1A <sub>13</sub>	1A <sub>14</sub>	1A <sub>16</sub>	n.c.	2A <sub>1</sub>	2A <sub>3</sub>	2A <sub>5</sub>	2A <sub>7</sub>	2A <sub>9</sub>	2A <sub>11</sub>	2A <sub>13</sub>	2A <sub>14</sub>	2A <sub>16</sub>
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

MNA562

Fig.1 Pin configuration.

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

74ALVCH32501



## 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

74ALVCH32501

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	DC supply voltage	2.5 V range (for maximum speed performance at 30 pF output load)	2.3	2.7	V
		3.3 V range (for maximum speed performance at 50 pF output load)	3.0	3.6	V
V <sub>I</sub>	DC input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	DC output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall time ratios (Δt/ΔV)	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5	+4.6	V
V <sub>I</sub>	DC input voltage	for control pins; note 1	-0.5	+4.6	V
		for data input pins; note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-	-50	mA
I <sub>OK</sub>	DC output clamping diode current	V <sub>O</sub> < 0; note 1	-	50	mA
V <sub>O</sub>	DC output voltage	see note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	DC output sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	-50	mA
I <sub>CC</sub> , I <sub>GND</sub>	DC V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>D</sub>	power dissipation per packages	for temperature range: -40 to +85 °C; note 2	-	1000	mW

### Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- Above 55 °C the value of P<sub>D</sub> derates linearly with 1.8 mW/K.

# 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

74ALVCH32501

## DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> (°C)			UNIT
		OTHER	V <sub>CC</sub> (V)	-40 to +85			
				MIN.	TYP. <sup>(1)</sup>	MAX.	
V <sub>IH</sub>	HIGH-level input voltage		2.3 to 2.7	1.7	1.2	–	V
			2.7 to 3.6	2.0	1.5	–	V
V <sub>IL</sub>	LOW-level input voltage		2.3 to 2.7	–	1.2	0.7	V
			2.7 to 3.6	–	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –100 µA I <sub>O</sub> = –6 mA I <sub>O</sub> = –12 mA I <sub>O</sub> = –12 mA I <sub>O</sub> = –12 mA I <sub>O</sub> = –24 mA	2.3 to 3.6	V <sub>CC</sub> – 0.2	V <sub>CC</sub>	–	V
			2.3	V <sub>CC</sub> – 0.3	V <sub>CC</sub> – 0.08	–	V
			2.3	V <sub>CC</sub> – 0.6	V <sub>CC</sub> – 0.26	–	V
			2.7	V <sub>CC</sub> – 0.5	V <sub>CC</sub> – 0.14	–	V
			3.0	V <sub>CC</sub> – 0.6	V <sub>CC</sub> – 0.09	–	V
			3.0	V <sub>CC</sub> – 1.0	V <sub>CC</sub> – 0.28	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA I <sub>O</sub> = 6 mA I <sub>O</sub> = 12 mA I <sub>O</sub> = 12 mA I <sub>O</sub> = 24 mA	2.3 to 3.6	–	GND	0.20	V
			2.3	–	0.07	0.40	V
			2.3	–	0.15	0.70	V
			2.7	–	0.14	0.40	V
			3.0	–	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 to 3.6	–	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; note 2	2.3 to 3.6	–	0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	2.3 to 3.6	–	0.4	80	µA
ΔI <sub>CC</sub>	additional quiescent supply current given per data I/O pin with bus-hold	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	150	750	µA
I <sub>BHL</sub>	bus-hold LOW sustaining current	V <sub>I</sub> = 0.7 V; note 3	2.3	45	–	–	µA
		V <sub>I</sub> = 0.8 V; note 3	3.0	75	150	–	µA
I <sub>BHH</sub>	bus-hold HIGH sustaining current	V <sub>I</sub> = 1.7 V; note 3	2.3	–45	–	–	µA
		V <sub>I</sub> = 2.0 V; note 3	3.0	–75	–175	–	µA
I <sub>BHLO</sub>	bus-hold LOW overdrive current	note 3	3.6	500	–	–	µA
I <sub>BHHO</sub>	bus-hold HIGH overdrive current	note 3	3.6	–500	–	–	µA

### Notes

1. All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
3. Valid for data inputs of bus-hold parts.

# 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

74ALVCH32501

**AC CHARACTERISTICS**

GND = 0 V

SYMBOL	PARAMETER	TEST CONDITIONS		T <sub>amb</sub> = -40 to +85 °C			UNIT
		WAVEFORMS	C <sub>L</sub>	MIN.	TYP.	MAX.	
<b>V<sub>CC</sub> = 2.3 to 2.7 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.0 ns; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to nB <sub>n</sub> ; nB <sub>n</sub> to nA <sub>n</sub>	see Figs 4 and 8	30 pF	1.0	2.8	5.1	ns
	nLE <sub>BA</sub> to nA <sub>n</sub> ; nLE <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8		1.1	3.5	6.1	ns
	nCP <sub>BA</sub> to nA <sub>n</sub> ; nCP <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8		1.0	3.3	6.1	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8		1.0	2.5	5.8	ns
	3-state output enable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8		1.3	2.8	6.3	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8		1.5	2.5	6.2	ns
	3-state output disable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8		1.3	2.5	5.3	ns
t <sub>w</sub>	nLE <sub>AB</sub> or nLE <sub>BA</sub> pulse width HIGH	see Figs 5 and 8		3.3	0.8	–	ns
	nCP <sub>AB</sub> or nCP <sub>BA</sub> pulse width HIGH or LOW	see Figs 5 and 8		3.3	2.0	–	ns
t <sub>su</sub>	set-up time nA <sub>n</sub> before nCP <sub>AB</sub> ↑ or nB <sub>n</sub> before nCP <sub>BA</sub> ↑	see Figs 7 and 8		1.7	0.1	–	ns
	set-up time CP HIGH or LOW nA <sub>n</sub> before nLE <sub>AB</sub> ↓ or nB <sub>n</sub> before nLE <sub>BA</sub> ↓	see Figs 7 and 8		1.1	0.1	–	ns
t <sub>h</sub>	hold time nA <sub>n</sub> after nCP <sub>AB</sub> ↑ or nB <sub>n</sub> after nCP <sub>BA</sub> ↑	see Figs 7 and 8		1.7	0.3	–	ns
	hold time CP HIGH or LOW nA <sub>n</sub> after nLE <sub>AB</sub> ↓ or nB <sub>n</sub> after nLE <sub>BA</sub> ↓	see Figs 7 and 8		1.6	0.3	–	ns
f <sub>max</sub>	maximum clock frequency	see Figs 5 and 8		150	330	–	MHz
<b>V<sub>CC</sub> = 2.7 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; note 2</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to nB <sub>n</sub> ; nB <sub>n</sub> to nA <sub>n</sub>	see Figs 4 and 8	50 pF	–	3.0	4.6	ns
	nLE <sub>BA</sub> to nA <sub>n</sub> ; nLE <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8		–	3.6	5.3	ns
	nCP <sub>BA</sub> to nA <sub>n</sub> ; nCP <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8		–	3.4	5.6	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8		–	2.7	5.3	ns
	3-state output enable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8		–	3.3	6.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8		–	3.6	5.7	ns
	3-state output disable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8		–	3.3	4.6	ns
t <sub>w</sub>	pulse width nLE <sub>AB</sub> or nLE <sub>BA</sub> HIGH	see Figs 5 and 8		3.3	0.7	–	ns
	pulse width nCP <sub>AB</sub> or nCP <sub>BA</sub> HIGH or LOW	see Figs 5 and 8		3.3	1.4	–	ns



**36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state**

74ALVCH32501

SYMBOL	PARAMETER	TEST CONDITIONS		$T_{amb} = -40 \text{ to } +85 \text{ } ^\circ\text{C}$			UNIT
		WAVEFORMS	$C_L$	MIN.	TYP.	MAX.	
$t_{su}$	set-up time $nA_n$ before $nCP_{AB}\uparrow$ or $nB_n$ before $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	+1.4	-0.1	-	ns
	set-up time CP HIGH or LOW $nA_n$ before $nLE_{AB}\downarrow$ or $nB_n$ before $nLE_{BA}\downarrow$	see Figs 7 and 8		+1.0	-0.2	-	ns
$t_h$	hold time $nA_n$ after $nCP_{AB}\uparrow$ or $nB_n$ after $nCP_{BA}\uparrow$	see Figs 7 and 8		1.6	0.3	-	ns
	hold time CP HIGH or LOW $nA_n$ after $nLE_{AB}\downarrow$ or $nB_n$ after $nLE_{BA}\downarrow$	see Figs 7 and 8		1.5	0.1	-	ns
$f_{max}$	maximum clock frequency	see Figs 5 and 8		150	333	-	MHz
<b><math>V_{CC} = 3.0 \text{ to } 3.6 \text{ V}</math>; <math>t_r = t_f \leq 2.5 \text{ ns}</math>; note 3</b>							
$t_{PHL}/t_{PLH}$	propagation delay $nA_n$ to $nB_n$ ; $nB_n$ to $nA_n$	see Figs 4 and 8	50 pF	1.0	3.0	4.2	ns
	$nLE_{BA}$ to $nA_n$ ; $nLE_{AB}$ to $nB_n$	see Figs 5 and 8		1.3	3.4	4.8	ns
	$nCP_{BA}$ to $nA_n$ ; $nCP_{AB}$ to $nB_n$	see Figs 5 and 8		1.4	3.3	4.9	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8		1.0	2.4	4.6	ns
	3-state output enable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8		1.1	2.5	5.0	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8		1.4	2.9	5.0	ns
	3-state output disable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8		1.3	3.1	4.2	ns
$t_w$	pulse width $nLE_{AB}$ or $nLE_{BA}$ HIGH	see Figs 5 and 8		3.3	0.9	-	ns
	pulse width $nCP_{AB}$ or $nCP_{BA}$ HIGH or LOW	see Figs 5 and 8		3.3	1.1	-	ns
$t_{su}$	set-up time $nA_n$ before $nCP_{AB}\uparrow$ or $nB_n$ before $nCP_{BA}\uparrow$	see Figs 7 and 8		+1.3	-0.3	-	ns
	set-up time CP HIGH or LOW $nA_n$ before $nLE_{AB}\downarrow$ or $nB_n$ before $nLE_{BA}\downarrow$	see Figs 7 and 8		1.0	0.3	-	ns
$t_h$	hold time $nA_n$ after $nCP_{AB}\uparrow$ or $nB_n$ after $nCP_{BA}\uparrow$	see Figs 7 and 8		+1.3	-0.4	-	ns
	hold time CP HIGH or LOW $nA_n$ after $nLE_{AB}\downarrow$ or $nB_n$ after $nLE_{BA}\downarrow$	see Figs 7 and 8		1.2	0.1	-	ns
$f_{max}$	maximum clock frequency	see Figs 5 and 8		150	340	-	MHz

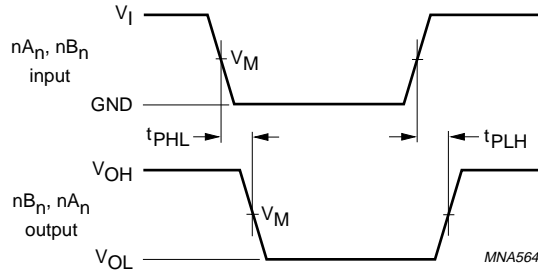
**Notes**

1. All typical values are measured at  $V_{CC} = 2.5 \text{ V}$  and  $T_{amb} = 25 \text{ } ^\circ\text{C}$ .
2. All typical values are measured at  $T_{amb} = 25 \text{ } ^\circ\text{C}$ .
3. All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ } ^\circ\text{C}$ .

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

74ALVCH32501

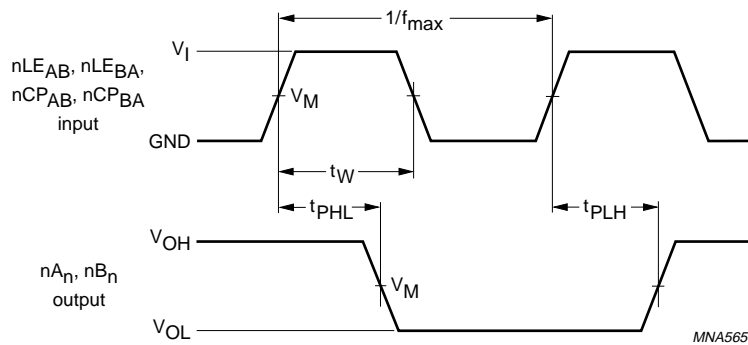
AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.4 Input nA<sub>n</sub>, nB<sub>n</sub> to output nB<sub>n</sub>, nA<sub>n</sub> propagation delay times.



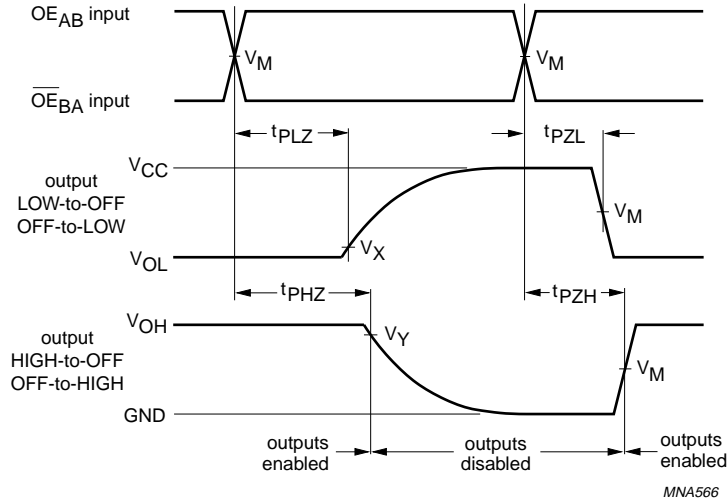
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 Latch enable input (nLE<sub>AB</sub>, nLE<sub>BA</sub>) and clock input (nCP<sub>AB</sub>, nCP<sub>BA</sub>) to output propagation delays and their pulse width.

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

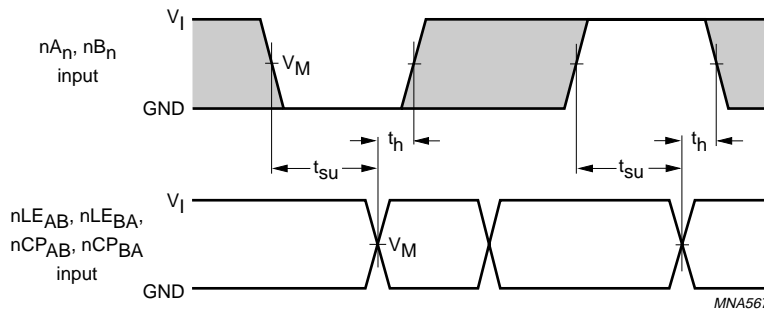
74ALVCH32501



V <sub>CC</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>	V <sub>I</sub>
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 150 mV	V <sub>OH</sub> - 150 mV	V <sub>CC</sub>
2.7 V	1.5 V	V <sub>OL</sub> + 300 mV	V <sub>OH</sub> - 300 mV	2.7 V
3.0 to 3.6 V	1.5 V	V <sub>OL</sub> + 300 mV	V <sub>OH</sub> - 300 mV	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

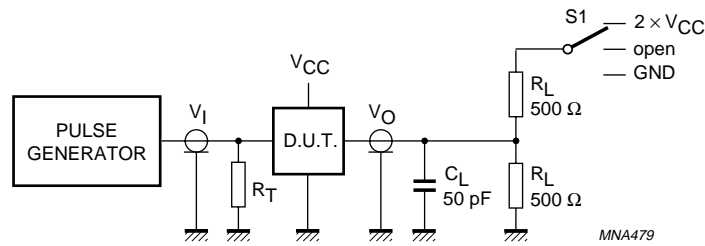
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 Data set-up and hold times for the nA<sub>n</sub> and nB<sub>n</sub> inputs to the nLE<sub>AB</sub>, nLE<sub>BA</sub>, nCP<sub>AB</sub> and nCP<sub>BA</sub> inputs.

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

74ALVCH32501



MNA479

TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

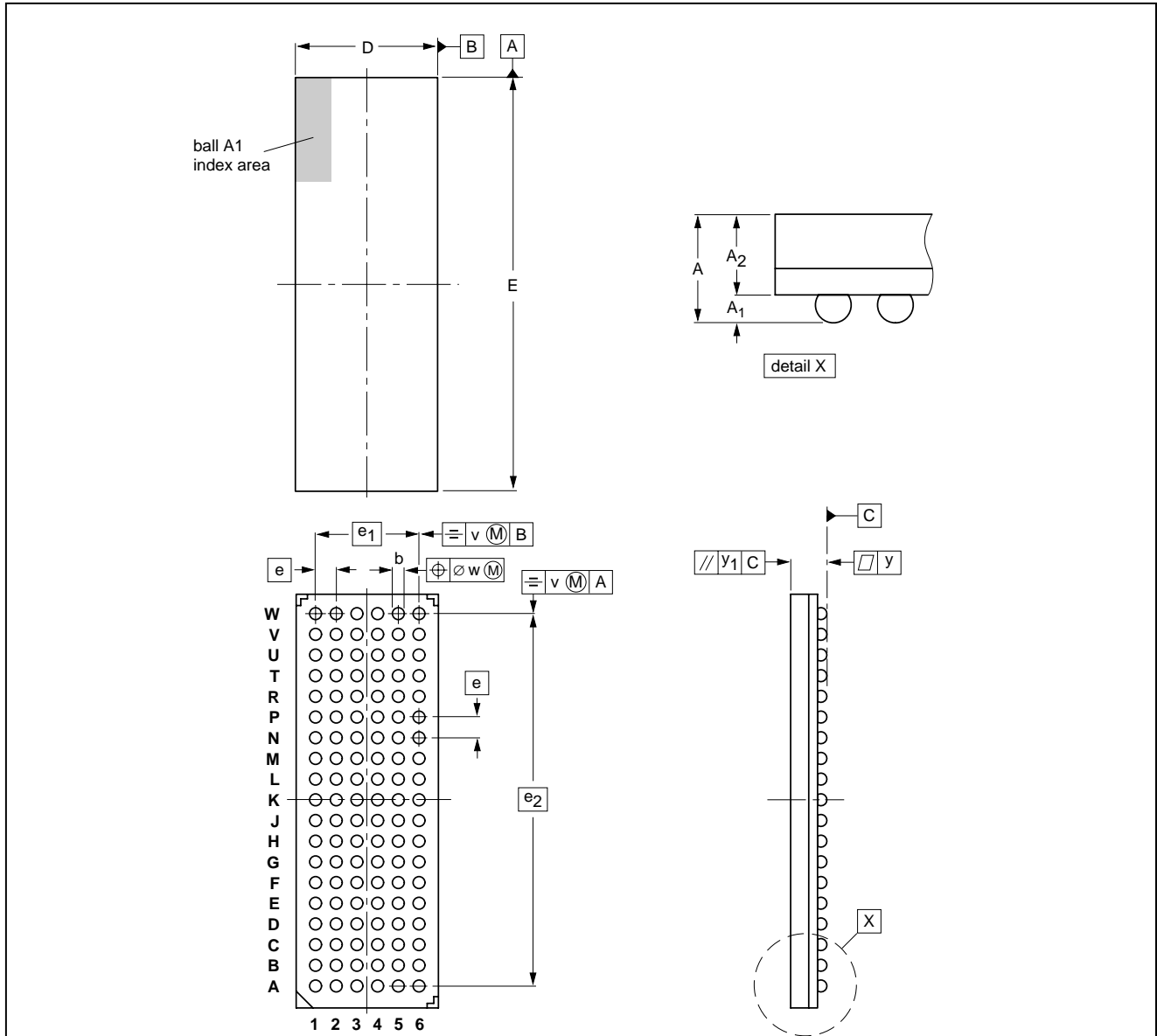
Fig.8 Load circuitry for switching times.

36-bit universal bus transceiver with direction pin;  
5 V tolerant; 3-state

74ALVCH32501

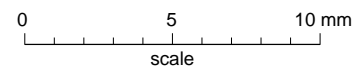
PACKAGE OUTLINE

LFBGA114: plastic low profile fine-pitch ball grid array package; 114 balls; body 16 x 5.5 x 1.05 mm SOT537-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	D	E	e	e <sub>1</sub>	e <sub>2</sub>	v	w	y	y <sub>1</sub>
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	16.1 15.9	0.8	4.0	14.4	0.15	0.1	0.1	0.2



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT537-1						99-12-02-00-03-04

## 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

74ALVCH32501

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 230 °C.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 36-bit universal bus transceiver with direction pin; 5 V tolerant; 3-state

74ALVCH32501

### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

#### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

#### DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

#### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 3 Figtree Drive, HOME BUSH, NSW 2140,  
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

**Belgium:** see The Netherlands

**Brazil:** see South America

**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
51 James Bourchier Blvd., 1407 SOFIA,  
Tel. +359 2 68 9211, Fax. +359 2 68 9102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** PT Philips Development Corporation, Semiconductors Division,  
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,  
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),  
Tel. +39 039 203 6838, Fax +39 039 203 6800

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Pakistan:** see Singapore

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762,  
Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

**Slovenia:** see Italy

**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,  
Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
04547-130 SÃO PAULO, SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 93 301 6312, Fax. +34 93 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2741 Fax. +41 1 488 3263

**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,  
Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,  
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381, Fax. +1 800 943 0087

**Uruguay:** see South America

**Vietnam:** see Singapore

**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 3341 299, Fax.+381 11 3342 553

**For all other countries apply to:** Philips Semiconductors,  
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,  
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

**Internet:** <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 2000

SCA 69

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

613507/01/pp16

Date of release: 2000 Mar 16

Document order number: 9397 750 06819

*Let's make things better.*

**Philips**  
Semiconductors



**PHILIPS**