

# DATA SHEET

## **74LV4052**

Dual 4-channel analog  
multiplexer/demultiplexer

Product specification  
Supersedes data of 1997 Jul 15  
IC24 Data Handbook

1998 Jun 23

## Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## FEATURES

- Optimized for low voltage applications: 1.0 to 6.0 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Low typ "ON" resistance:  
60  $\Omega$  at  $V_{CC} - V_{EE} = 4.5$  V  
90  $\Omega$  at  $V_{CC} - V_{EE} = 3.0$  V  
145  $\Omega$  at  $V_{CC} - V_{EE} = 2.0$  V
- Logic level translation: to enable 3 V logic to communicate with  $\pm 3$  V analog signals
- Typical "break before make" built in
- Analog/Digital multiplexing and demultiplexing
- Signal gating
- Output capability: non-standard
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV4052 is a low-voltage CMOS device and is pin and function compatible with the 74HC/HCT4052.

The 74LV4052 is a dual 4-channel analog multiplexer/demultiplexer with a common select logic. Each multiplexer has four independent inputs/outputs ( $nY_0$  to  $nY_3$ ) and a common input/output ( $nZ$ ). The common channel select logics include two digital select inputs ( $S_0$  and  $S_1$ ) and an active LOW enable input ( $\bar{E}$ ).

With  $\bar{E}$  LOW, one of the four switches is selected (low impedance ON-state) by  $S_0$  and  $S_1$ . With  $\bar{E}$  HIGH, all switches are in the high impedance OFF-state, independent of  $S_0$  and  $S_1$ .  $V_{CC}$  and GND are the supply voltage pins for the digital control inputs ( $S_0$ ,  $S_1$  and  $\bar{E}$ ). The  $V_{CC}$  to GND ranges are 1.0 to 6.0 V. The analog inputs/outputs ( $nY_0$ , to  $nY_3$ , and  $nZ$ ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.  $V_{CC} - V_{EE}$  may not exceed 6.0 V. For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^\circ\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PZH}/t_{PZL}$	Turn "ON" time $\bar{E}$ or $V_{OS} S_n$	$C_L = 15$ pF $R_L = 1\text{K}\Omega$ $V_{CC} = 3.3$ V	30	ns
$t_{PHZ}/t_{PLZ}$	Turn "OFF" time $\bar{E}$ or $V_{OS} S_n$		22	
$C_i$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per switch	See Notes 1 and 2	57	
$C_S$	Maximum switch capacitance independent (Y) common (Z)		5 12	

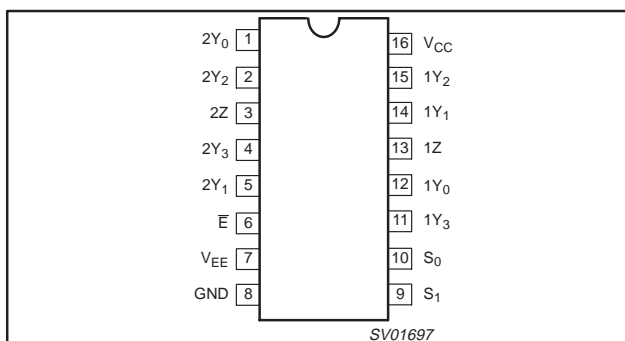
## NOTES:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $C_S$  = maximum switch capacitance in pF;  
 $V_{CC}$  = supply voltage in V;  
 $\sum ((C_L + C_S) \times V_{CC}^2 \times f_o)$  = sum of the outputs.
2. The condition is  $V_i = \text{GND to } V_{CC}$ .

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	Code
16-Pin Plastic DIL	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	74LV4052 N	74LV4052 N	SOT38-4
16-Pin Plastic SO	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	74LV4052 D	74LV4052 D	SOT109-1
16-Pin Plastic SSOP Type II	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	74LV4052 DB	74LV4052 DB	SOT338-1
16-Pin Plastic TSSOP Type I	$-40^\circ\text{C}$ to $+125^\circ\text{C}$	74LV4052 PW	74LV4052PW DH	SOT403-1

## PIN CONFIGURATION



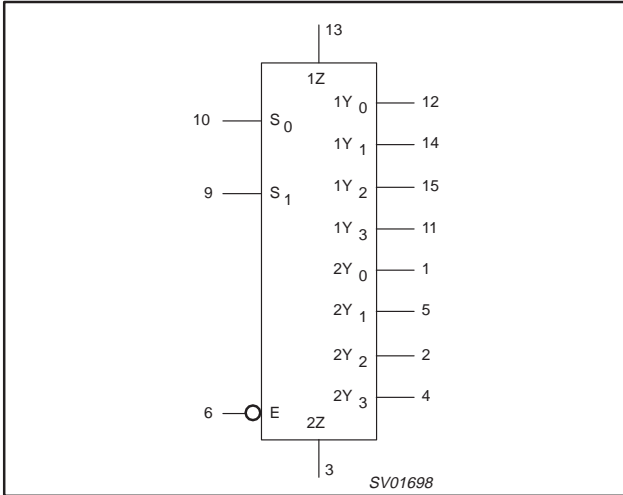
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 5, 2, 4	$2Y_0, 2Y_3$	Independent inputs/outputs
6	$\bar{E}$	Enable input (active LOW)
7	$V_{EE}$	Negative supply voltage
8	GND	Ground (0 V)
10, 9	$S_0, S_1$	Select inputs
12, 14, 15, 11	$1Y_0$ to $1Y_3$	Independent inputs/outputs
13, 3	1Z, 2Z	Common inputs/outputs
16	$V_{CC}$	Positive supply voltage

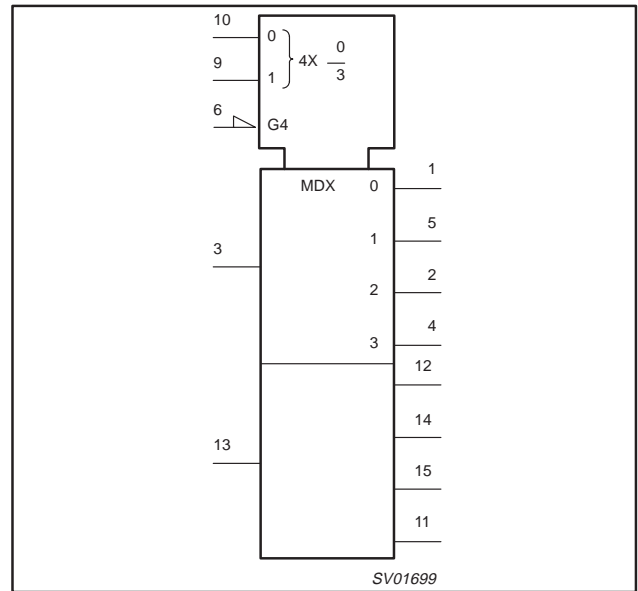
# Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## FUNCTION TABLE

INPUTS			CHANNEL ON
$\bar{E}$	S <sub>1</sub>	S <sub>0</sub>	
L	L	L	nY <sub>0</sub> – nZ
L	L	H	nY <sub>1</sub> – nZ
L	H	L	nY <sub>2</sub> – nZ
L	H	H	nY <sub>3</sub> – nZ
H	X	X	None

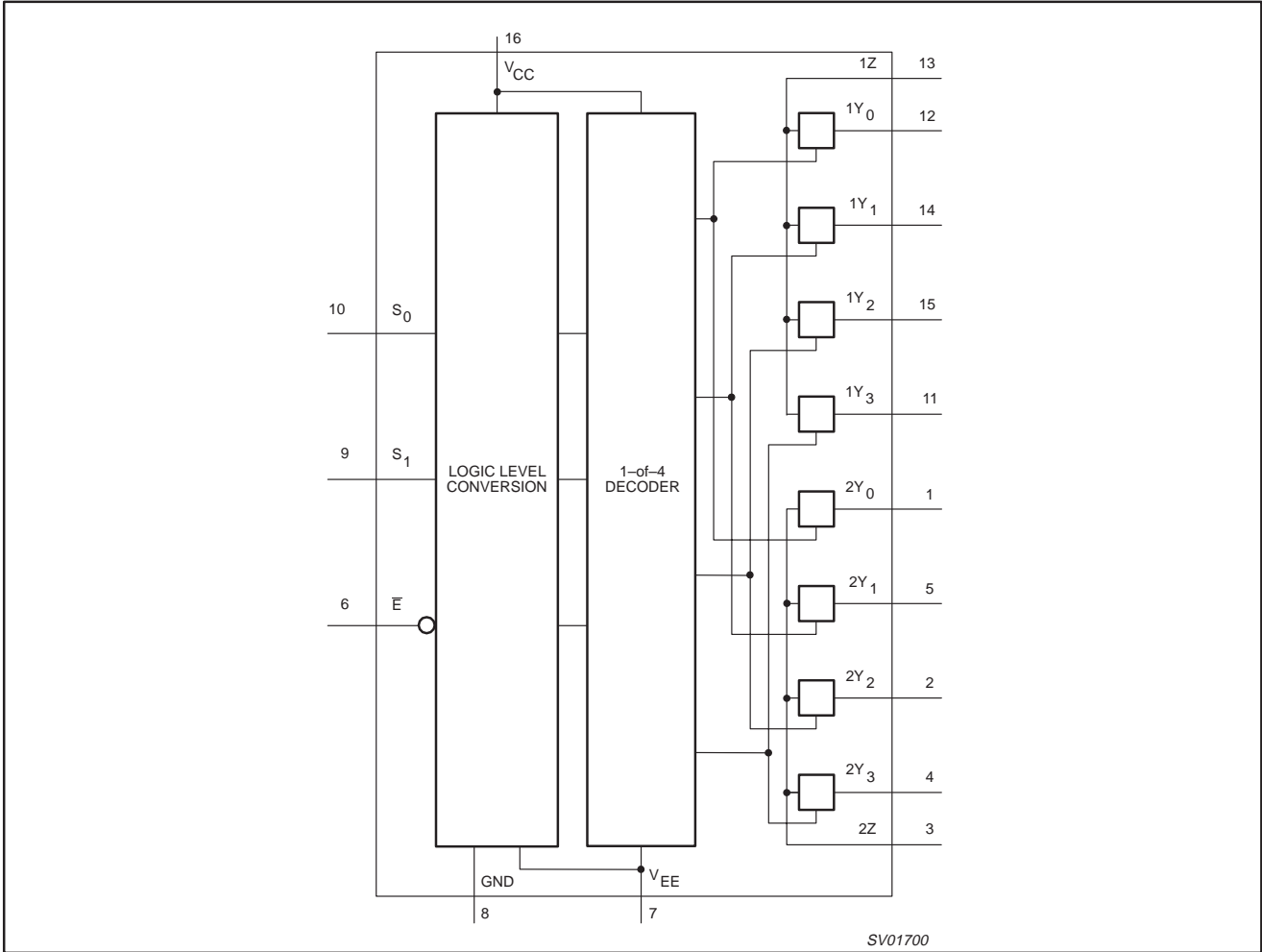
### NOTES:

1. H = HIGH voltage level
2. L = LOW voltage level
3. X = don't care

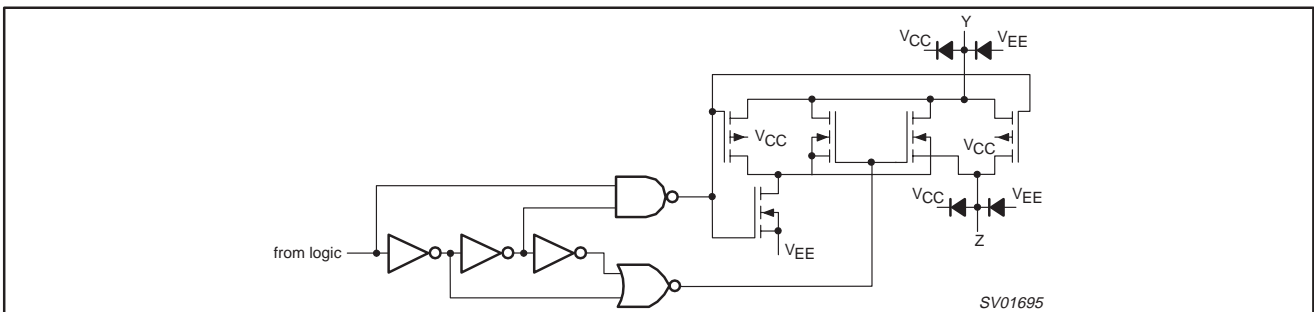
# Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## FUNCTIONAL DIAGRAM



## SCHEMATIC DIAGRAM (ONE SWITCH)



## Dual 4-channel analog multiplexer/demultiplexer

74LV4052

**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134).  
 Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V	20	mA
$\pm I_{SK}$	DC switch diode current	$V_S < -0.5$ or $V_S > V_{CC} + 0.5$ V	20	mA
$\pm I_S$	DC switch current	$-0.5$ V $< V_S < V_{CC} + 0.5$ V	25	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1 and Figure 5	1.0	3.3	6.0	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0$ V to 2.0 V $V_{CC} = 2.0$ V to 2.7 V $V_{CC} = 2.7$ V to 6.0 V	– – –	– – –	500 200 100	ns/V

**NOTE:**

- The LV is guaranteed to function down to  $V_{CC} = 1.0$ V (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2$ V to  $V_{CC} = 6.0$ V.

## Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions, voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2\text{ V}$	0.9			0.9		V
		$V_{CC} = 2.0\text{ V}$	1.4			1.4		
		$V_{CC} = 2.7\text{ to }3.6\text{ V}$	2.0			2.0		
		$V_{CC} = 4.5\text{ V}$	3.15			3.15		
		$V_{CC} = 6.0\text{ V}$	4.20			4.20		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2\text{ V}$			0.3		0.3	V
		$V_{CC} = 2.0\text{ V}$			0.6		0.6	
		$V_{CC} = 2.7\text{ to }3.6\text{ V}$			0.8		0.8	
		$V_{CC} = 4.5\text{ V}$			1.35		1.35	
		$V_{CC} = 6.0\text{ V}$			1.80		1.80	
$\pm I_I$	Input leakage current	$V_{CC} = 3.6$	$V_I = V_{CC}$ or GND			1.0	1.0	$\mu\text{A}$
		$V_{CC} = 6.0$				2.0	2.0	
$\pm I_S$	Analog switch OFF-state current per channel	$V_{CC} = 3.6$	$V_I = V_{IH}$ or $V_{IL}$ $ I_{S1}  = V_{CC} - \text{GND}$ (See Figure 2)			1.0	1.0	$\mu\text{A}$
		$V_{CC} = 6.0$				2.0	2.0	
$\pm I_S$	Analog switch ON-state current	$V_{CC} = 3.6$	$V_I = V_{IH}$ or $V_{IL}$ $ I_{S1}  = V_{CC} - \text{GND}$ (See Figure 3)			1.0	1.0	$\mu\text{A}$
		$V_{CC} = 6.0$				2.0	2.0	
$I_{CC}$	Quiescent supply current	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$ or GND; $V_{IS} = \text{GND}$ or $V_{CC}$ ; $V_{OS} = V_{CC}$ or GND			20.0	40	$\mu\text{A}$
		$V_{CC} = 6.0\text{ V}$				40.0	80	
$\Delta I_{CC}$	Additional quiescent supply current per input	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	$V_I = V_{CC} - 0.6\text{ V}$			500	850	$\mu\text{A}$
$R_{ON}$	ON-resistance (peak)	$V_{CC} = 1.2\text{ V}$	$V_I = V_{IH}$ or $V_{IL}$ ; $I_S = 100\ \mu\text{A}$ ; $V_{IS} = V_{CC}$ to GND					$\Omega$
		$V_{CC} = 2.0\text{ V}$			145	325	375	
		$V_{CC} = 2.7\text{ V}$			90	200	235	
		$V_{CC} = 3.0\text{ to }3.6\text{ V}$			80	180	210	
		$V_{CC} = 4.5\text{ V}$			60	135	160	
$R_{ON}$	ON-resistance (rail)	$V_{CC} = 1.2\text{ V}$	$V_I = V_{IH}$ or $V_{IL}$ ; $I_S = 100\ \mu\text{A}$ ; $V_{IS} = \text{GND}$			225		$\Omega$
		$V_{CC} = 2.0\text{ V}$			110	235	270	
		$V_{CC} = 2.7\text{ V}$			70	145	165	
		$V_{CC} = 3.0\text{ to }3.6\text{ V}$			60	130	150	
		$V_{CC} = 4.5\text{ V}$			45	100	115	
$V_{CC} = 6.0\text{ V}$		40	85	100				

## NOTES:

- All typical values are measured at  $T_{amb} = 25^\circ\text{C}$ .
- At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- $R_{ON}$  (MAX) data is preliminary.

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$R_{ON}$	ON-resistance (rail)	$V_{CC} = 1.2\text{ V}$		250				$\Omega$
		$V_{CC} = 2.0\text{ V}$		120	320		370	$\Omega$
		$V_{CC} = 2.7\text{ V}$		75	195		225	
		$V_{CC} = 3.0\text{ to }3.6\text{ V}$		70	175		205	
		$V_{CC} = 4.5\text{ V}$		50	130		150	
		$V_{CC} = 6.0\text{ V}$		45	120		135	
$\Delta R_{ON}$	Maximum variation of ON-resistance between any two channels	$V_{CC} = 1.2\text{ V}$						$\Omega$
		$V_{CC} = 2.0\text{ V}$		5				
		$V_{CC} = 2.7\text{ V}$		4				
		$V_{CC} = 3.0\text{ to }3.6\text{ V}$		4				
		$V_{CC} = 4.5\text{ V}$		3				
		$V_{CC} = 6.0\text{ V}$		2				

NOTES:

1. All typical values are measured at  $T_{amb} = 25^\circ\text{C}$ .
2. At supply voltages approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
3.  $R_{ON}$  (MAX) data is preliminary.

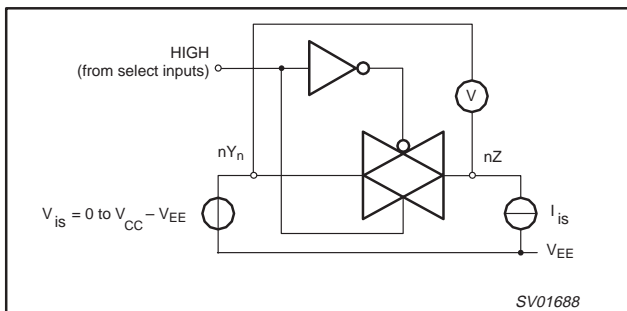


Figure 1. Test circuit for measuring ON-resistance ( $R_{ON}$ ).

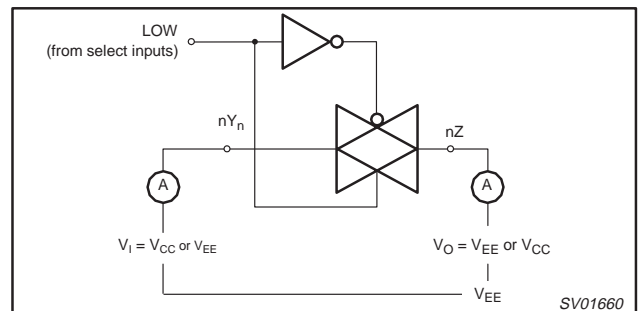


Figure 2. Test circuit for measuring OFF-state current.

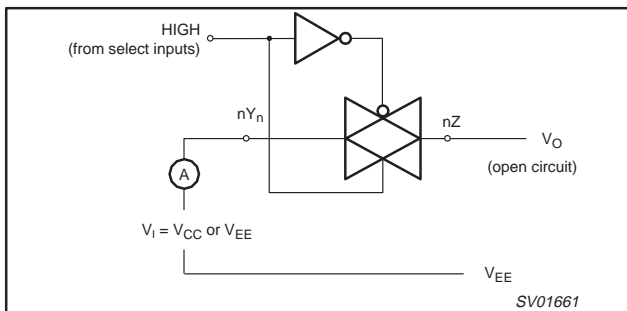


Figure 3. Test circuit for measuring ON-state current.

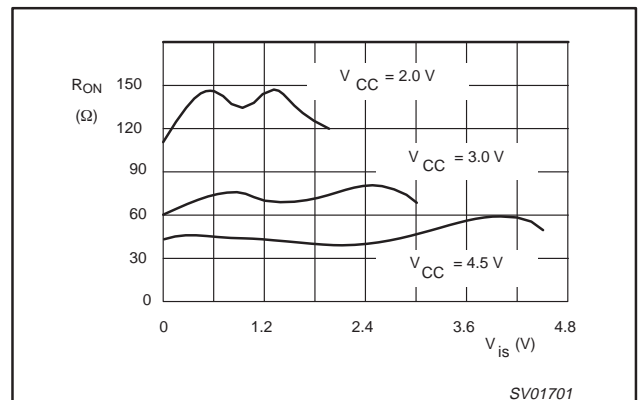


Figure 4. Typical ON-resistance ( $R_{ON}$ ) as a function of input voltage ( $V_{is}$ ) for  $V_{is} = 0$  to  $V_{CC} - V_{EE}$ .

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

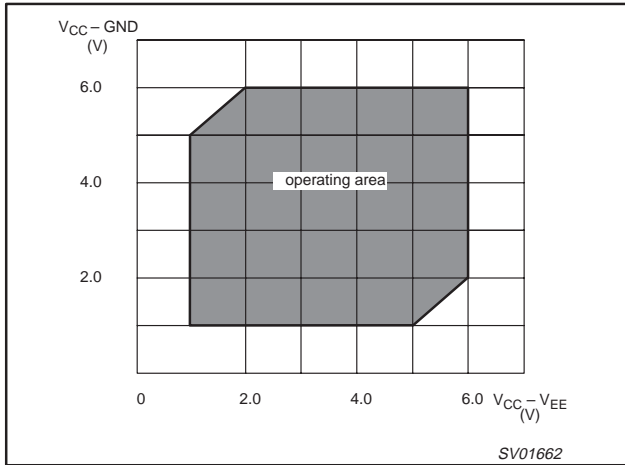


Figure 5. Guaranteed operating area as a function of the supply voltages.

AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \le 2.5\text{ns}$ ;  $C_L = 50\text{pF}$

SYMBOL	PARAMETER	CONDITION		LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
		V <sub>CC</sub> (V)	OTHER	MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay V <sub>is</sub> to V <sub>os</sub>	1.2	R <sub>L</sub> = ∞; C <sub>L</sub> = 50 pF Figure 12		25				ns
		2.0		9	17		20		
		2.7		6	13		15		
		3.0 to 3.6		5 <sup>2</sup>	10		12		
		4.5		4	9		10		
		6.0		3	7		8		
t <sub>PZH</sub> /t <sub>PZL</sub>	Turn-on time E, S <sub>n</sub> to V <sub>OS</sub>	1.2	R <sub>L</sub> = 1kΩ; C <sub>L</sub> = 50 pF Figures 13 and 1		190				ns
		2.0		65	121		146		
		2.7		48	89		108		
		3.0 to 3.6		36 <sup>2</sup>	71		86		
		4.5		32	60		73		
		6.0		25	46		56		
t <sub>PHZ</sub> /t <sub>PLZ</sub>	Turn-off time E, S <sub>n</sub> to V <sub>OS</sub>	1.2	R <sub>L</sub> = 1kΩ; C <sub>L</sub> = 50 pF Figures 13 and 1		125				ns
		2.0		43	80		95		
		2.7		33	59		71		
		3.0 to 3.6		26 <sup>2</sup>	48		57		
		4.5		23	41		49		
		6.0		18	32		38		

NOTES:

1. Unless otherwise stated, all typical values are measured at T<sub>amb</sub> = 25°C
2. Typical values are measured at V<sub>CC</sub> = 3.3 V.



# Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## ADDITIONAL AC CHARACTERISTICS

Recommended conditions and typical values

GND = 0 V;  $t_r = t_f \leq 2.5\text{ns}$

SYMBOL	PARAMETER	TYP.	UNIT	V <sub>CC</sub> (V)	V <sub>is(p-p)</sub> (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80 0.40	%	3.0 6.0	2.75 5.50	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pf Figure 9 and 10
	Sine-wave distortion f = 10 kHz	2.40 1.20	%	3.0 6.0	2.75 5.50	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pf Figure 9 and 10
	Switch "OFF" signal feed through	-50 -50	dB	3.0 6.0	Note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pf; f = 1 MHz Figures 5 and 11
	Crosstalk between any two switches/multiplexers	-60 -60	dB	3.0 6.0	Note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pf; f = 1 MHz Figure 8
V <sub>(p-p)</sub>	Crosstalk voltage between enable or address input to any switch (peak-to-peak value)	110 120	mV	3.0 6.0		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pf; f = 1 MHz (S <sub>n</sub> or $\bar{E}$ , square wave between V <sub>CC</sub> and GND $t_r = t_f = 6\text{ ns}$ ) Figure 8
f <sub>max</sub>	Minimum frequency response (-3 dB)	180 200	MHz	3.0 6.0	Note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 50 pF Figures 6, 8 and 9
C <sub>S</sub>	Maximum switch capacitance	5	pf			

**GENERAL NOTES:**

- V<sub>is</sub> is the input voltage at nY or nZ terminal, whichever is assigned as an input.
- V<sub>OS</sub> is the output voltage at nY or nZ terminal, whichever is assigned as an output.

**NOTES:**

- Adjust input voltage V<sub>is</sub> is 0 dBm level (0 dBm = 1 mW into 600 Ω).
- Adjust input voltage V<sub>is</sub> is 0 dBm level at V<sub>OS</sub> for 1 MHz (0 dBm = 1 mW into 50 Ω).

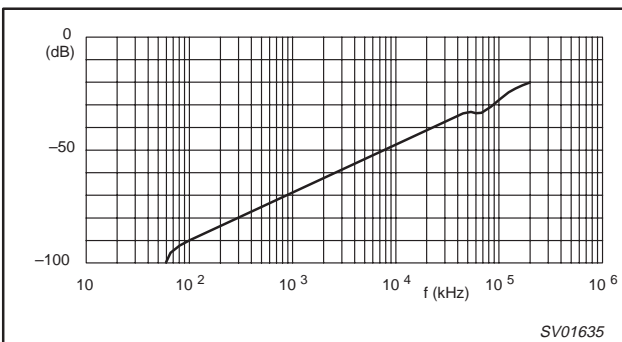


Figure 6. Typical switch "OFF" signal feed-through as a function of frequency.

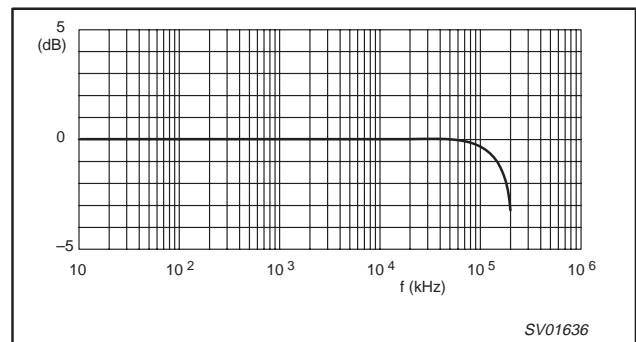


Figure 7. Typical frequency response.

**NOTES TO FIGURES 6 AND 7:**

Test conditions: V<sub>CC</sub> = 3.0 V; GND = 0 V; V<sub>EE</sub> = -3.0 V; R<sub>L</sub> = 50 Ω; R<sub>SOURCE</sub> = 1kΩ.

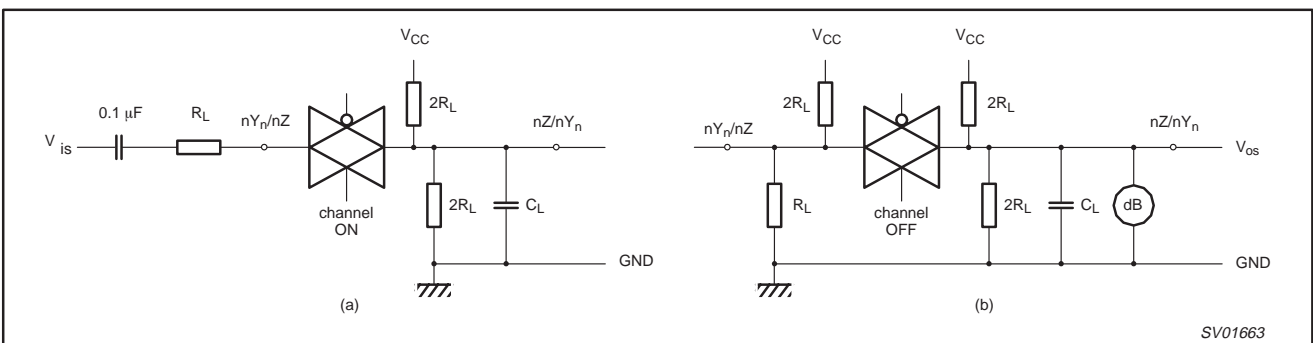


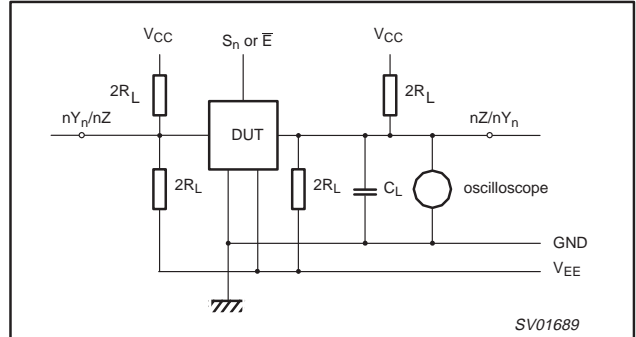
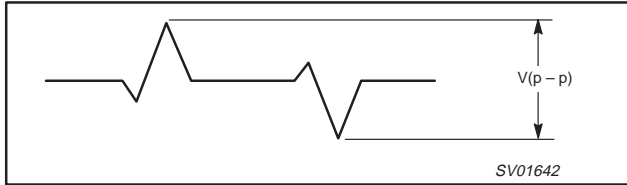
Figure 8. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

**NOTE TO FIGURE 8:**

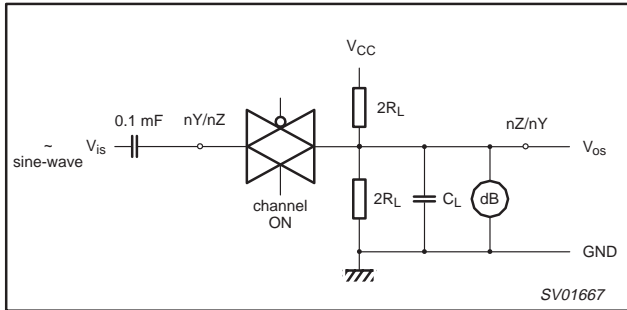
The crosstalk is defined as follows (oscilloscope output):



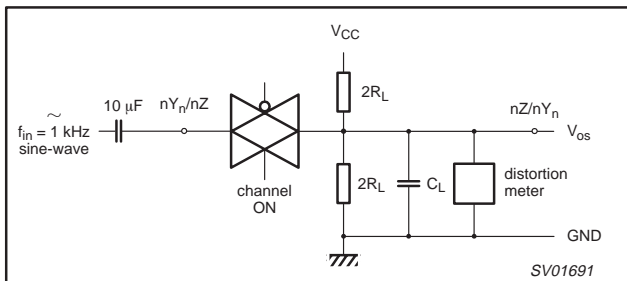
**Figure 9. Test circuit for measuring crosstalk between control and any switch.**

**NOTE TO FIGURE 9:**

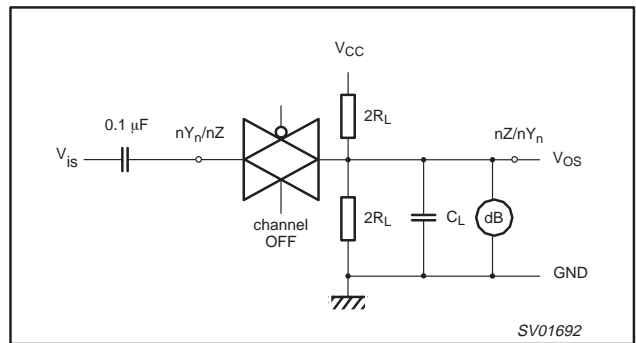
Adjust input voltage to obtain 0 dBm at  $V_{OS}$  when  $F_{in} = 1$  MHz. After set-up frequency of  $f_{in}$  is increased to obtain a reading of  $-3$  dB at  $V_{OS}$ .



**Figure 10. Test circuit for measuring minimum frequency response.**



**Figure 11. Test circuit for measuring sine-wave distortion.**



**Figure 12. Test circuit for measuring switch "OFF" signal feed-through.**

# Dual 4-channel analog multiplexer/demultiplexer

# 74LV4052

## WAVEFORMS

### NOTES:

- $V_M = 1.5\text{ V}$  at  $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$   
 $V_M = 0.5 \times V_{CC}$  at  $2.7\text{ V} > V_{CC} > 3.6\text{ V}$
- $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load
- $V_X = V_{OL} + 0.3\text{ V}$  at  $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$   
 $V_X = V_{OL} + 0.1 \times V_{CC}$  at  $2.7\text{ V} > V_{CC} > 3.6\text{ V}$   
 $V_Y = V_{OH} - 0.3\text{ V}$  at  $2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$   
 $V_Y = V_{OH} - 0.1 \times V_{CC}$  at  $2.7\text{ V} > V_{CC} > 3.6\text{ V}$

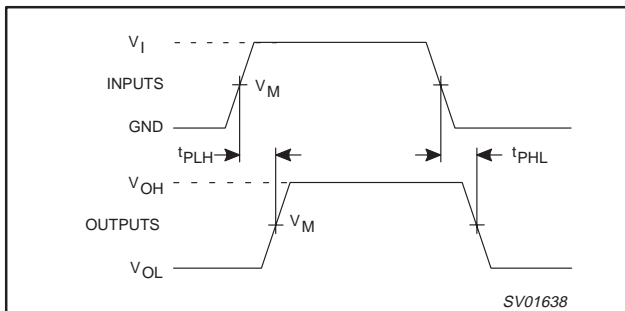


Figure 13. Input ( $V_{1s}$ ) to output ( $V_{0s}$ ) propagation delays.

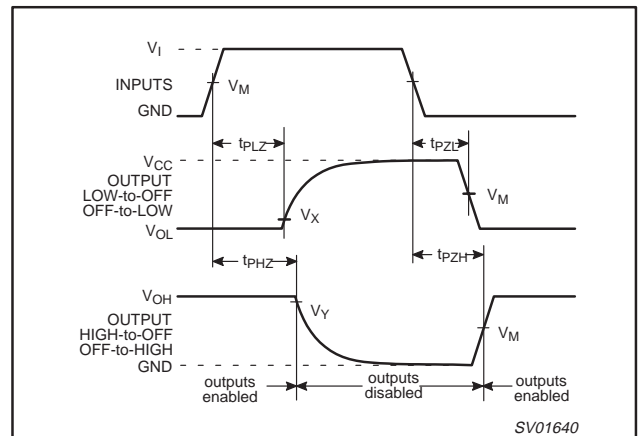


Figure 14. Turn-on and turn-off times for the inputs ( $S_n, \bar{E}$ ) to the output ( $V_{0s}$ ).

## TEST CIRCUIT

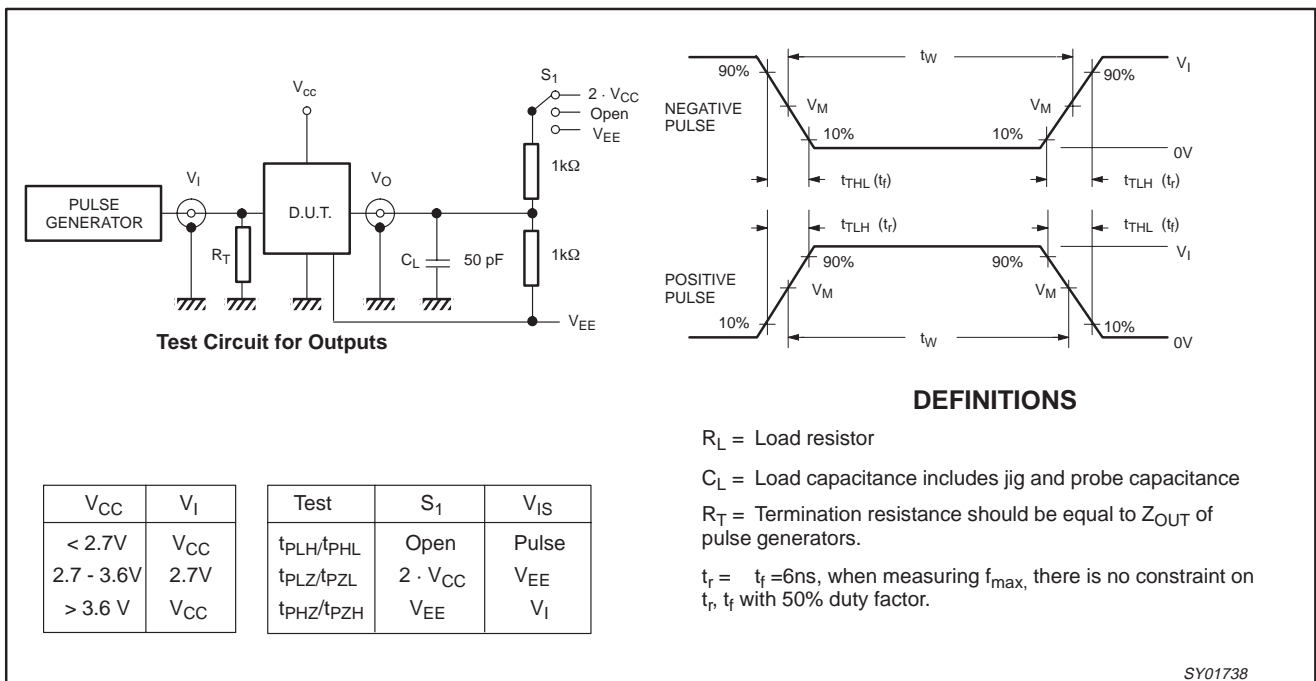


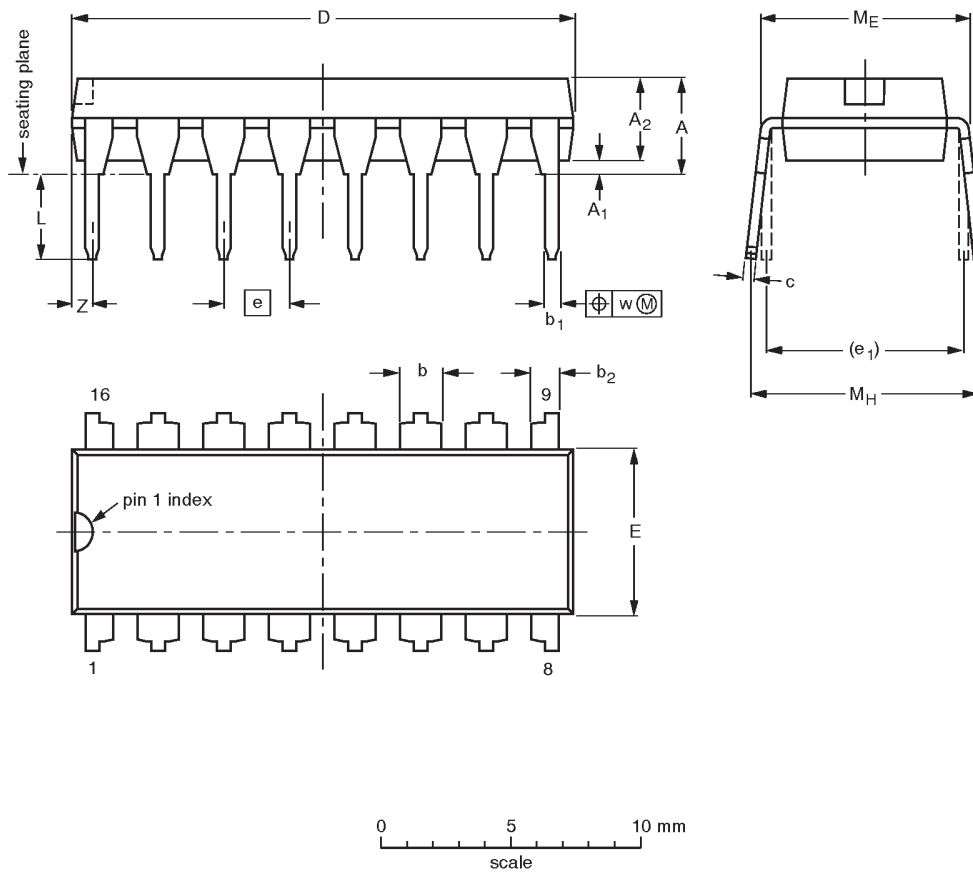
Figure 15. Load circuitry for switching times.

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

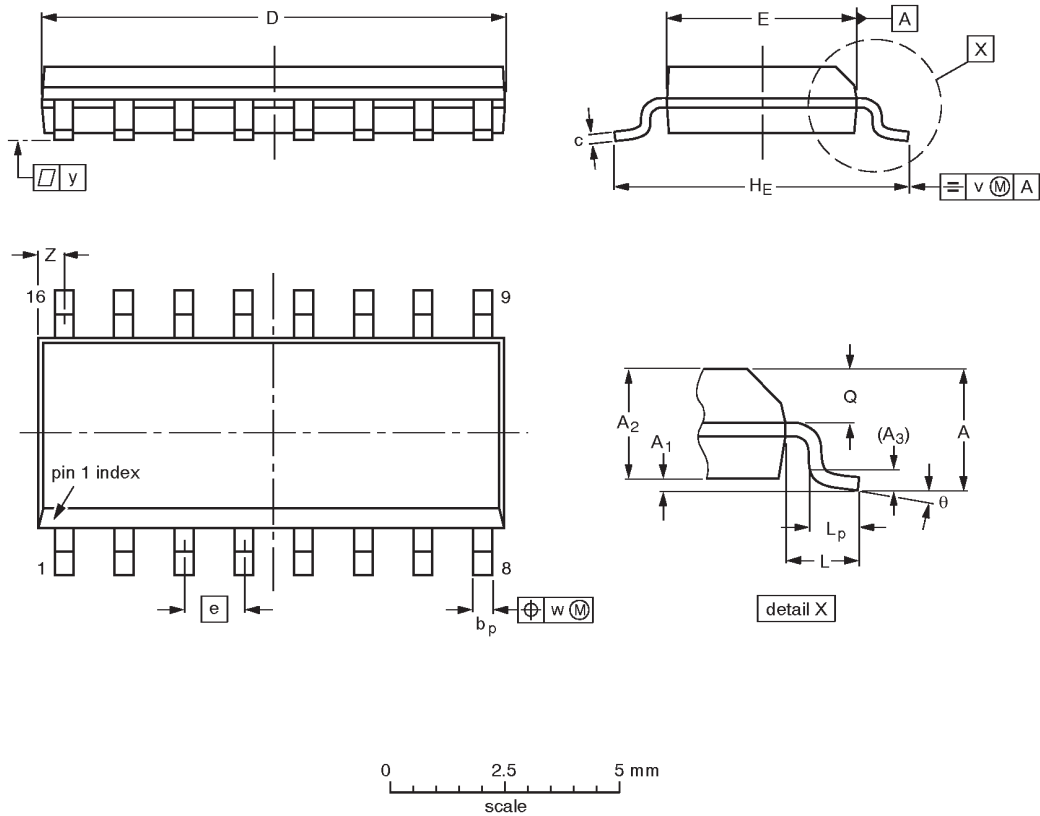
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

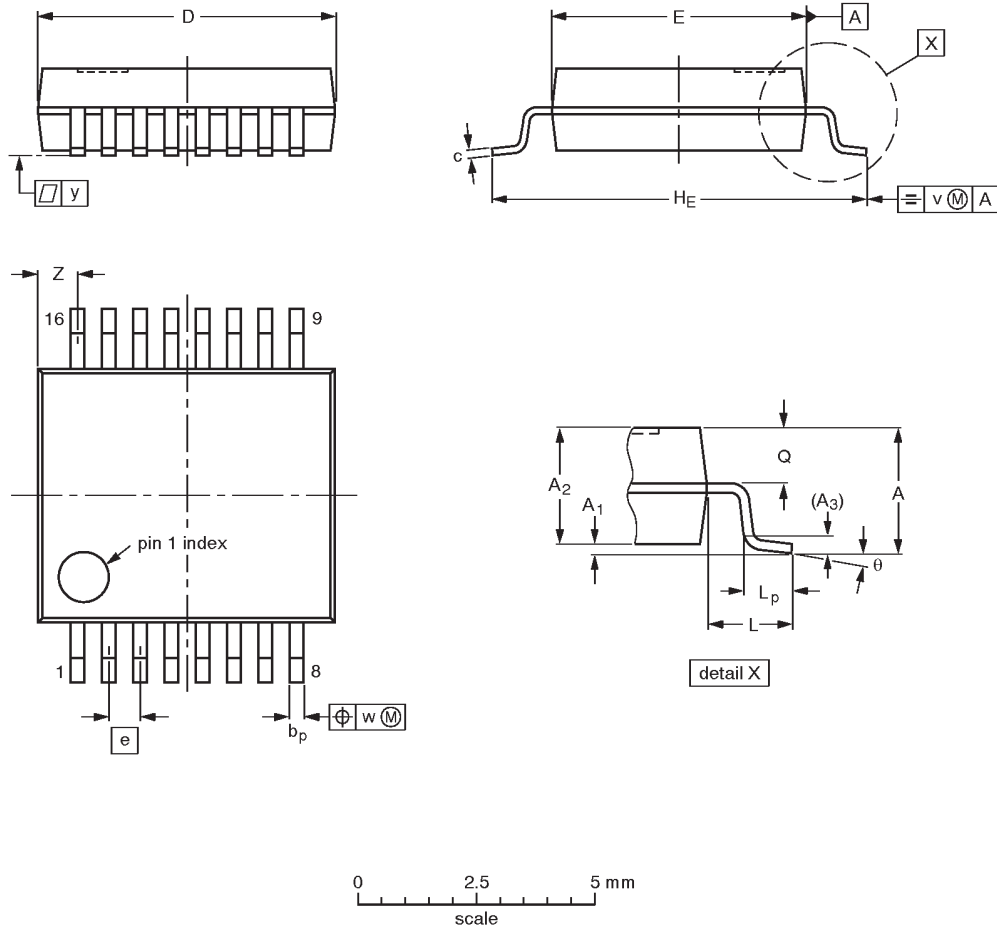
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07S	MS-012AC			91-08-13 95-01-23

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

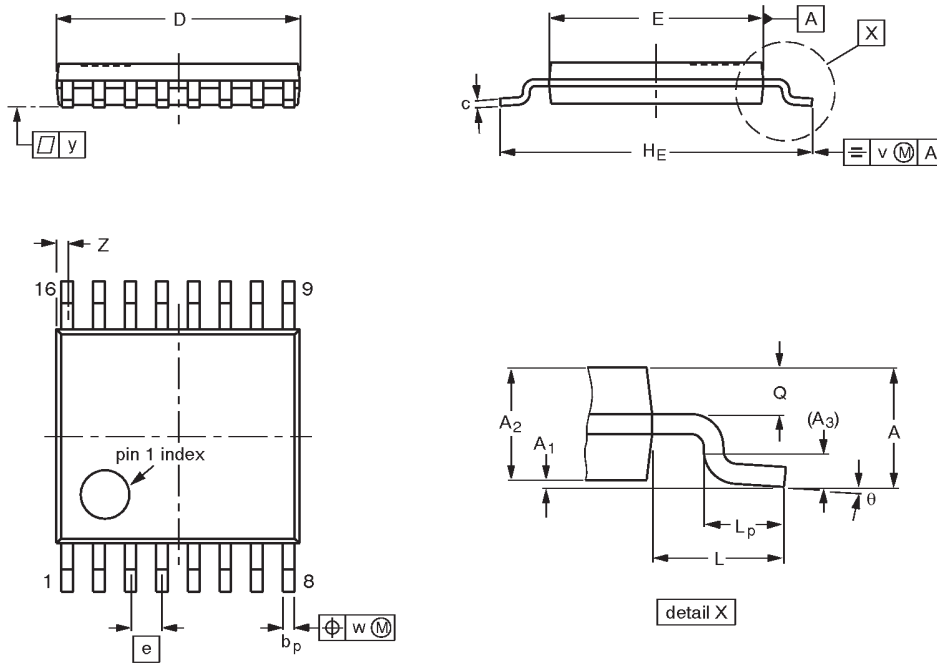
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

Dual 4-channel analog multiplexer/demultiplexer

74LV4052

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				<del>94-07-12</del> 95-04-04

## Dual 4-channel analog multiplexer/demultiplexer

74LV4052

## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
<i>Preliminary Specification</i>	<b>Preproduction Product</b>	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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