

DATA SHEET

74LVT20

3.3V Dual 4-input NAND gate

Product specification

1996 Aug 28

IC24 Data Handbook

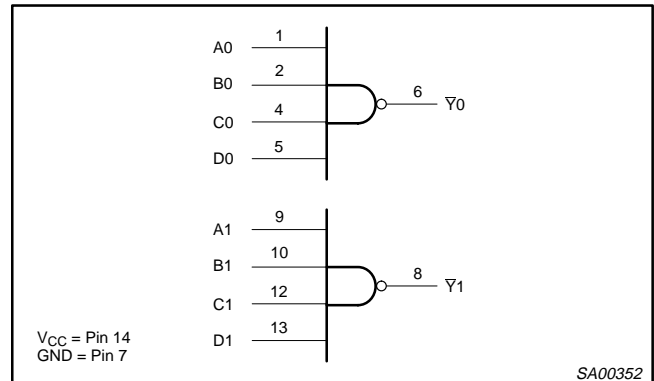
3.3V Dual 4-input NAND gate

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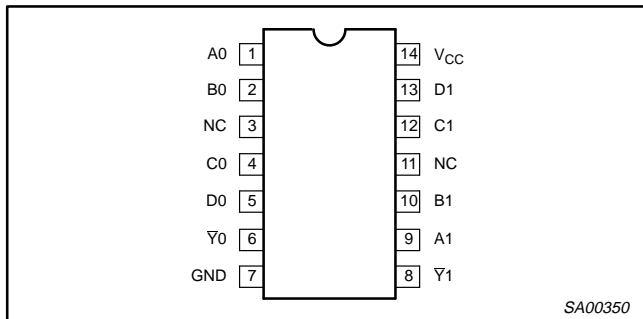
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}\text{C};$ $GND = 0\text{V}$ | TYPICAL | UNIT |
|------------------------|---|--|------------|------|
| t_{PLH} t_{PHL} | Propagation delay An, Bn, Cn, Dn to \bar{Y}_n | $C_L = 50\text{pF};$ $V_{CC} = 3.3\text{V}$ | 3.4 3.2 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or 3.0V | 3 | pF |
| I_{CCL} | Total supply current | Outputs Low; $V_{CC} = 3.6\text{V}$ | 0.5 | mA |

LOGIC DIAGRAM



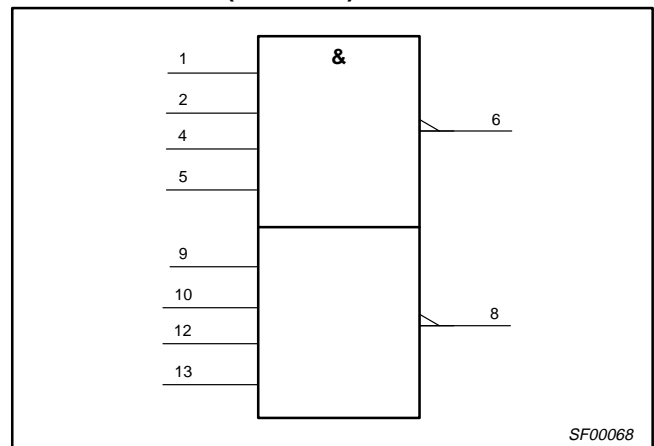
PIN CONFIGURATION



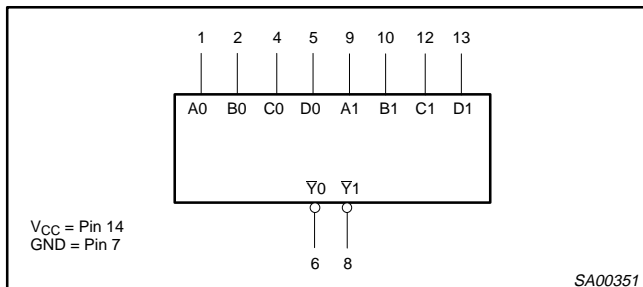
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---------------------------|----------------|-------------------------|
| 1, 2, 4, 5, 9, 10, 12, 13 | An, Bn, Cn, Dn | Data inputs |
| 6, 8 | \bar{Y}_n | Data outputs |
| 7 | GND | Ground (0V) |
| 14 | V_{CC} | Positive supply voltage |

LOGIC SYMBOL (IEEE/IEC)



LOGIC SYMBOL



FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|--------|-----|-----|-----|-------------|
| Dna | Dnb | Dnc | Dnd | \bar{Q}_n |
| L | X | X | X | H |
| X | L | X | X | H |
| X | X | L | X | H |
| X | X | X | L | H |
| H | H | H | H | L |

NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|----------------------|-------------------|-----------------------|---------------|------------|
| 14-Pin Plastic SO | -40°C to +85°C | 74LVT20 D | 74LVT20 D | SOT108-1 |
| 14-Pin Plastic SSOP | -40°C to +85°C | 74LVT20 DB | 74LVT20 DB | SOT337-1 |
| 14-Pin Plastic TSSOP | -40°C to +85°C | 74LVT20 PW | 74LVT20PW DH | SOT402-1 |

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +4.6 | V |
| I _{IK} | DC input diode current | V _I < 0 | -50 | mA |
| V _I | DC input voltage ³ | | -0.5 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | -50 | mA |
| V _{OUT} | DC output voltage ³ | Output in Off or High state | -0.5 to +7.0 | V |
| I _{OUT} | DC output current | Output in High state | -32 | mA |
| | | Output in Low state | 64 | |
| T _{stg} | Storage temperature range | | -65 to 150 | °C |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|------------------|--|--------|-----|------|
| | | MIN | MAX | |
| V _{CC} | DC supply voltage | 2.7 | 3.6 | V |
| V _I | Input voltage | 0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | V |
| V _{IL} | Low-level Input voltage | | 0.8 | V |
| I _{OH} | High-level output current | | -20 | mA |
| I _{OL} | Low-level output current | | 32 | mA |
| | Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz | | 48 | |
| T _{amb} | Operating free-air temperature range | -40 | +85 | °C |

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions
 Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|-----------------|--|--|-----------------------|------------------|------|---------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V_{IK} | Input clamp voltage | $V_{CC} = 2.7V; I_{IK} = -18mA$ | | | -1.2 | V |
| V_{OH} | High-level output voltage | $V_{CC} = 2.7$ to $3.6V; I_{OH} = -100\mu A$ | $V_{CC}-0.2$ | | | V |
| | | $V_{CC} = 2.7V; I_{OH} = -6mA$ | 2.4 | | | |
| | | $V_{CC} = 3.0V; I_{OH} = -20mA$ | 2.0 | | | |
| V_{OL} | Low-level output voltage | $V_{CC} = 2.7V; I_{OL} = 100\mu A$ | 0.2 | | | V |
| | | $V_{CC} = 2.7V; I_{OL} = 24mA$ | 0.5 | | | |
| | | $V_{CC} = 3.0V; I_{OL} = 32mA$ | 0.5 | | | |
| I_I | Input leakage current | $V_{CC} = 0$ or $3.6V; V_I = 5.5V$ | 10 | | | μA |
| | | $V_{CC} = 3.6V; V_I = V_{CC}$ or GND | ± 1 | | | |
| I_{OFF} | Output off current | $V_{CC} = 0V; V_I$ or $V_O = 0$ to $4.5V$ | ± 100 | | | μA |
| I_{CCH} | Quiescent supply current | $V_{CC} = 3.6V; \text{Outputs High, } V_I = \text{GND or } V_{CC}, I_O = 0$ | 0.02 | | | mA |
| I_{CCL} | | $V_{CC} = 3.6V; \text{Outputs Low, } V_I = \text{GND or } V_{CC}, I_O = 0$ | 0.5 | 1.2 | | |
| ΔI_{CC} | Additional supply current per input pin ² | $V_{CC} = 3V$ to $3.6V; \text{One input at } V_{CC}-0.6V, \text{Other inputs at } V_{CC}$ or GND | 0.2 | | | μA |
| C_I | Input capacitance | $V_I = 3V$ or 0 | 3 | | | pF |

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500\Omega; T_{amb} = -40^\circ C$ to $+85^\circ C$.

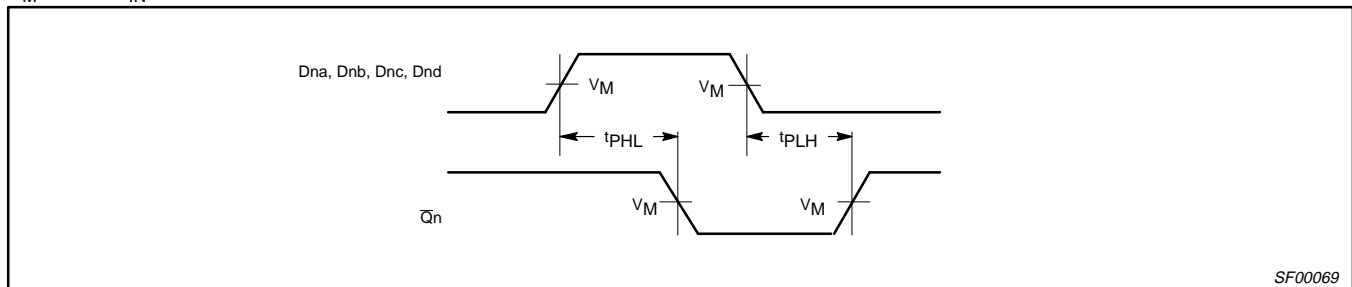
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | UNIT |
|------------------------|--|----------|--------------------------|------------------|------------|-----------------|------|
| | | | $V_{CC} = 3.3V \pm 0.3V$ | | | $V_{CC} = 2.7V$ | |
| | | | MIN | TYP ¹ | MAX | MAX | |
| t_{PLH} t_{PHL} | Propagation delay An, Bn, Cn, Dn to \bar{Y}_n | 1 | 1.0 1.0 | 3.4 3.2 | 5.4 4.4 | 6.4 4.3 | ns |

NOTE:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC WAVEFORMS

$V_M = 1.5V, V_{IN} = \text{GND to } 2.7V$

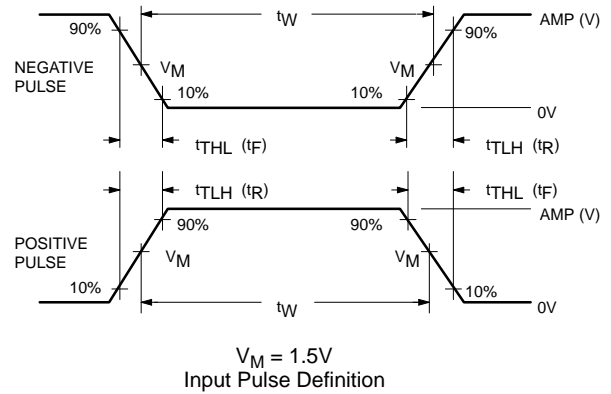
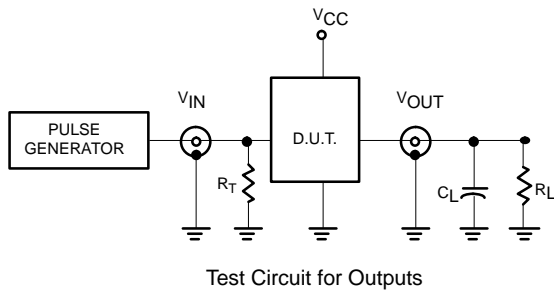


Waveform 1. Propagation Delay for Inverting Outputs

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TEST CIRCUIT AND WAVEFORMS



DEFINITIONS

- R_L = Load resistor; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|--------------|-------|--------------|--------------|
| | Amplitude | Rep. Rate | t_w | t_r | t_f |
| 74LVT | 2.7V | $\leq 10MHz$ | 500ns | $\leq 2.5ns$ | $\leq 2.5ns$ |

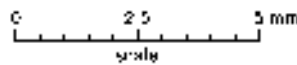
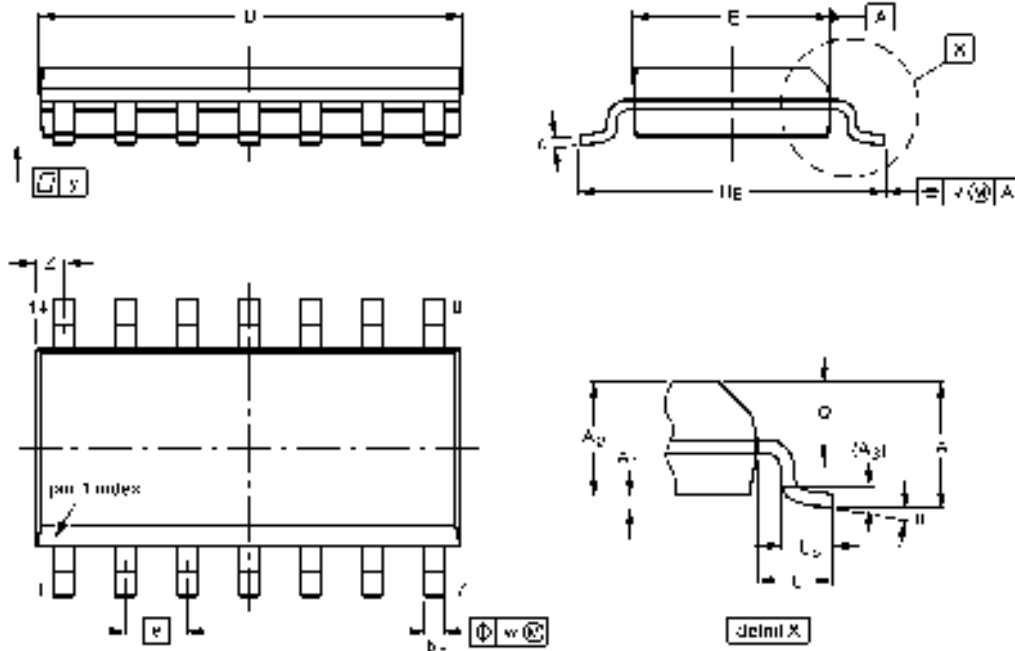
SV00022

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | e | φ ⁽¹⁾ | ε ⁽¹⁾ | φ | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | φ w ⁽²⁾ |
|--------|--------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|--------------------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.20 | 0.45 0.30 | 0.25 0.19 | 0.75 0.50 | 4.0 3.0 | 1.27 | 5.2 5.0 | 1.5 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | φ w ⁽²⁾ |
| inches | 0.069 | 0.0098 0.0039 | 0.057 0.049 | 0.01 | 0.018 0.014 | 0.0099 0.0075 | 0.03 0.02 | 0.16 0.12 | 0.050 | 0.21 0.20 | 0.061 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.029 0.012 | φ w ⁽²⁾ |

Note

1 Plastic or metal protrusions of 0.15 mm maximum per side are not included

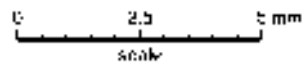
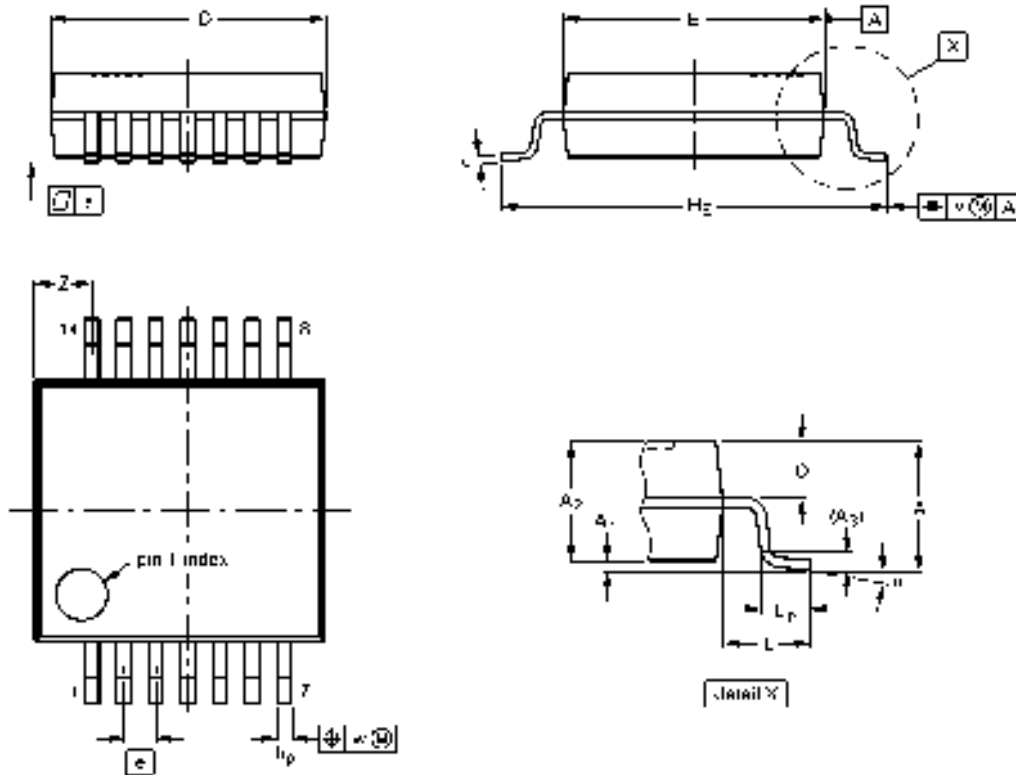
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT108-1 | 076E060 | MS-012AB | | | 5-198-19 95-01-23 |

3.3V Dual 4-input NAND gate

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | Ø ⁽¹⁾ | e ⁽¹⁾ | e | H _E | L | L _p | Ø | γ | w | y | z ⁽¹⁾ | r |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.71 0.75 | 1.80 1.05 | 0.20 | 0.28 0.25 | 0.20 0.09 | 6.4 0.0 | 5.4 5.2 | 0.65 | 7.0 7.8 | 1.25 | 1.03 0.82 | 0.9 0.7 | 0.2 | 0.12 | 0.1 | 1.4 0.9 | 0° 0° |

Note

1 Plastic or metal protrusions of 0.25 mm maximum per side are not included

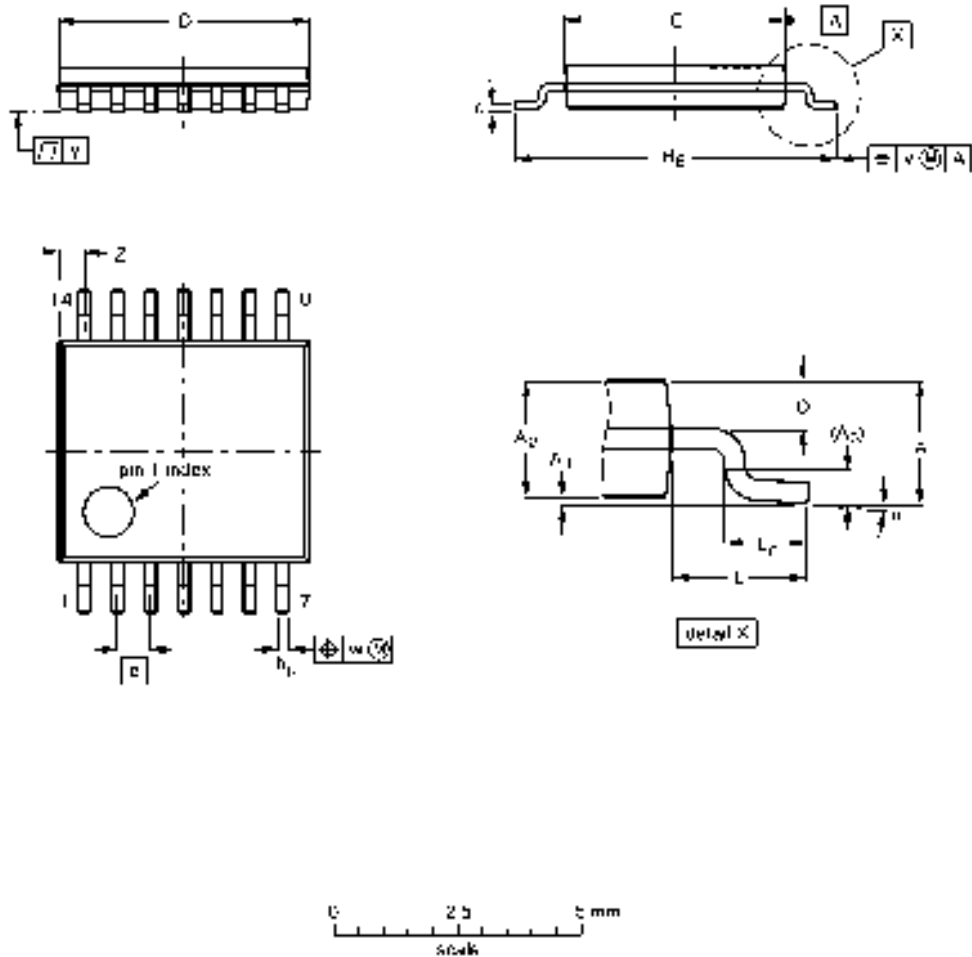
| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT337-1 | | MO-150AB | | | 95-85-94 96-01-19 |

3.3V Dual 4-input NAND gate

74LVT20

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max | A ₁ | A ₂ | A ₃ | b _p | c | Ø(1) | Ø(2) | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | II |
|------|-------|----------------|----------------|----------------|----------------|------------|------------|------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 | 0.15 0.75 | 0.05 0.00 | 0.25 | 0.50 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.55 | 6.6 6.2 | 1.0 | 0.75 0.57 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.20 | 0° 0° |

Notes

- 1 Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2 Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT402-1 | | MO-150 | | | | 94-07-12 95-11-01 |

3.3V Dual 4-input NAND gate

74LVT20

NOTES

3.3V Dual 4-input NAND gate

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DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|-------------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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