INTEGRATED CIRCUITS

DATA SHEET

74ABT162240 74ABTH162240

16-bit inverting buffer/driver with 30Ω series termination resistors

Product specification Supersedes data of 1998 Jan 16 IC23 Data Handbook





16-bit inverting buffer/driver with 30 Ω series termination resistors (3-State)

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FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-32mA
- TTL input and output switching levels
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH162240 incorporates bus hold data inputs which eliminate the need for external pull up resistors to hold unused inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT162240 is a high-performance BiCMOS device which combines low static and dynamic power dissipation with high speed.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-State outputs.

Two options are available, 74ABT162240 which does not have the bus hold feature and 74ABTH162240 which incorporates the bus hold feature.

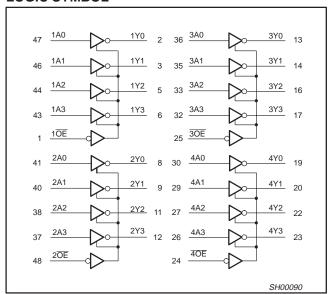
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to n∀x	$C_L = 50pF;$ $V_{CC} =$	2.7 2.6	ns
C _{IN}	Input capacitance nOE	$V_I = 0V \text{ or } 3.0V$	4	pF
C _{OUT}	Output capacitance	Outputs disabled; V _O = 0V or	6	pF
I _{CCZ}	Quiescent supply current	Outputs disabled; V _{CC} =	500	μΑ
I _{CCL}	Quiescent supply current	Outputs low; V _{CC} = 5.5V	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT162240 DL	BT162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT162240 DGG	BT162240 DGG	SOT362-1
48-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH162240 DL	BH162240 DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH162240 DGG	BH162240 DGG	SOT362-1

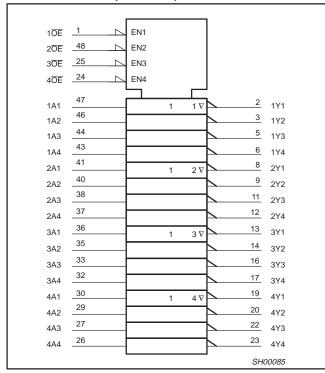
LOGIC SYMBOL



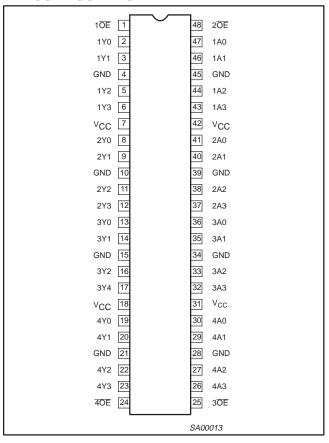
16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



FUNCTION TABLE

Inp	uts	Outputs
nŌĒ	nAx	n₹x
L	L	Н
L	Н	L
Н	Х	Z

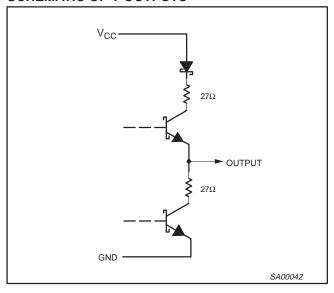
H = High voltage level

L = Low voltage level

X = Don't care

Z = High Impedance "off" state

SCHEMATIC OF Y OUTPUTS



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0-1A3 2A0-2A3 3A0-3A3 4A0-4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Ÿ0-1Ÿ3 2Ÿ0-2Ÿ3 3Ÿ0-3Ÿ3 4Ÿ0-4Ÿ3	Data outputs
1, 48, 25, 24	1 <u>OE</u> , 2 <u>OE</u> , 3 <u>OE</u> , 4 <u>OE</u>	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
VI	DC input voltage ³		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
Vout	DC output voltage ³	Output in Off or High state	-0.5 to +5.5	V
la	DC output current	Output in Low state	128	mA
Гоит	De output current	Output in High state	-64] "''^
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the
device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to
absolute-maximum-rated conditions for extended periods may affect device reliability.

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

CVMDOL	DADAMETED	LIM	LINUT	
SYMBOL	PARAMETER	MIN	MAX	UNIT
V _{CC}	DC supply voltage	4.5	5.5	V
VI	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Input voltage		0.8	V
I _{OH}	High-level output current		-32	mA
I _{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		12	
Δt/Δν	Input transition rise or fall rate; Outputs enabled	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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DC ELECTRICAL CHARACTERISTICS

						LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	S	Ta	_{mb} = +25	°C	T _{amb} =	-40°C 85°C	UNIT
				Min	Тур	Max	Min	Max	1
V _{IK}	Input clamp voltage	$V_{CC} = 4.5V; I_{IK} = -18mA$			-0.9	-1.2		-1.2	V
		$V_{CC} = 4.5V$; $I_{OH} = -3mA$; $V_I = V_{IL}$ or V_{IH}		2.5	2.9		2.5		V
V_{OH}	High-level output voltage	$V_{CC} = 5.0V; I_{OH} = -3mA; V_{I} = V$	_{IL} or V _{IH}	3.0	3.4		3.0		V
		$V_{CC} = 4.5V; I_{OH} = -32mA; V_{I} =$	V _{IL} or V _{IH}	2.0	2.4		2.0		V
Vol	Low-level output voltage	$V_{CC} = 4.5V; I_{OL} = 8mA; V_I = V_{IL}$	or V _{IH}			0.65		0.65	V
VOL	Low-level output voltage	$V_{CC} = 4.5V; I_{OL} = 12mA; V_{I} = V$	_{IL} or V _{IH}			0.80		0.80	V
II	Input leakage current	$V_{CC} = 5.5V$; $V_I = GND \text{ or } 5.5V$			±0.01	±1.0		±1.0	μΑ
	Input leakage current	$V_{CC} = 5.5V$; $V_I = V_{CC}$ or GND	Control pins		±0.01	±1		±1	μА
I _I	74ABTH162240	$V_{CC} = 5.5V$; $V_I = V_{CC}$	Data pins		0.01	1		1	μΑ
		$V_{CC} = 5.5V; V_I = 0$	Data pins		-2	-3		-5	μΑ
	D 1111	$V_{CC} = 4.5V$; $V_I = 0.8V$		50			50		
I_{HOLD}	Bus Hold current A inputs ³ 74ABTH162240	V _{CC} = 4.5V; V _I = 2.0V		-75			-75		μΑ
		$V_{CC} = 5.5V; V_I = 0 \text{ to } 5.5V$		±500					
I _{OFF}	Power-off leakage current	$V_{CC} = 0.0V$; V_O or $V_I \le 4.5V$			±5.0	±100		±100	μΑ
I _{PU} /I _{PD}	Power-up/down 3-State output current	$V_{CC} = 2.0V; V_{O} = 0.5V; V_{I} = GN$ $V_{OE} = V_{CC}$	ID or V _{CC} ;		±5.0	±50		±50	μА
I _{OZH}	3-State output High current	$V_{CC} = 5.5V; V_{O} = 2.7V; V_{I} = V_{IL}$	or V _{IH}		1.0	10		10	μΑ
I _{OZL}	3-State output Low current	$V_{CC} = 5.5V$; $V_{O} = 0.5V$; $V_{I} = V_{IL}$	or V _{IH}		-1.0	-10		-10	μΑ
I _{CEX}	Output high leakage current	$V_{CC} = 5.5V; V_{O} = 5.5V; V_{I} = GN$	ID or V _{CC}		1.0	50		50	μΑ
Io	Output current ¹	$V_{CC} = 5.5V; V_{O} = 2.5V$		-50	-70	-180	-50	-180	mA
I _{CCH}		V_{CC} = 5.5V; Outputs High, V_{I} =	GND or V _{CC}		0.5	1.0		1.0	mA
I _{CCL}	Quiescent supply current	$V_{CC} = 5.5V$; Outputs Low, $V_I = 0$	V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		8	19		19	mA
I _{CCZ}	Quiocociii suppi) suii siii	V_{CC} = 5.5V; Outputs 3-State; V _I = GND or V_{CC}			0.5	1.0		1.0	mA
Δl _{CC}	Additional supply current per input pin ² 74ABT162240	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V			10	200		200	μΑ
Δl _{CC}	Additional supply current per input pin ² 74ABTH162240	Outputs enabled, one input at 3 inputs at V _{CC} or GND; V _{CC} = 5.			0.2	1.0		1.0	mA

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
 This is the increase in supply current for each input at 3.4V.
- 3. This is the bus hold overdrive current required to force the input to the opposite logic state.

16-bit inverting buffer/driver with 30Ω series termination resistors (3-State)

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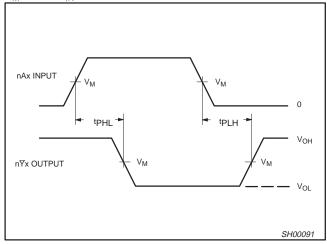
AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500 Ω ; T_{amb} = -40°C to +85°C.

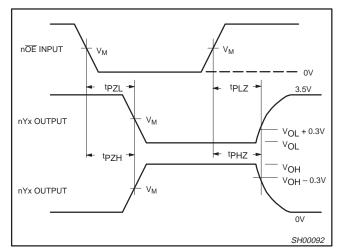
					LIMIT	rs		
SYMBOL	PARAMETER	WAVEFORM	T _a	_{amb} = +25° CC = +5.0°	C V	T _{amb} = -40° V _{CC} = +5	UNIT	
			Min	Тур	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 1.0	2.7 2.6	3.8 3.2	1.0 1.0	4.2 3.7	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.2 1.0	2.3 2.9	3.2 3.8	1.2 1.0	4.0 4.7	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.6 1.4	3.0 2.8	4.1 3.8	1.6 1.4	4.7 4.0	ns

AC WAVEFORMS

 $V_{M} = 1.5V$, $V_{IN} = GND$ to 2.7V



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



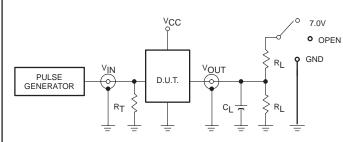
Waveform 2. 3-State Output Enable and Disable Times

1998 Feb 25 7

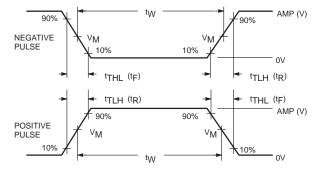
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TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	7V
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

 $C_L = Load$ capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

EAMILY	IN	INPUT PULSE REQUIREMENTS							
FAMILY	Amplitude	Rep. Rate	t _W	t _R	t _F				
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns				

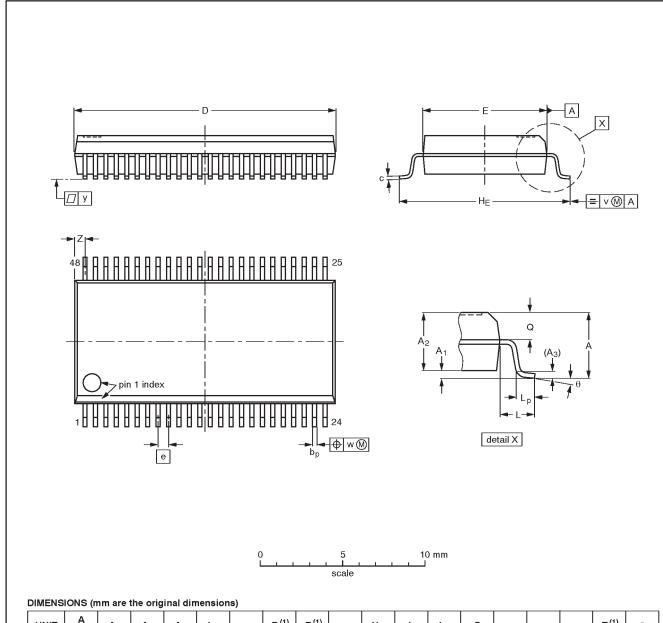
SH00093

16-bit inverting buffer/driver with 30Ω Series Termination Resistors (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



UNIT	A max.	Α1	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

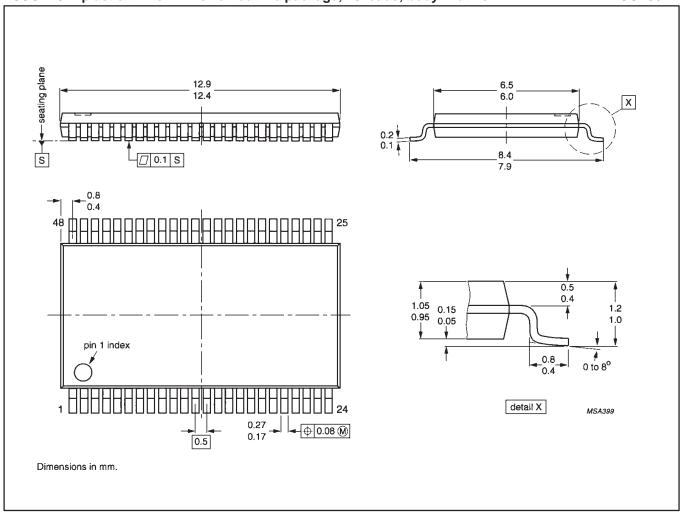
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT370-1		MO-118AA			93-11-02 95-02-04

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TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



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16-bit inverting buffer/driver with 30Ω Series Termination Resistors (3-State)

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NOTES

16-bit inverting buffer/driver with 30 Ω series termination resistors (3-State)

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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^[1] Please consult the most recently issued datasheet before initiating or completing a design.

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