DATA SHEET

74ABT16543
74ABTH16543
16-bit latched transceivers with dual enable (3-State)

Product specification
Supersedes data of 1995 Aug 17
IC23 Data Handbook

1998 Feb 27

Philips
Semiconductors

PHILIPS

16-bit latched transceivers with dual enable (3-State)

74ABT16543
74ABTH16543

FEATURES

- Two 8-bit octal transceivers with D-type latch
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 74ABTH16543 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- See 74ABT161543 for same function with Master Reset control pins

DESCRIPTION

The 74ABT16543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable (n$\overline{\text{LEAB}}$, n$\overline{\text{LEBA}}$) and Output Enable (n$\overline{\text{OEAB}}$, n$\overline{\text{OEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64mA.

Two options are available, 74ABT16543 which does not have the bus-hold feature and 74ABTH16543 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nAx to nBx	C_L = 50pF; V_{CC} = 5V	2.5 2.2	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3	pF
$C_{I/O}$	I/O capacitance	V_O = 0V or $V_{CC;}$ 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5V	550	µA
I_{CCL}		Outputs low; V_{CC} = 5.5V	9	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABT16543 DL	BT16543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABT16543 DGG	BT16543 DGG	SOT364-1
56-Pin Plastic SSOP Type III	–40°C to +85°C	74ABTH16543 DL	BH16543 DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40°C to +85°C	74ABTH16543 DGG	BH16543 DGG	SOT364-1

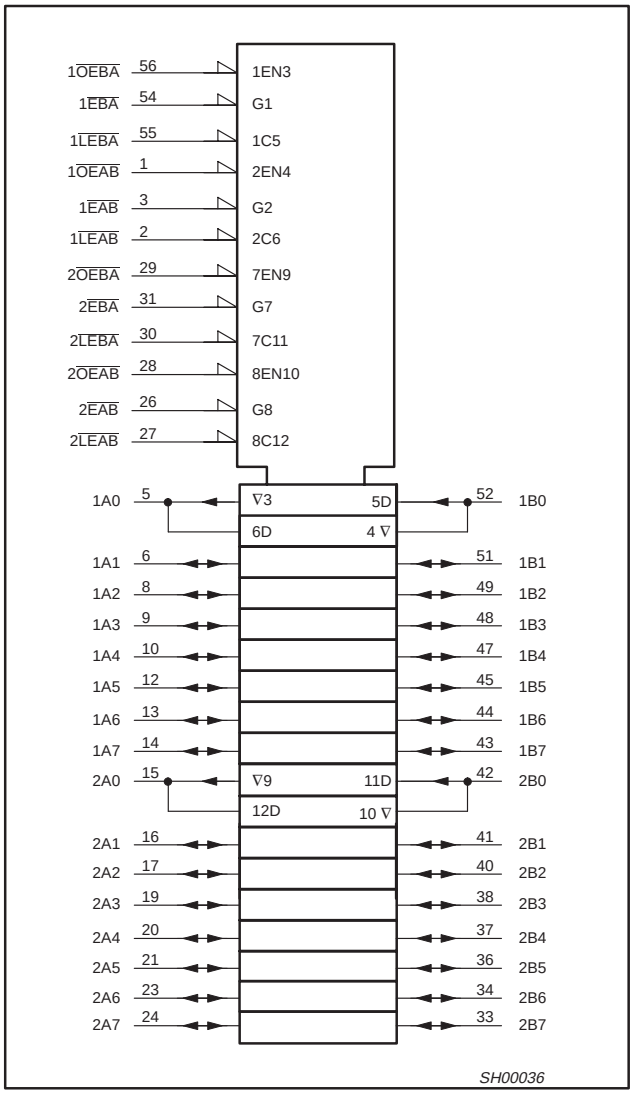
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs
1, 56 28, 29	1$\overline{\text{OEAB}}$, 1$\overline{\text{OEBA}}$, 2$\overline{\text{OEAB}}$, 2$\overline{\text{OEBA}}$	A to B / B to A Output Enable inputs (active-Low)
3, 54 26, 31	1$\overline{\text{EAB}}$, 1$\overline{\text{EBA}}$, 2$\overline{\text{EAB}}$, 2$\overline{\text{EBA}}$	A to B / B to A Enable inputs (active-Low)
2, 55 27, 30	1$\overline{\text{LEAB}}$, 1$\overline{\text{LEBA}}$, 2$\overline{\text{LEAB}}$, 2$\overline{\text{LEBA}}$	A to B / B to A Latch Enable inputs (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

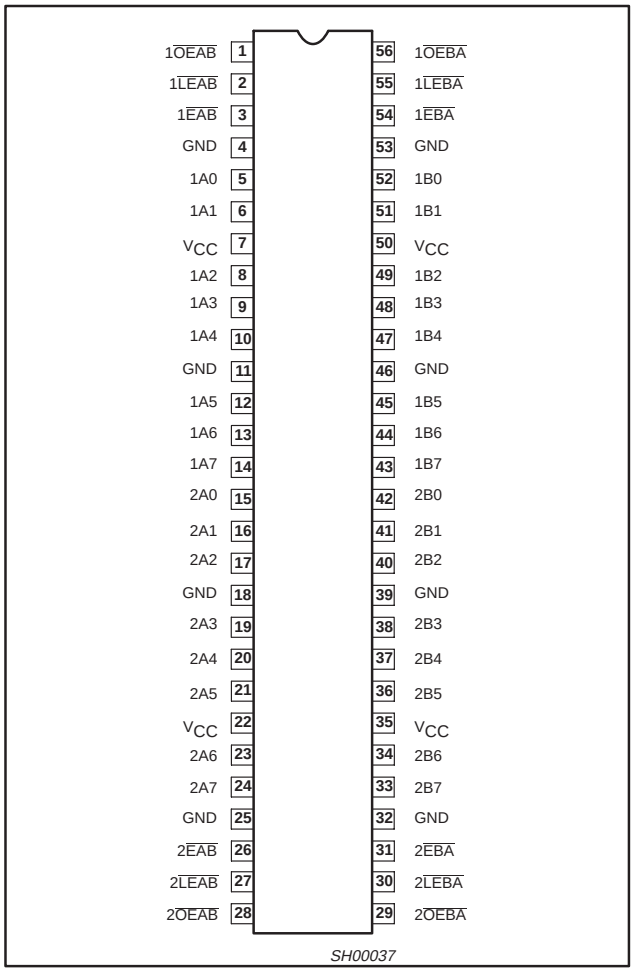
16-bit latched transceivers with dual enable (3-State)

74ABT16543
74ABTH16543

LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



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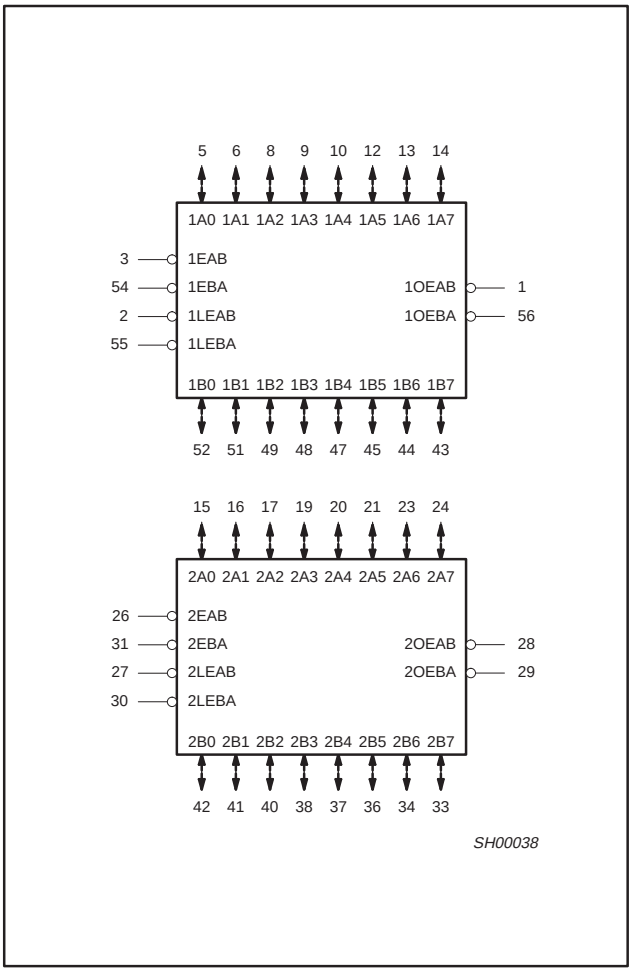


FUNCTIONAL DESCRIPTION

The 74ABT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable ($n\overline{EAB}$) input and the A-to-B Latch Enable ($n\overline{LEAB}$) input are Low the A-to-B path is transparent.

A subsequent Low-to-High transition of the $n\overline{LEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{EAB}$ and $n\overline{OEAB}$ both Low, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

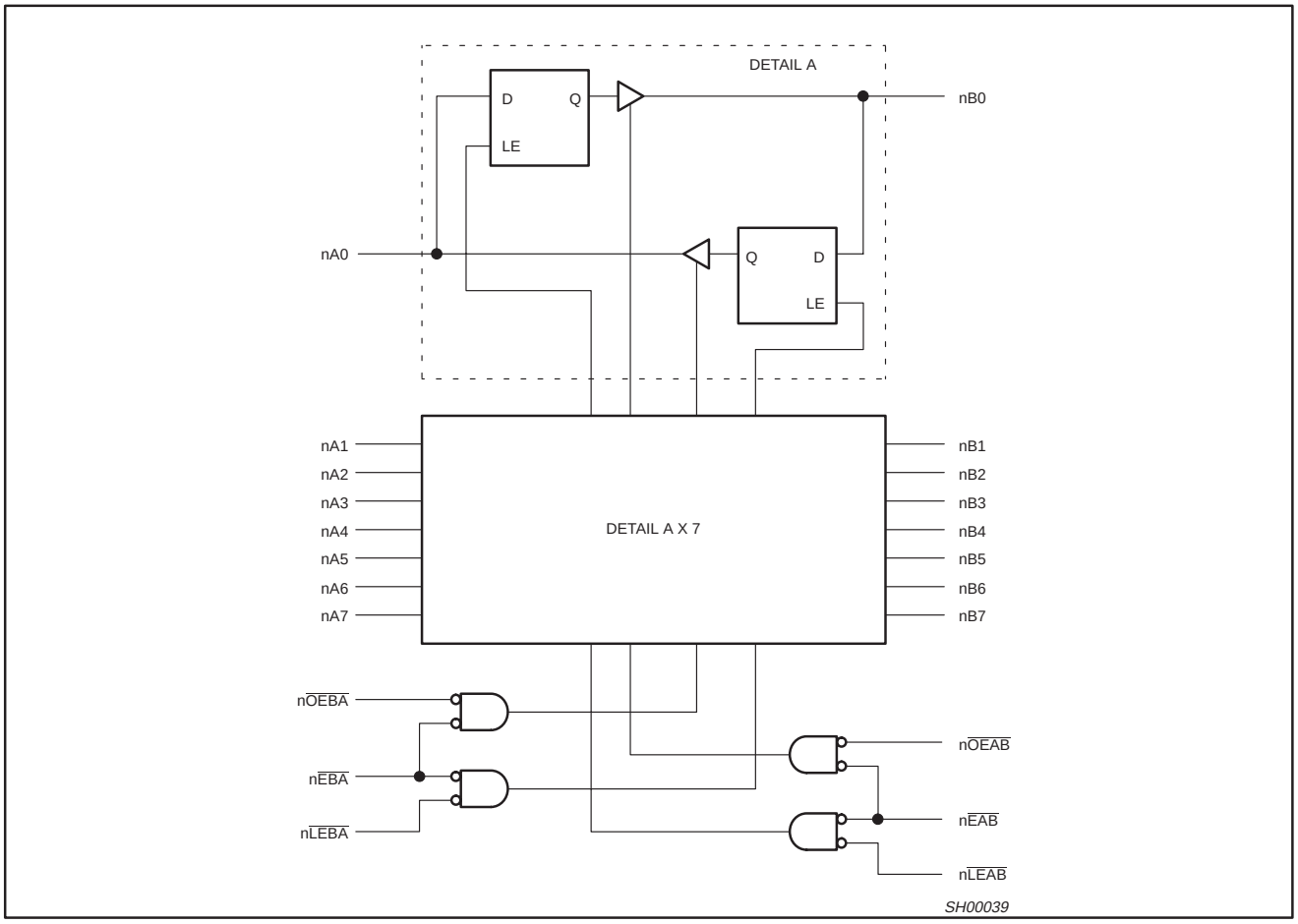
Control of data flow from B to A is similar, but using the $n\overline{EBA}$, $n\overline{LEBA}$, and $n\overline{OEBA}$ inputs.

FUNCTION TABLE

INPUTS				OUTPUTS	STATUS
$n\overline{OEXX}$	$n\overline{EXX}$	$n\overline{LEXX}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	H L	Latch + Display
L L	L L	L L	H L	H L	Transparent
L	L	H	X	NC	Hold

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
X = Don't care
↑ = Low-to-High transition of $n\overline{LEXX}$ or $n\overline{EXX}$ (XX = AB or BA)
NC = No change
Z = High impedance or "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
		output in High state	–64	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = –18mA			–1.2		–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	2.9		2.5		V
		V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	3.4		3.0		V
		V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.36	0.55		0.55	V
V_{RST}	Power-up output voltage[3]	V_{CC} = 5.5V; I_O = 1mA; V_I = GND or V_{CC}		0.13	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V (Control pins)		±0.01	±1.0		±1.0	µA
I_{HOLD}	Bus Hold current A or B Ports[5] 74ABTH16543	V_{CC} = 4.5V; V_I = 0.8V	35			35		µA
		V_{CC} = 4.5V; V_I = 2.0V	–75			–75		
		V_{CC} = 5.5V; V_I = 0 to 5.5V	±800					
I_{OFF}	Power-off leakage current	V_{CC} = 0.0V; V_O or $V_I \leq$ 4.5V		± 2.0	±100		±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1V; V_O = 0.0V or V_{CC}; V_I = GND or V_{CC}; V_{OE} = Don't care		± 1.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 5.5V; V_I = V_{IL} or V_{IH}		1.0	10		10	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.0V; V_I = V_{IL} or V_{IH}		–1.0	–10		–10	µA
I_{CEX}	Output High leakage current	V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		1.0	50		50	µA
I_O	Output current[1]	V_{CC} = 5.5V; V_O = 2.5V	–50	–100	–200	–50	–200	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.55	2		2	mA
I_{CCL}		V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		9	19		19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}		0.55	2		2	mA
ΔI_{CC}	Additional supply current per input pin[2] 74ABT16543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		5.0	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2] 74ABTH16543	V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND		200	500		500	µA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
5. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay nAx to nBx, nBx to nAx	2	1.0 1.0	2.5 2.2	3.3 4.4	1.0 1.0	3.8 5.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to nAx, $\overline{LEAB}$ to nBx	1, 2	1.0 1.2	3.1 3.0	4.3 4.8	1.0 1.2	5.2 5.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.0 1.1	3.3 3.3	4.3 5.9	1.0 1.1	5.2 7.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to nAx, $\overline{OEAB}$ to nBx	4 5	1.9 1.6	3.5 2.6	5.0 4.2	1.9 1.6	5.7 4.6	ns
t_{PZH} t_{PZL}	Output enable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	1.0 1.2	3.4 3.4	4.9 6.5	1.0 1.2	6.2 7.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{EBA}$ to nAx, $\overline{EAB}$ to nBx	4 5	2.0 1.7	3.4 2.6	5.6 5.1	2.0 1.7	6.6 5.4	ns

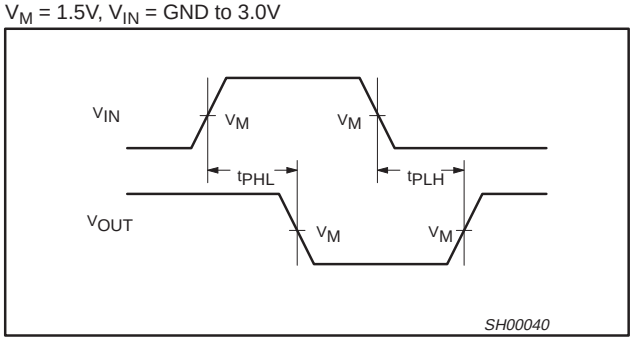
AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F$ = 2.5ns, C_L = 50pF, R_L = 500Ω

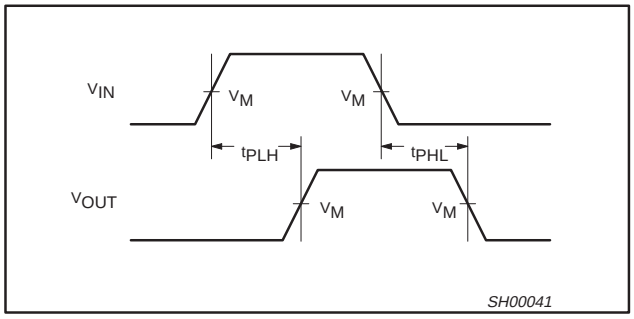
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V		T_{amb} = –40 to +85°C, V_{CC} = +5.0V ±0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Setup time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 3.5	0.4 –0.1	1.5 3.5	ns
t_h(H) t_h(L)	Hold time nAx to $\overline{LEAB}$, nBx to $\overline{LEBA}$	3	1.5 2.0	0.2 –0.3	1.5 2.0	ns
t_s(H) t_s(L)	Setup time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 3.5	0.2 –0.3	1.5 3.5	ns
t_h(H) t_h(L)	Hold time nAx to $\overline{EAB}$, nBx to $\overline{EBA}$	3	1.5 2.0	0.3 –0.2	1.5 2.0	ns
t_w(L)	Latch enable pulse width, Low	3	4.0	3.1	4.0	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



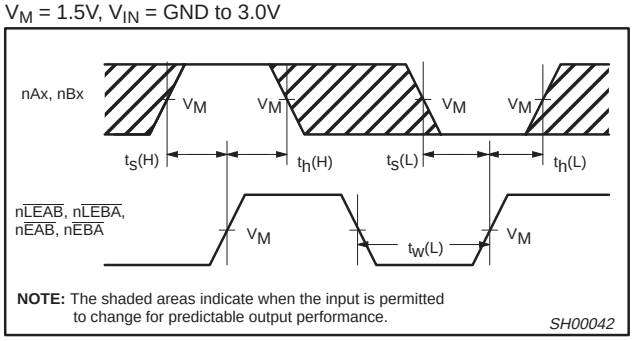
Waveform 1. Propagation Delay For Inverting Output



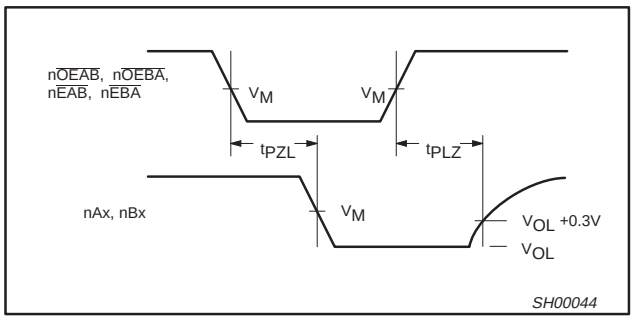
Waveform 2. Propagation Delay For Non-Inverting Output

AC WAVEFORMS (Continued)

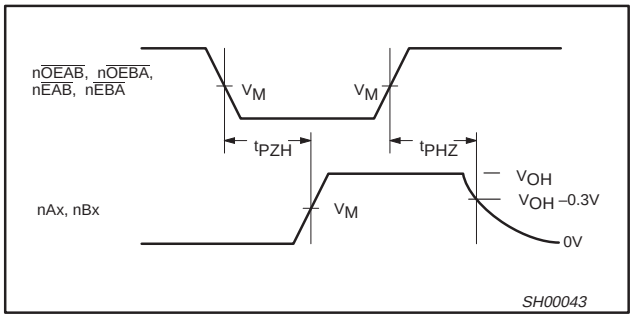
V_M = 1.5V, V_{IN} = GND to 3.0V



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width

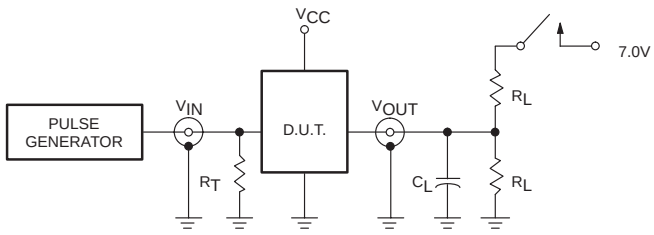


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

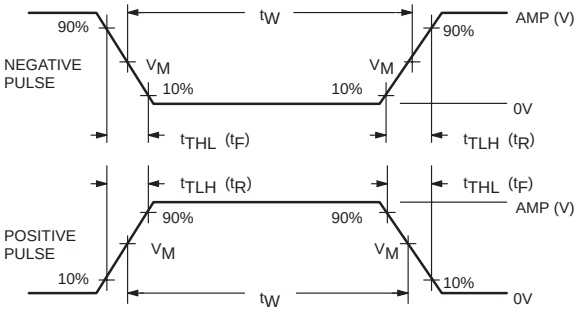


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

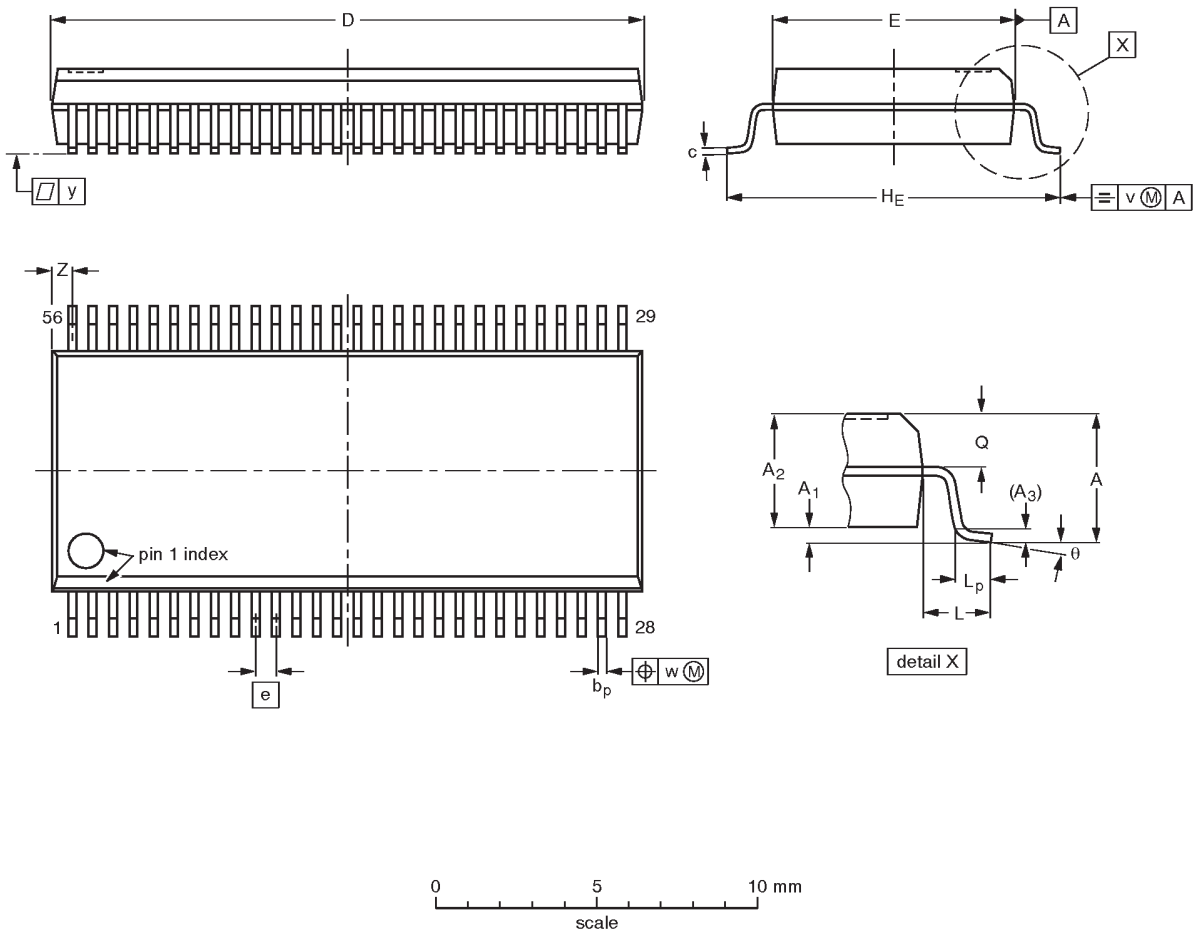
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00018

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

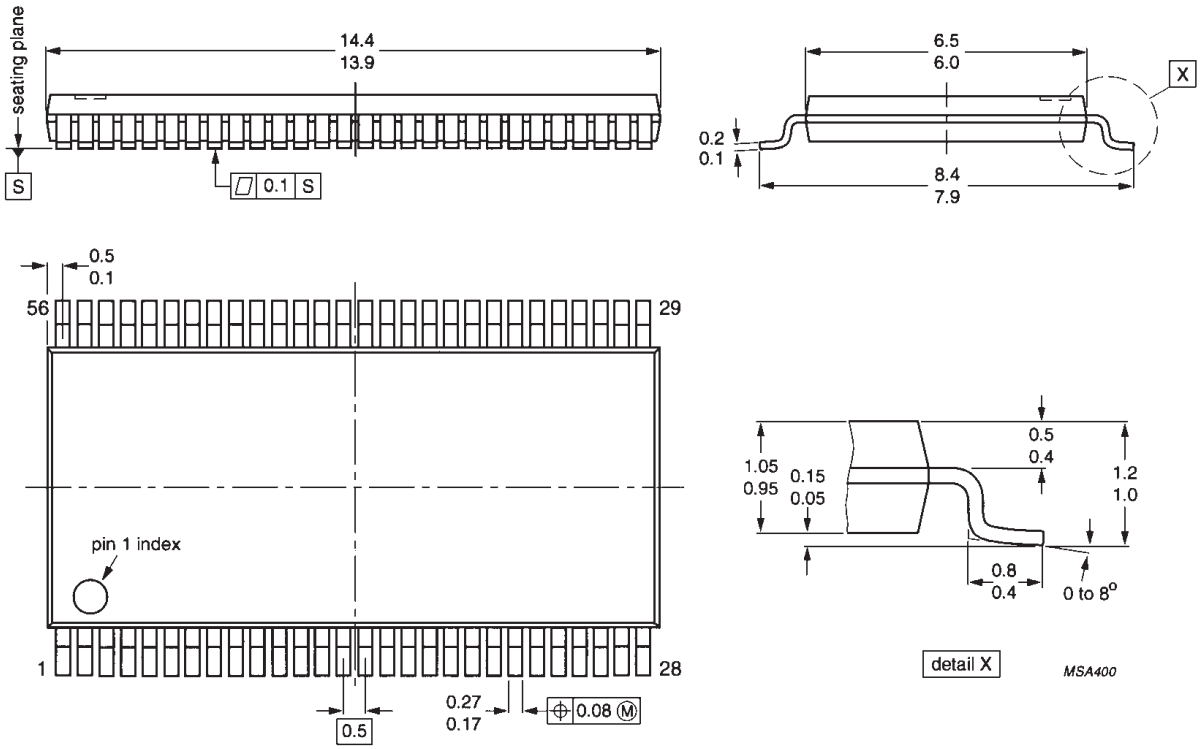
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



Dimensions in mm.

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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