# DATA SHEET

## 74F173
## Quad D-type flip-flop (3-State)

Product specification

1990 Aug 31

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

# Quad D-type flip–flop (3-State) 74F173

## FEATURES

- Edge–triggered D–type register
- Gated clock enable for hold ”do nothing” mode
- 3–state output buffers
- Gated output enable control
- Speed upgrade of N8T10 and current sink upgrade
- Controlled output edges to minimize ground bounces
- 48mA sinking capability

## DESCRIPTION

The 74F173 is a high speed 4–bit parallel load register with clock enable control, 3–state buffered outputs, and master reset (MR). When the two clock enable ($\overline{E}0$ and $\overline{E}1$) inputs are low, the data on the D inputs is loaded into the register simultaneously with low–to–high clock (CP) transition. When one or both enable inputs are high one setup time before the low–to–high clock transition, the register retains the previous data.

Data inputs and clock enable inputs are fully edge–triggered and must be stable only one setup time before the low–to–high clock transition.

The master reset (MR) is an active–high asynchronous input. When the MR is high, all four flip–flops are reset (cleared) independently of any other input condition.

The 3–state output buffers are controlled by a 2–input NOR gate. When both output enable ($\overline{OE}0$ and $\overline{OE}1$) inputs are low, the data in the register is presented at the Q output.

When one or both $\overline{OE}$ inputs are high, the outputs are forced to a high impedance ”off” state.

The 3–state output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

| TYPE | TYPICAL $f_{max}$ | TYPICAL SUPPLY CURRENT (TOTAL) |
|---|---|---|
| 74F173 | 125MHz | 23mA |

## ORDERING INFORMATION

| DESCRIPTION | ORDER CODE<br>COMMERCIAL RANGE<br>$V_{CC}$ = 5V ±10%, $T_{amb}$ = 0°C to +70°C | PKG DWG # |
|---|---|---|
| 16–pin plastic DIP | N74F173N | SOT38-4 |
| 16–pin plastic SO | N74F173D | SOT109-1 |

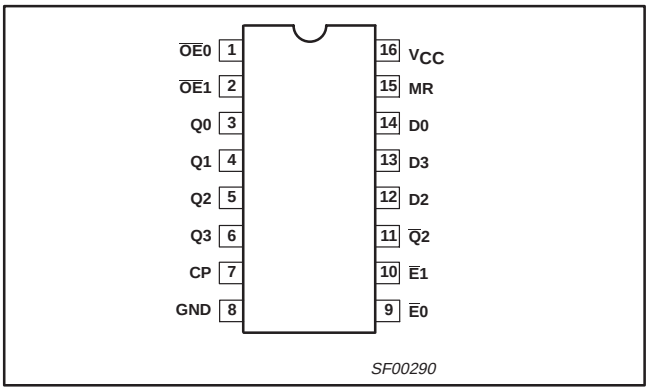
## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

| PINS | DESCRIPTION | 74F (U.L.) HIGH/ LOW | LOAD VALUE HIGH/LOW |
|---|---|---|---|
| D0 – D3 | Data inputs | 1.0/1.0 | 20µA/0.6mA |
| CP | Clock input | 1.0/1.0 | 20µA/0.6mA |
| $\overline{E}0$, $\overline{E}1$ | Clock enable inputs | 1.0/1.0 | 20µA/0.6mA |
| MR | Master reset input | 1.0/1.0 | 20µA/0.6mA |
| $\overline{OE}0$, $\overline{OE}1$ | Output enable inputs | 1.0/1.0 | 20µA/0.6mA |
| Q0 – Q3 | Data outputs | 750/80 | 15mA/48mA |

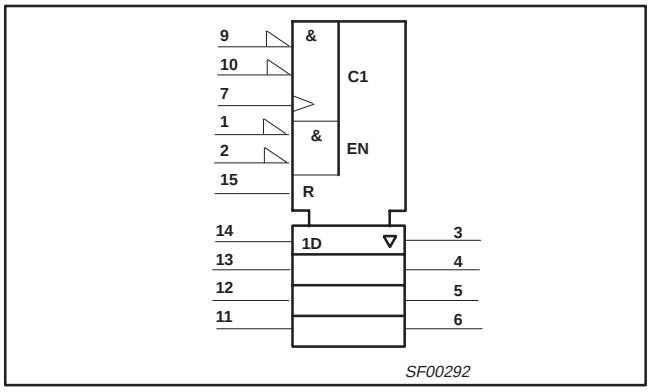
**Note to input and output loading and fan out table**

1. One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

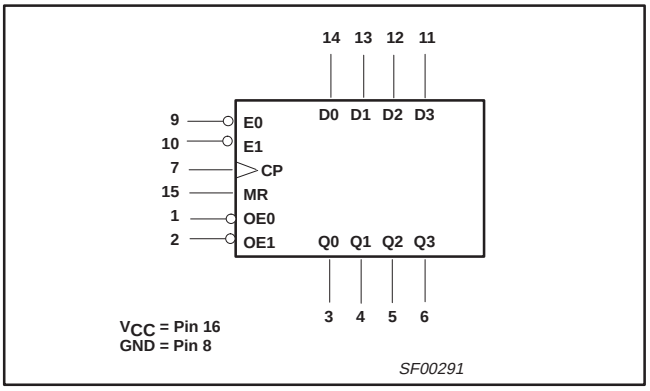
## PIN CONFIGURATION




## IEC/IEEE SYMBOL




## LOGIC SYMBOL




## FUNCTION TABLE

| INPUTS | | | | | OUTPUTS | OUTPUTS |
|---|---|---|---|---|---|---|
| MR | CP | $\overline{E}0$ | $\overline{E}1$ | Dn | Qn (register) | |
| H | X | X | X | X | L | Reset (clear) |
| L | ↑ | l | l | l | L | Parallel load |
| L | ↑ | l | l | h | H | |
| L | X | h | X | X | qn | Hold (do nothing) |
| L | X | X | h | X | qn | |

**Notes to function table**

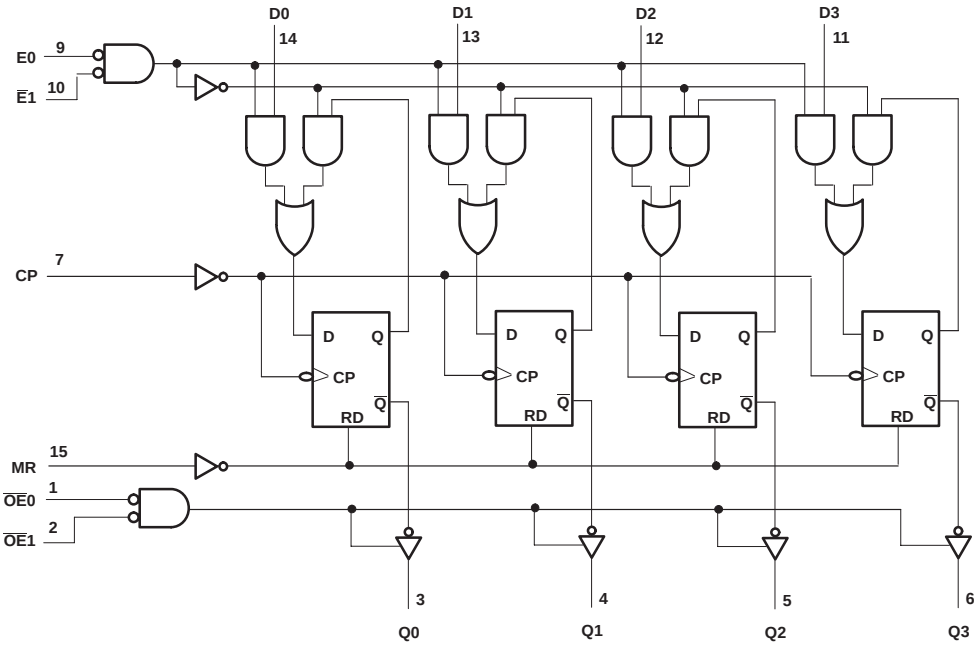
H = High–voltage level
h = High state one setup time before the low–to–high clock transition
L = Low–voltage level
l = Low state one setup time before the low–to–high clock transition
qn = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the low–to–high clock transition
X = Don't care
↑ = Low–to–high clock transition

## FUNCTION TABLE

| INPUTS | | | OUTPUTS | OUTPUTS |
|---|---|---|---|---|
| Qn (register) | $\overline{OE}0$ | $\overline{OE}1$ | Qn | |
| L | L | L | L | Read |
| H | L | L | H | |
| X | H | X | Z | Disabled |
| X | X | H | Z | |

**Notes to function table**
H = High–voltage level
L = Low–voltage level
X = Don't care
Z = High impedance "off" state

## LOGIC DIAGRAM




$V_{CC}$ = Pin 16
GND = Pin 8

SF00293

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{CC}$ | Supply voltage | –0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | –0.5 to +7.0 | V |
| $I_{IN}$ | Input current | –30 to +5 | mA |
| $V_{OUT}$ | Voltage applied to output in high output state | –0.5 to $V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in low output state | 96 | mA |
| $T_{amb}$ | Operating free air temperature range | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature range | –65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High–level input voltage | 2.0 | | | V |
| $V_{IL}$ | Low–level input voltage | | | 0.8 | V |
| $I_{Ik}$ | Input clamp current | | | –18 | mA |
| $I_{OH}$ | High–level output current | | | –15 | mA |
| $I_{OL}$ | Low–level output current | | | 48 | mA |
| $T_{amb}$ | Operating free air temperature range | 0 | | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS[1] | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP[2] | MAX | |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, | ±10%$V_{CC}$ | 2.4 | | | V |
| | | | $V_{IH}$ = MIN, $I_{OH}$ = MAX | ±5%$V_{CC}$ | 2.7 | 3.4 | | V |
| | | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, | ±10%$V_{CC}$ | 2.0 | | | V |
| | | | $V_{IH}$ = MIN, $I_{OH}$ = –15mA | ±5%$V_{CC}$ | 2.0 | 3.1 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, | ±10%$V_{CC}$ | | 0.35 | 0.50 | V |
| | | | $V_{IH}$ = MIN, $I_{OL}$ = MAX | ±5%$V_{CC}$ | | 0.35 | 0.50 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | –0.73 | -1.2 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 7.0V | | | | 100 | µA |
| $I_{IH}$ | High–level input current | | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | | 20 | µA |
| $I_{IL}$ | Low–level input current | | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | | –0.6 | mA |
| $I_{OZH}$ | Off–state output current, high–level voltage applied | | $V_{CC}$ = MAX, $V_O$ = 2.7V | | | | 50 | µA |
| $I_{OZL}$ | Off–state output current, low–level voltage applied | | $V_{CC}$ = MAX, $V_O$ = 0.5V | | | | –50 | µA |
| $I_{OS}$ | Short–circuit output current3 | | $V_{CC}$ = MAX | | -60 | | -150 | mA |
| $I_{CC}$ | Supply current (total) | $I_{CCH}$ | $V_{CC}$ = MAX | | | 19 | 26 | mA |
| | | $I_{CCL}$ | | | | 27 | 37 | mA |
| | | $I_{CCZ}$ | | | | 23 | 32 | mA |

**Notes to DC electrical characteristics**

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_{amb}$ = 25°C.
3. Not more than one output should be shorted at a time. For testing $I_{OS}$, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

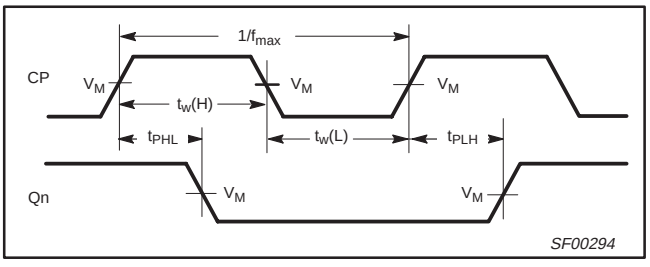
## AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C<br>$V_{CC}$ = +5.0V<br>$C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = 0°C to +70°C<br>$V_{CC}$ = +5.0V ± 10%<br>$C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | Maximum clock frequency | Waveform 1 | 100 | 125 | | 90 | | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>CP to Qn | Waveform 1 | 4.5<br>6.0 | 6.5<br>8.0 | 9.0<br>10.5 | 4.0<br>5.5 | 10.0<br>11.5 | ns |
| $t_{PHL}$ | Propagation delay<br>MR to Qn | Waveform 2 | 6.5 | 8.5 | 11.5 | 6.0 | 12.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time<br>to high or low level | Waveform 4<br>Waveform 5 | 3.5<br>5.5 | 5.0<br>7.0 | 8.0<br>10.0 | 2.5<br>4.5 | 8.5<br>11.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time<br>from high or low level | Waveform 4<br>Waveform 5 | 1.5<br>3.0 | 3.5<br>5.0 | 7.0<br>8.5 | 1.0<br>2.5 | 8.0<br>9.0 | ns |
| $t_{THL}$<br>$t_{TLH}$ | Transition time<br>10% to 90%, 90% to 10% | Waveform 5<br>Waveform 4 | 2.0<br>4.0 | 5.0<br>7.5 | 8.0<br>10.0 | 2.0<br>4.0 | 8.5<br>11.0 | ns |

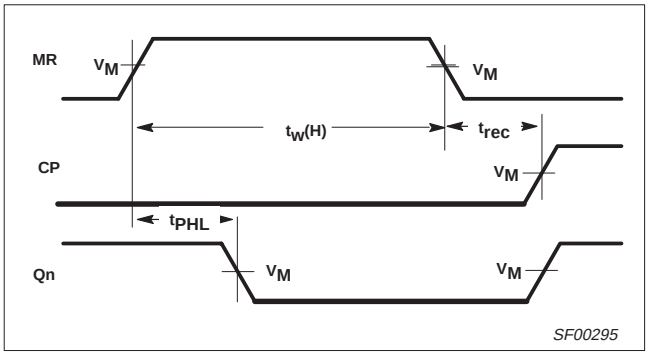
## AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C<br>$V_{CC}$ = +5.0V<br>$C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = 0°C to +70°C<br>$V_{CC}$ = +5.0V ± 10%<br>$C_L$= 50pF, $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{su}$ (H)<br>$t_{su}$ (L) | Setup time, high or low level<br>Dn to CP | Waveform 3 | 2.5<br>2.5 | | | 3.0<br>4.0 | | ns |
| $t_h$ (H)<br>$t_h$ (L) | Hold time, high or low level<br>Dn to CP | Waveform 3 | 0<br>0 | | | 0<br>0 | | ns |
| $t_{su}$ (H)<br>$t_{su}$ (L) | Setup time, high or low level<br>$\overline{E}$ to CP | Waveform 3 | 4.5<br>7.5 | | | 5.0<br>8.5 | | ns |
| $t_h$ (H)<br>$t_h$ (L) | Hold time, high or low level<br>$\overline{E}$ to CP | Waveform 3 | 0<br>0 | | | 0<br>0 | | ns |
| $t_w$ (H)<br>$t_w$ (L) | CP Pulse width,<br>high or low | Waveform 1 | 3.0<br>6.0 | | | 3.0<br>6.0 | | ns |
| $t_w$ (H) | MR Pulse width, high | Waveform 2 | 3.5 | | | 3.5 | | ns |
| $t_{rec}$ | Recovery time, MR to CP | Waveform 2 | 4.5 | | | 5.5 | | ns |

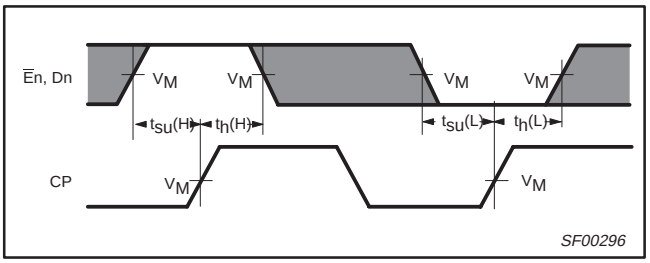
## AC WAVEFORMS



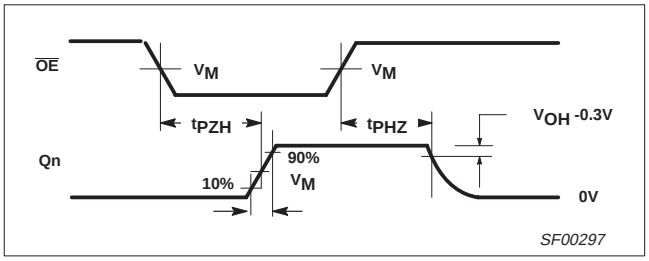

**Waveform 1. Propagation delay for clock input to output, clock pulse widths, and maximum clock frequency**



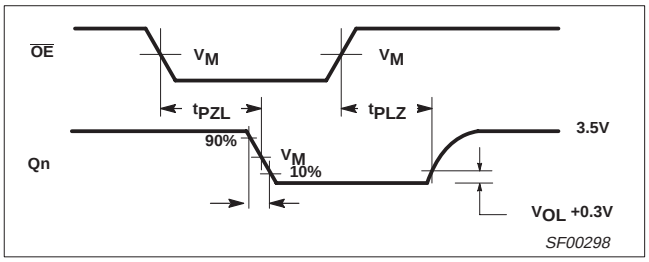

**Waveform 2. Master reset pulse width, master reset to output delay and master reset to clock recovery time**




**Waveform 3. Data and enable setup time and hold times**



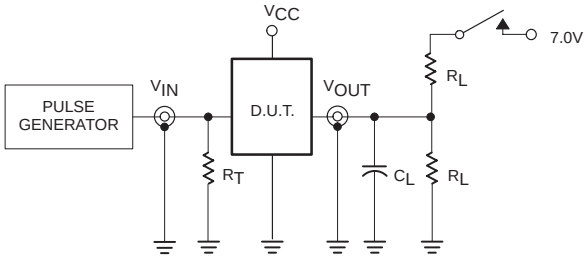

**Waveform 4. 3-state output enable time to high level, output disable time from high level and transition time to high level**




**Waveform 5. 3-state output enable time to low level, output disable time from low level and transition time to low level**

**Notes to AC waveforms**
1. For all waveforms, $V_M$ = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

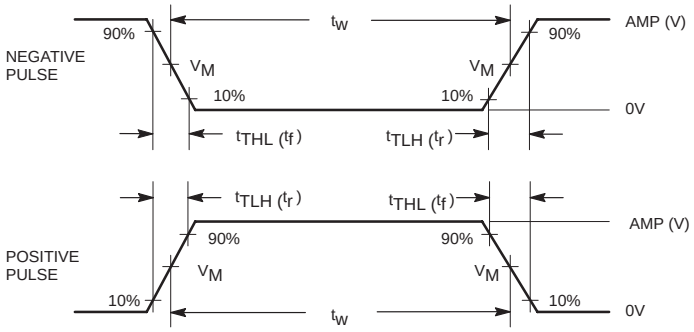
## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for Open Collector Outputs**

**SWITCH POSITION**

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open |



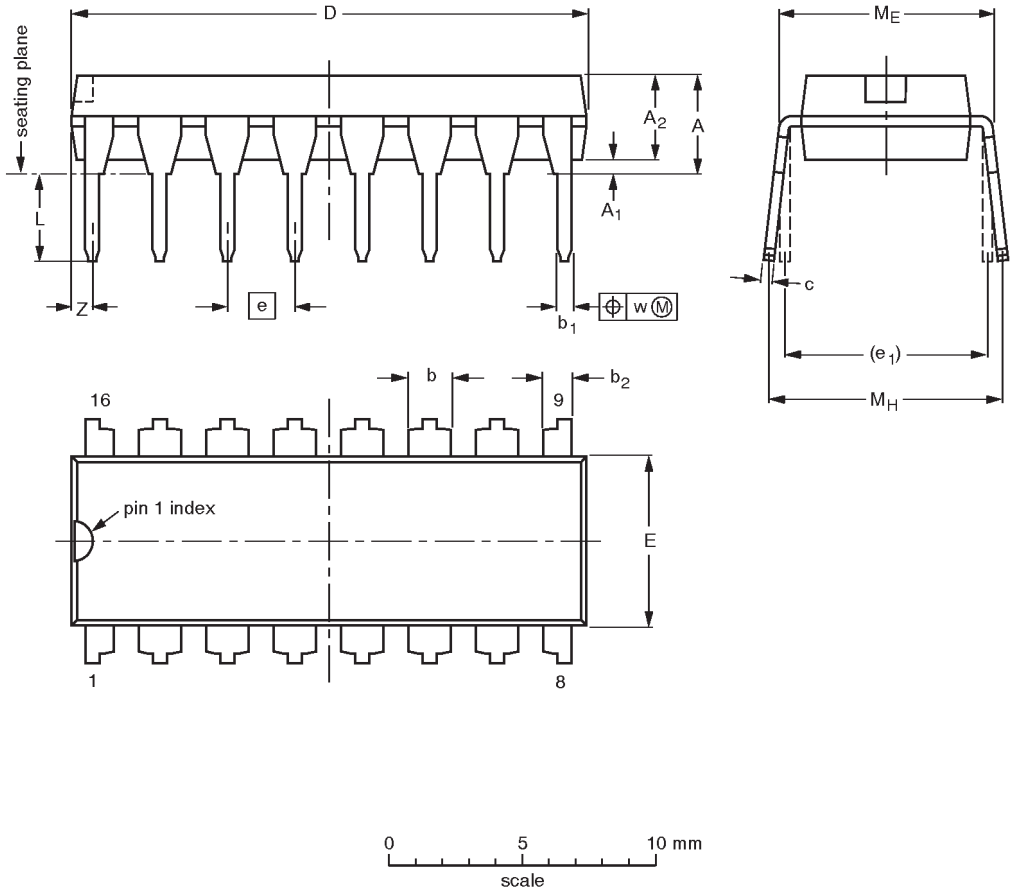

**Input Pulse Definition**

**DEFINITIONS:**
$R_L$ = Load resistor; see AC electrical characteristics for value.
$C_L$ = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

| family | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | amplitude | $V_M$ | rep. rate | $t_w$ | $t_{TLH}$ | $t_{THL}$ |
| 74F | 3.0V | 1.5V | 1MHz | 500ns | 2.5ns | 2.5ns |

SF00128

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

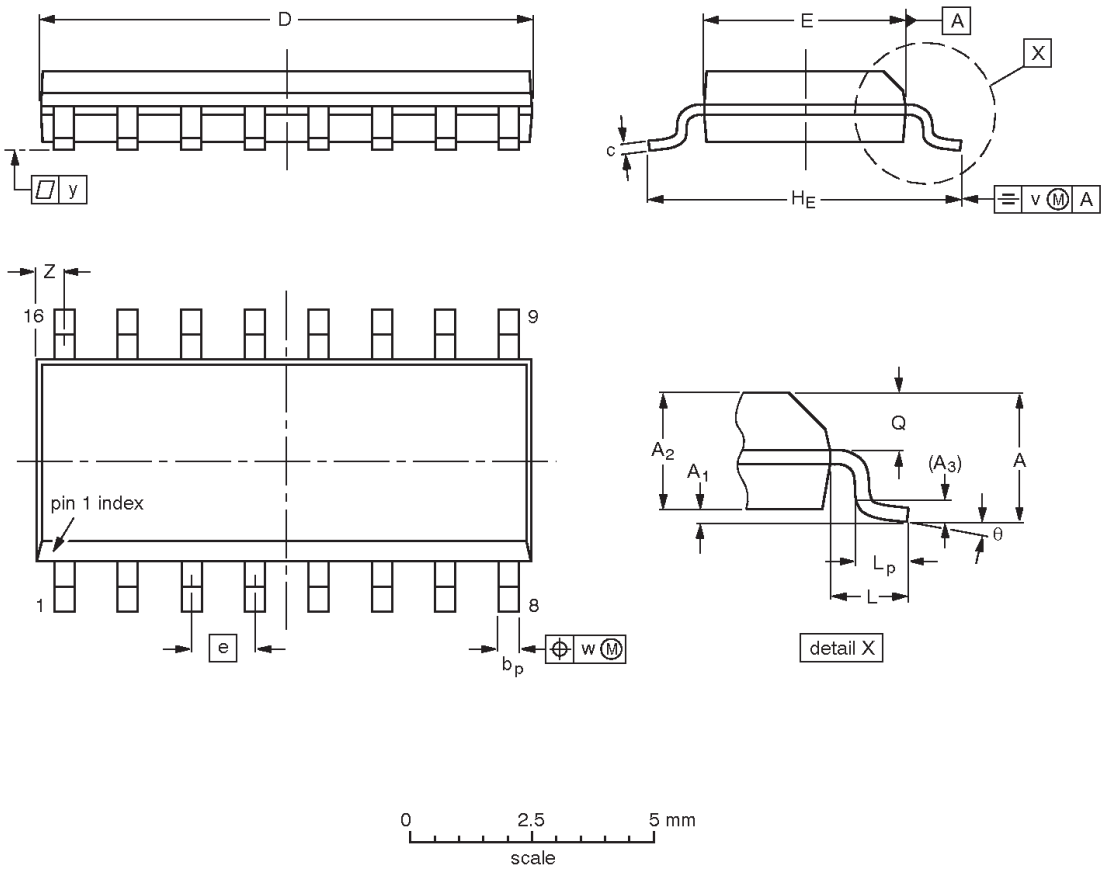
| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.10 | 0.30 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.030 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | ~~92-11-17~~<br>95-01-14 |

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.050 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | ~~95-01-23~~<br>97-05-22 |

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information —** Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support —** These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes —** Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

**Philips Semiconductors**
**811 East Arques Avenue**
**P.O. Box 3409**
**Sunnyvale, California 94088–3409**
**Telephone 800-234-7381**



print code Date of release: 10-98

Document order number: 9397-750-05088

Let's make things better.

**Philips Semiconductors**

PHILIPS