DATA SHEET

74F50729
Synchronizing dual D-type flip-flop with edge-triggered set and reset with metastable immune characteristics

Product specification

1990 Sep 14

IC15 Data Handbook

Philips Semiconductors

PHILIPS

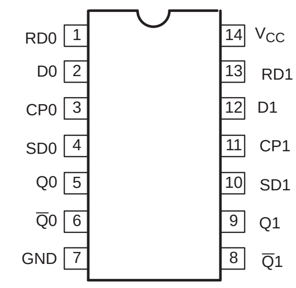
Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- See 74F5074 for synchronizing dual D–type flip–flop
- See 74F50109 for synchronizing dual J–$\overline{K}$ positive edge–triggered flip–flop
- See 74F50728 for synchronizing cascaded dual D–type flip–flop
- Industrial temperature range available (–40°C to +85°C)

PIN CONFIGURATION



SF00611

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F50729	120 MHz	19mA

DESCRIPTION

The 74F50729 is a dual positive edge–triggered D–type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

The 74F50729 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50729 are: $\tau \cong 135$ps and $\tau \cong$ 9.8 X 10^6 sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_o represents a function of the measurement of the propensity of a latch to enter a metastable state.

Set (SDn) and reset (RDn) are asynchronous positive–edge triggered inputs and operate independently of the clock (CPn) input. Data must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive–going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE		PKG DWG #
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
14–pin plastic DIP	N74F50729N	I74F50729N	SOT27-1
14–pin plastic SO	N74F50729D	I74F50729D	SOT108-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

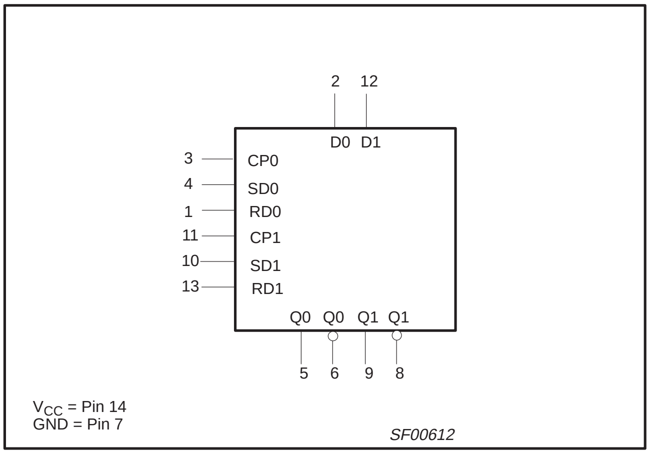
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0, D1	Data inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/1.0	20µA/20µA
SD0, SD1	Set inputs (active rising edge)	1.0/1.0	20µA/20µA
RD0, RD1	Reset inputs (active rising edge)	1.0/1.0	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

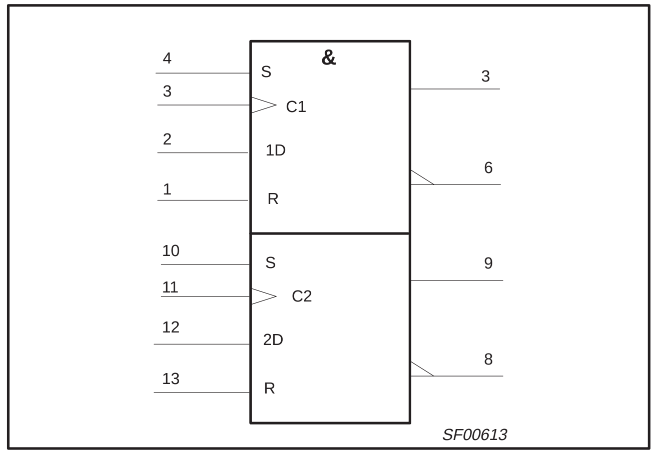
Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

LOGIC SYMBOL



IEC/IEEE SYMBOL



METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term ‘metastable immune’ to describe characteristics of some of the products in its family. Specifically the 74F50XXX family presently consist of 4 products which will not glitch or display metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volt, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50729 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/t)} / T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t’ is the time after the clock pulse that the output is sampled (t’ < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 3. it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51 X 10^{10} seconds or about 480 years.

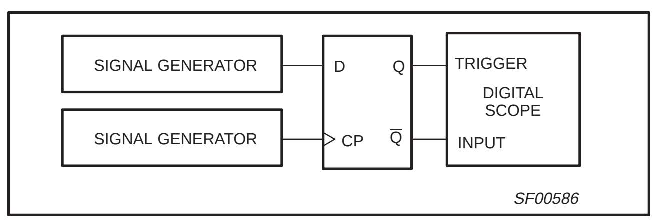


Figure 1. Test Setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

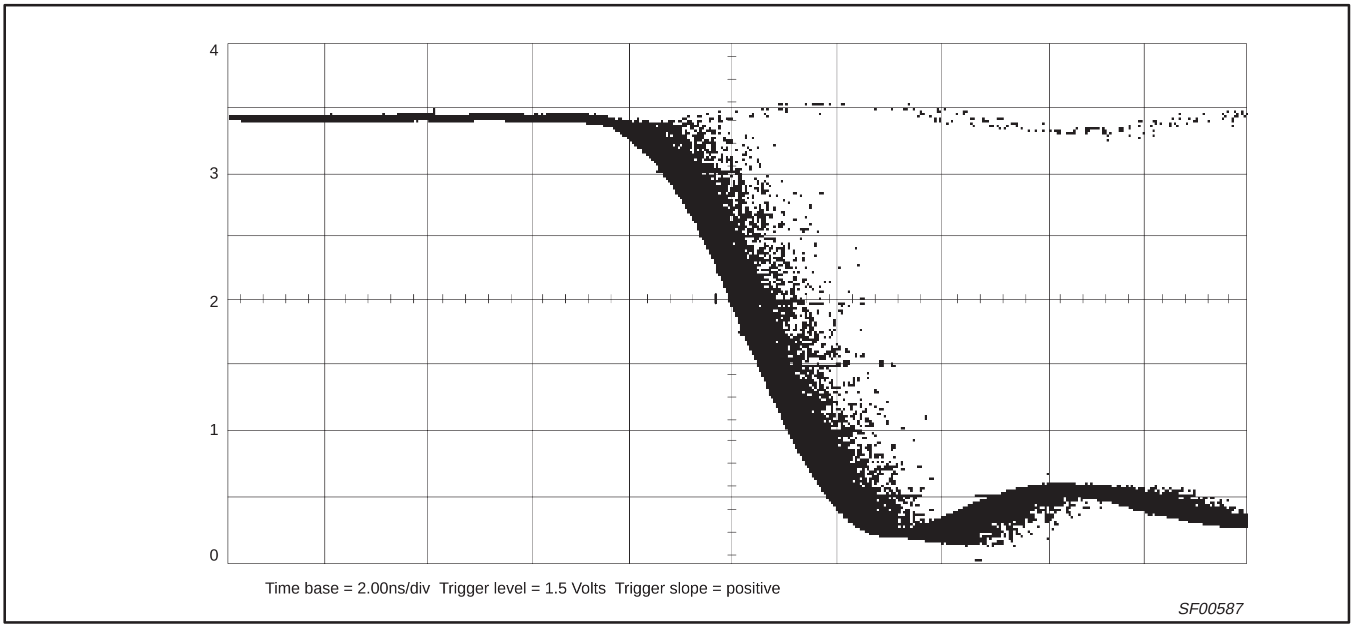


Figure 2. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

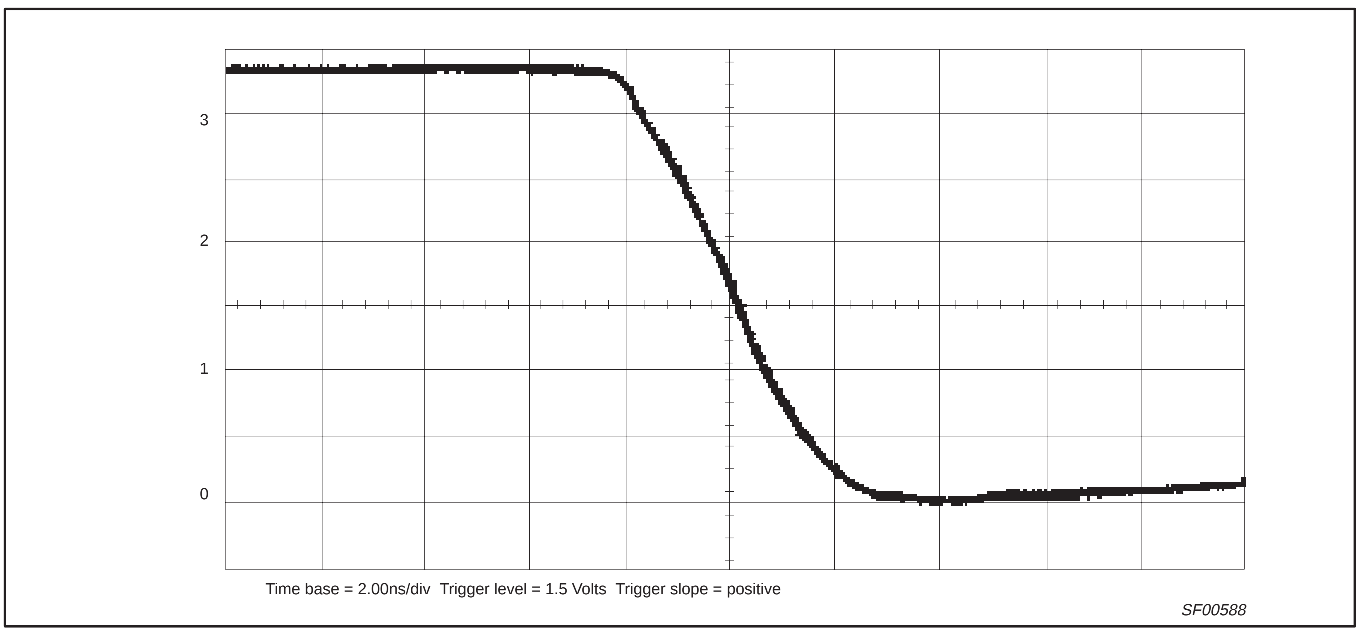
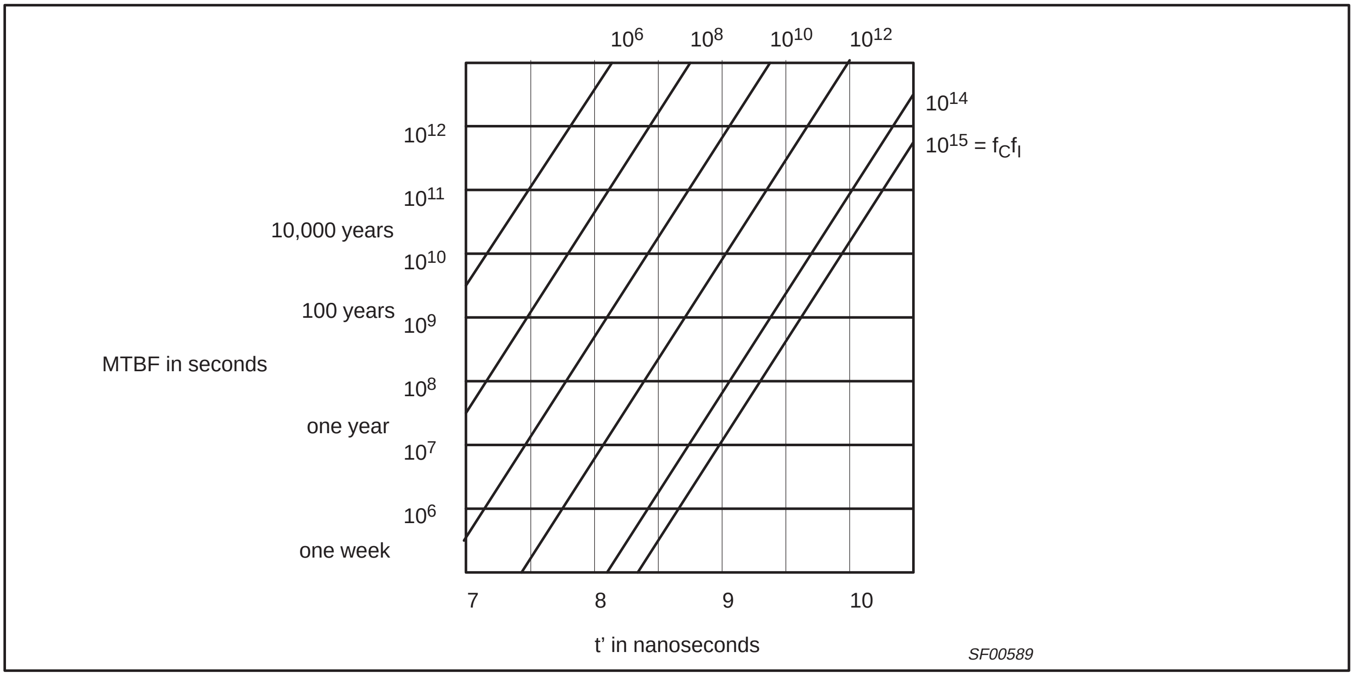


Figure 3. 74F74 $\overline{Q}$ output triggered by Q output, setup and hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'



NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^6 sec

Figure 4.

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

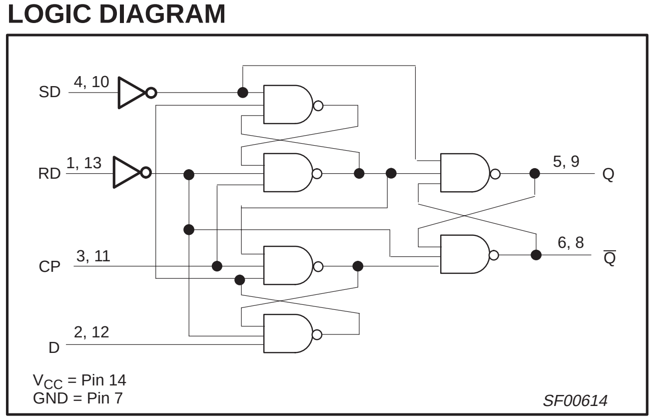
	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$	MODE
↑	↑̸	X	X	H	L	Asynchronous set
↑̸	↑	X	X	L	H	Asynchronous reset
↑̸	↑̸	↑	h	H	L	Load "1"
↑̸	↑̸	↑	l	L	H	Load "0"
↑̸	↑̸	↑̸	X	NC	NC	Hold

NOTES:
1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. NC= No change from the previous setup
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↑̸ = Not low–to–high clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		–0.5 to +7.0	V
V_{IH}	Input voltage		–0.5 to +7.0	V
I_{IN}	Input current		–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state		–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state		40	mA
T_{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	–40 to +85	°C
T_{stg}	Storage temperature range		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High–level input voltage		2.0			V
V_{IL}	Low–level input voltage				0.8	V
I_{Ik}	Input clamp current				–18	mA
I_{OH}	High–level output current	$V_{CC} \pm 10\%$			–12	mA
		$V_{CC} \pm 5\%$			–15	mA
I_{OL}	Low–level output current				20	mA
T_{amb}	Operating free air temperature range	Commercial range	0		+70	°C
		Industrial range	–40		+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS MIN	LIMITS TY.[2]	LIMITS MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
					±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low–level input current	Dn	V_{CC} = MAX, V_I = 0.5V					-250	μA
		CPn, SDn, RDn						–20	μA
I_{OS}	Short–circuit output current[3]		V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				19	27	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS: T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	105	120		85		75		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	6.5 6.5	1.5 2.0	7.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SDn RDn to Qn or $\overline{Q}$n	Waveform 2	2.0 3.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	1.5 2.0	7.5 8.0	ns
$t_{ok(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5		1.5	ns

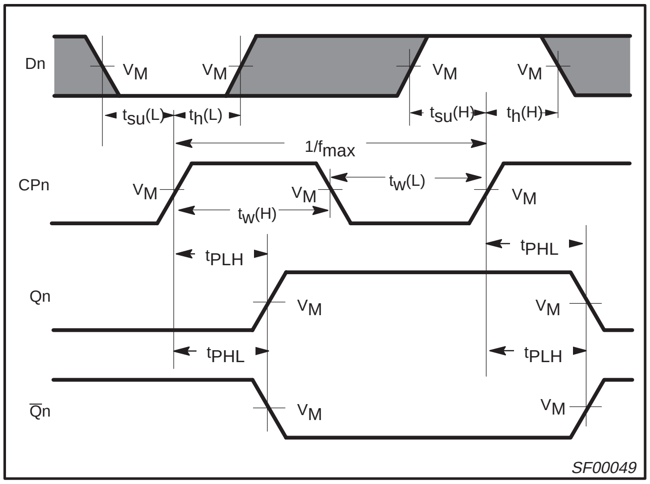
NOTES:
1. | t_{PLH} actual –t_{PHL} actual | for any one output compared to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC}, loading, etc.,).

AC SETUP REQUIREMENTS

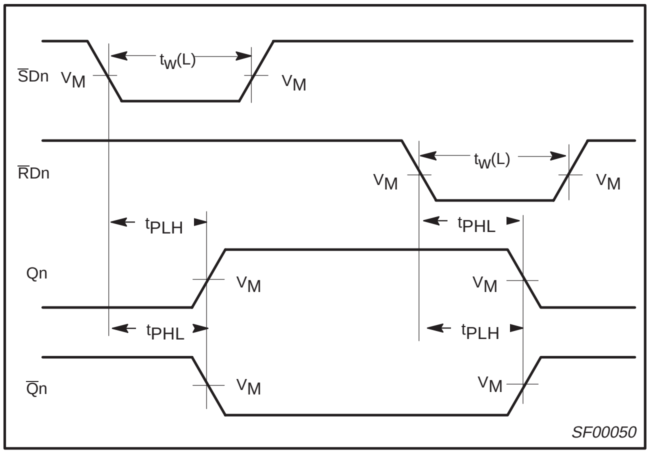
SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		T_{amb} = –40°C to +85°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Dn to CPn	Waveform 1	1.5 1.5			2.0 2.0		2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Dn to CPn	Waveform 1	1.0 1.0			1.5 1.5		1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 2	3.0 4.0			3.5 6.0		3.5 6.0		ns
t_w (L)	SDn, RDn pulse width, low	Waveform 3	3.5			4.0		4.0		ns
t_{rec}	Recovery time SDn, RDn to CPn	Waveform 3	6.0			6.5		6.5		ns
t_{rec}	Recovery time SDn to RDn or RDn to SDn	Waveform 3	6.0			1.0		1.0		ns

AC WAVEFORMS

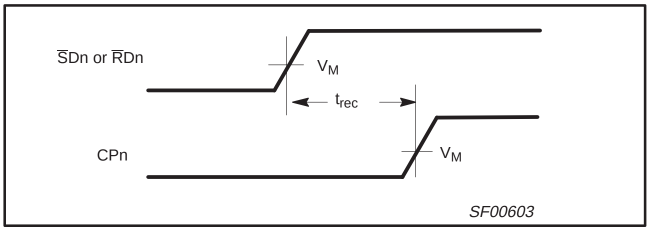
For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



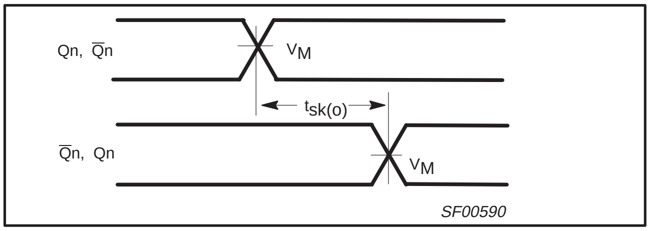
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width

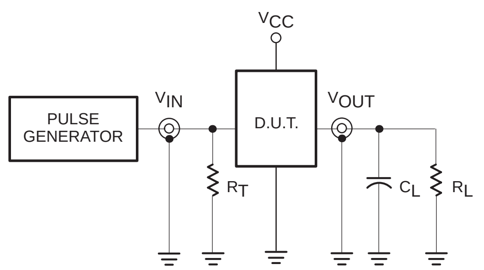


Waveform 3. Recovery time for set or reset to output

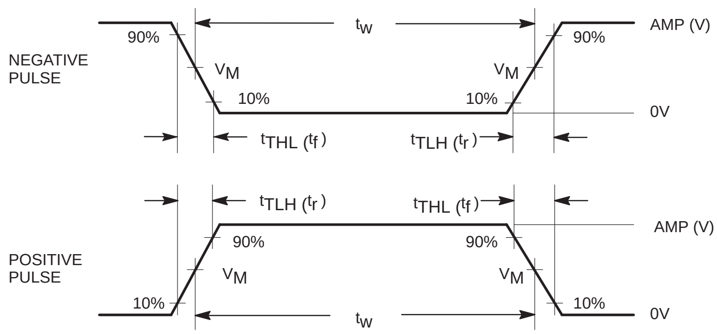


Waveform 4. Output skew

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.

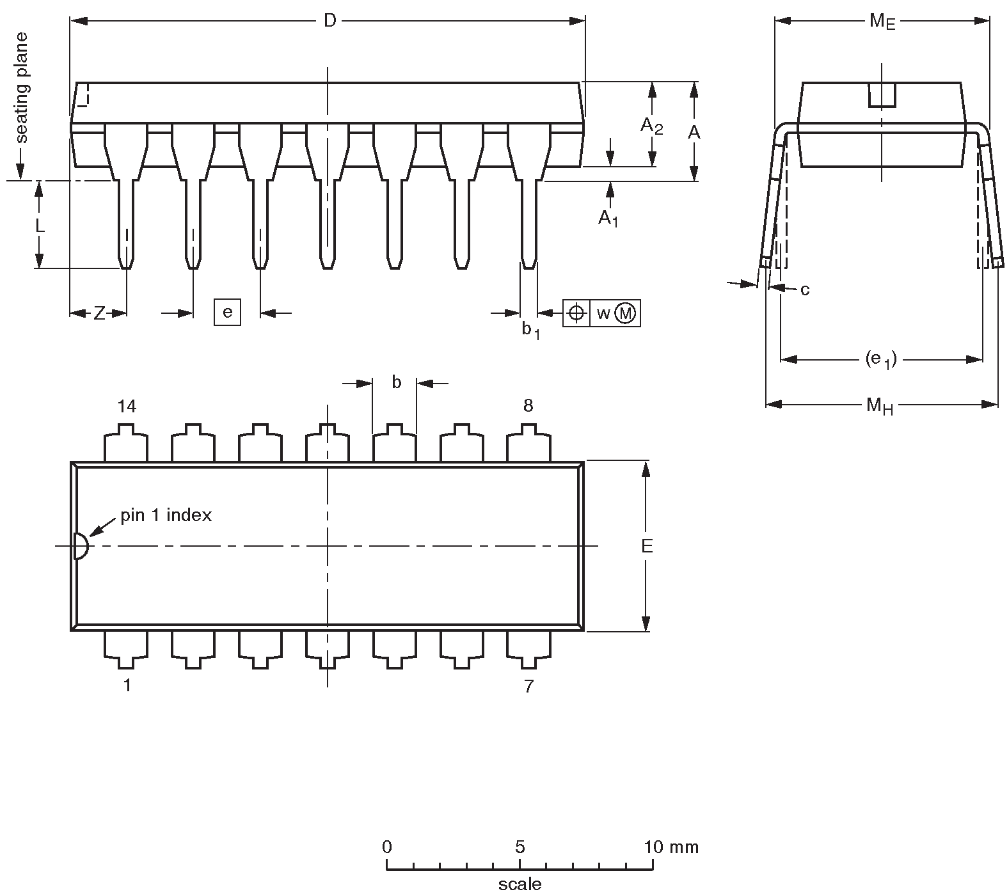
C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	**V_M**	**rep. rate**	**t_w**	**t_{TLH}**	**t_{THL}**
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00006

DIP14: plastic dual in-line package; 14 leads (300 mil) SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

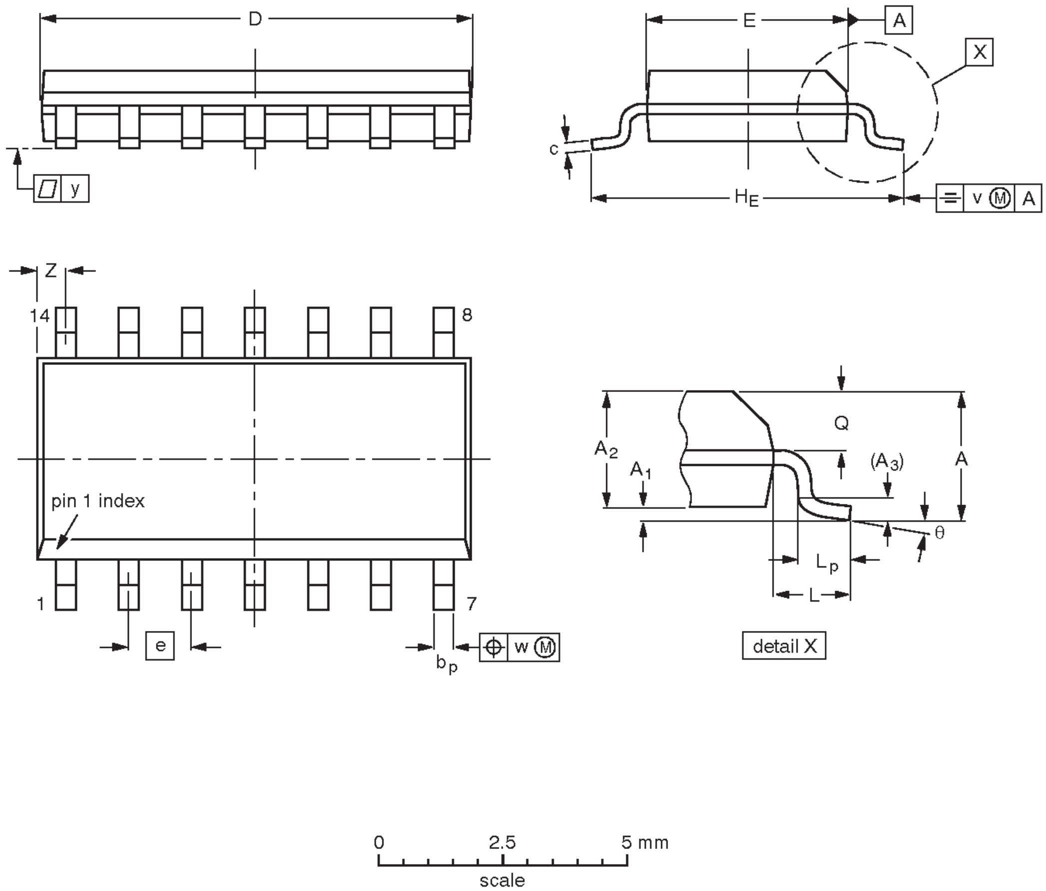
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				~~92-11-17~~ 95-03-11

SO14: plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				~~95-01-23~~ 97-05-22

Synchronizing dual D-type flip-flop with edge-triggered set and reset and metastable immune characteristics

74F50729

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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