DATA SHEET

74F670
4 x 4 register file (3-State)

Product specification

1990 Jul 12

IC15 Data Handbook

Philips
Semiconductors

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4 x 4 register file (3-State) 74F670

FEATURES

- Simultaneous and Independent Read and Write operations
- Expandable to almost any word size and bit length
- 3-State outputs

DESCRIPTION

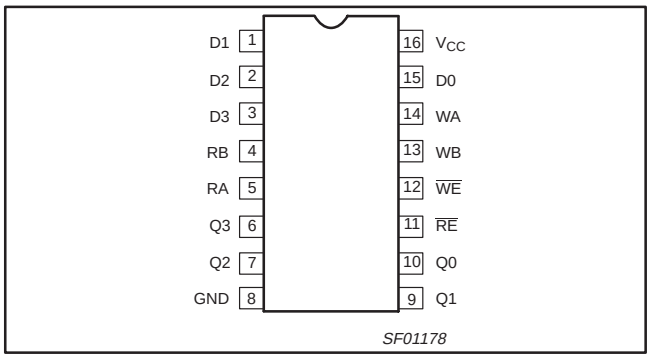
The 74F670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four data inputs.

The Write address inputs (WA and WB) determine the location of the stored word. The Write Address inputs should only be changed when the Write Enable input ($\overline{WE}$) is High for conventional operation. When the $\overline{WE}$ is Low, the data is entered into the addressed location.

The addressed location remains transparent to the data while the $\overline{WE}$ is Low. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and address inputs are inhibited when the $\overline{WE}$ is High. Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (RA, RB). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is Low. Data outputs are in the high impedance "off" state when the $\overline{RE}$ is High. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output High current, further stacking is possible by tying pullup reisistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the Low levels which cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and address inputs of each device in parallel.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F670	6.5ns	50mA

ORDERING INFORMATION

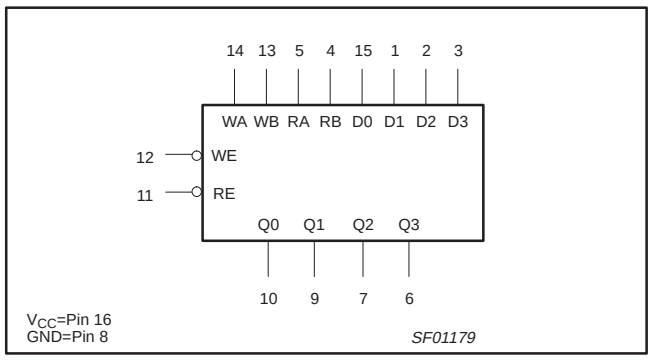
DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	PKG DWG #
16-pin plastic DIP	N74F670N	SOT38-4
16-pin plastic SOL	N74F670D	SOT162-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

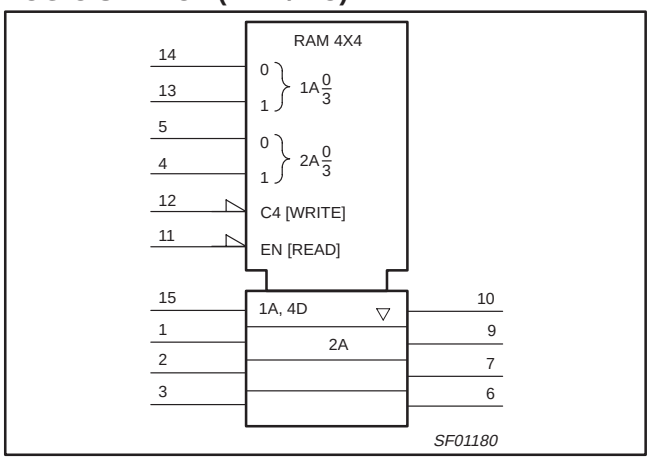
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20µA/0.6mA
WA, WB	Write address inputs	1.0/1.0	20µA/0.6mA
RA, RB	Read address inputs	1.0/1.0	20µA/0.6mA
$\overline{WE}$	Write Enable inputs	1.0/1.0	20mA/0.6mA
$\overline{RE}$	Read Enable inputs	1.0/1.0	20mA/0.6mA
Q0–Q3	Data output	150/40	3.0mA/24mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



WORD SELECT FUNCTION TABLE

WRITE MODE		READ MODE		OPERATING MODE
WB	**WA**	**RB**	**RA**	**Word Selected**
L	L	L	L	Word 0
L	H	L	H	Word 1
H	L	H	L	Word 2
H	H	H	H	Word 3

H = High voltage level
L = Low voltage level

READ MODE FUNCTION TABLE

INPUT	INTERNAL LATCHES*	OUTPUT	OPERATING MODE
$\overline{\text{RE}}$		Qn	
L	L	L	Read
L	H	H	
H	X	Z	Disabled

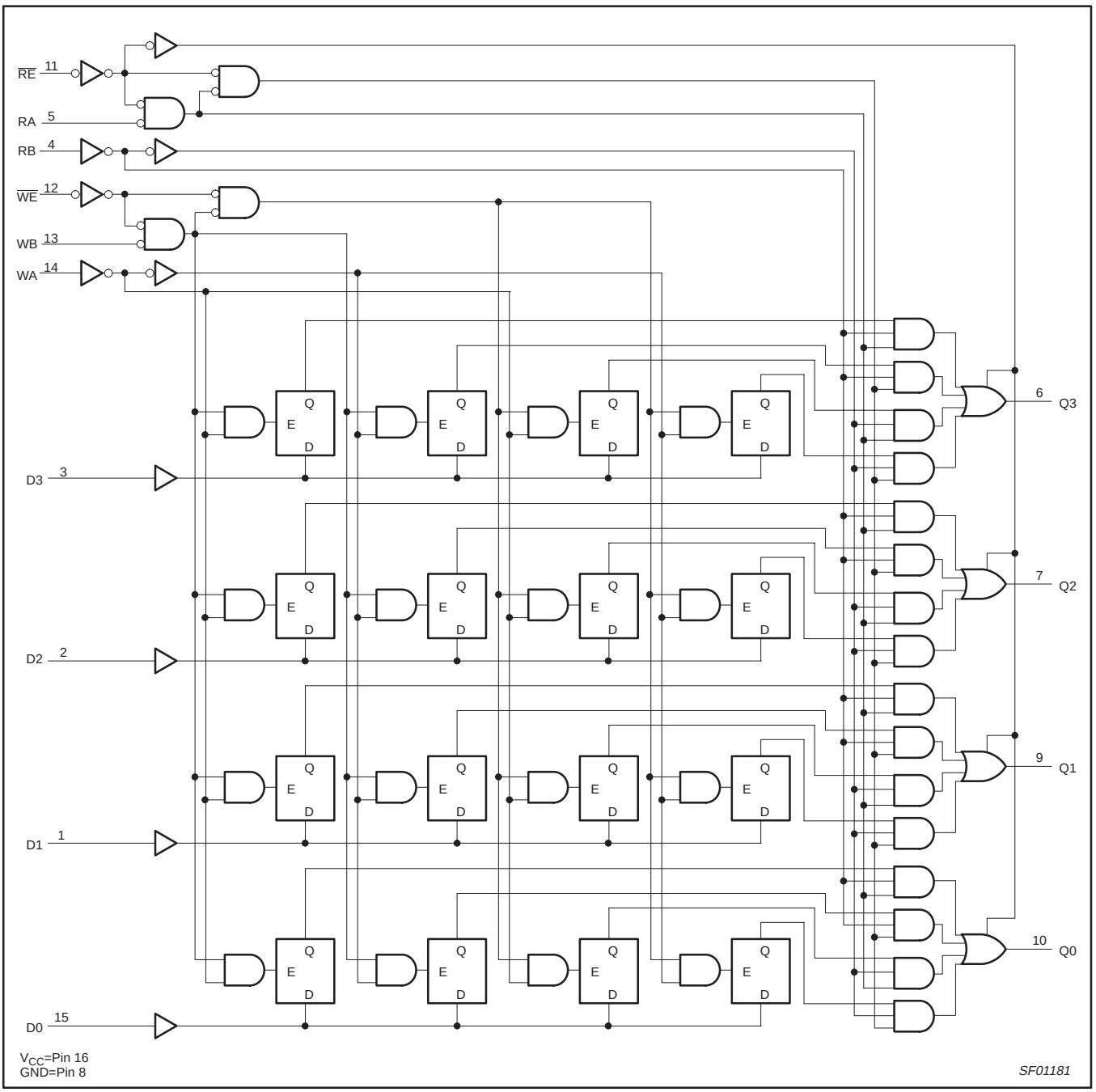
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
* = The selection of "internal latches" by Read Address (RA and RB) are not constrained by $\overline{\text{WE}}$ or $\overline{\text{RE}}$ operation.

WRITE MODE FUNCTION TABLE

INPUTS		INTERNAL LATCHES*	OPERATING MODE
$\overline{\text{WE}}$	Dn		
L	L	L	Write data
L	H	H	
H	X	NC	Data latched

H = High voltage level
L = Low voltage level
NC= No change
X = Don't care
* = The write address (WA and WB) to the "internal latches" must be stabled while $\overline{\text{WE}}$ is Low for conventional operation.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[NO TAG]		LIMITS			UNIT
					MIN	TYP NO TAG	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.4			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V				–0.6	mA
I_{OZH}	Off state output current, High-level voltage applied		V_{CC} = MAX, V_O = 2.7V				50	µA
I_{OZL}	Off state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V				–50	µA
I_{OS}	Short-circuit output current[NO TAG]		V_{CC} = MAX		–60		–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			50	70	mA
		I_{CCL}				50	70	mA
		I_{CCZ}				55	80	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting

of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb}= +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay RA, RB to Qn	Waveform 3, 4	3.5 4.0	5.5 5.5	9.0 8.5	3.0 3.5	10.0 9.9	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{WE}$ to Qn	Waveform 1, 2	5.0 6.5	7.0 8.5	10.0 11.5	4.5 6.0	11.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	Waveform 1, 2	3.5 6.0	6.0 8.0	8.5 11.0	3.0 5.5	9.5 12.5	ns ns
t_{PZH} t_{PZL}	$\overline{RE}$ Enable time Qn to High or Low level	Waveform 5 Waveform 6	3.0 4.5	7.0 6.5	12.0 9.0	2.5 4.0	13.0 10.0	ns ns
t_{PHZ} t_{PLZ}	$\overline{RE}$ Disable time Qn to High or Low level	Waveform 5 Waveform 6	2.0 3.0	3.0 5.0	6.5 8.5	1.5 3.0	7.5 8.5	ns ns

AC SETUP REQUIREMENTS

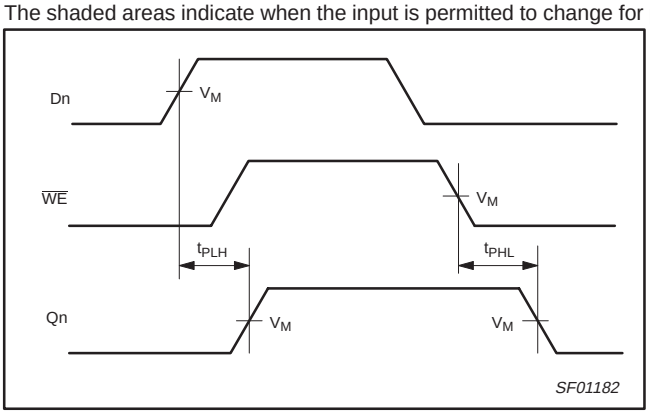
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to positive going $\overline{WE}$	Waveform 3, 4	1.5 6.0			1.5 7.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to positive going $\overline{WE}$	Waveform 3, 4	0 1.0			0 1.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low WA, WB to negative going WE[1]	Waveform 3, 4	0 0			0 0		ns ns
t_h(H) t_h(L)	Hold time, High or Low WA, WB to negative going WE[1]	Waveform 3, 4	0 0			0 0		ns ns
t_w(L)	$\overline{WE}$ Pulse width, Low	Waveform 3, 4	6.5			8.5		ns

NOTES:

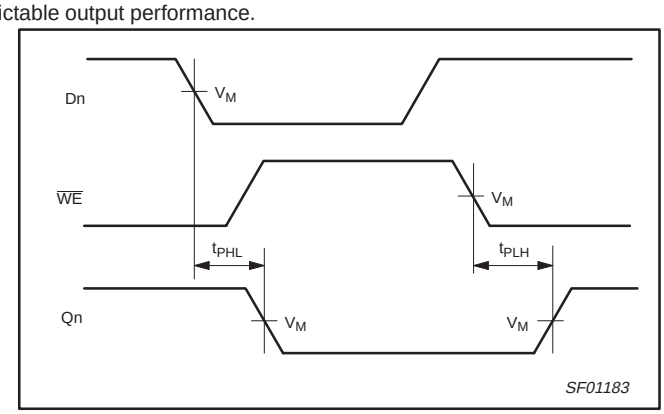
1. Write Address (WA, WB) setup time will protect the data written into the previous address. If protection of data in the previous address is not required, setup time for Write Address to $\overline{WE}$ can be ignored. Any address selection sustained for the final 7ns of the $\overline{WE}$ pulse during hold time for Write Address to $\overline{WE}$ will result in data being written into that location.

AC WAVEFORMS

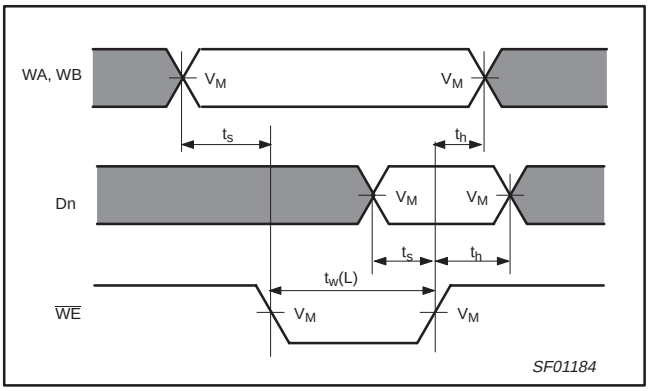
For all waveforms, V_M=1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



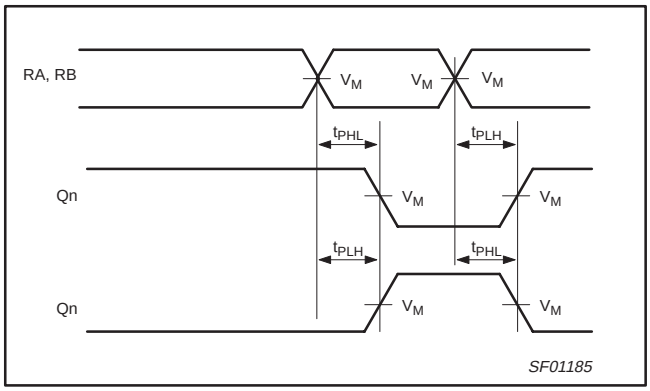
Waveform 1. Propagation Delay, Write Enable and Data to Outptus



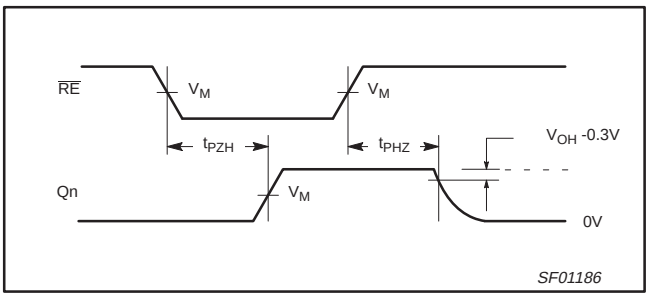
Waveform 2. Propagation Delay, Write Enable and Data to Outputs



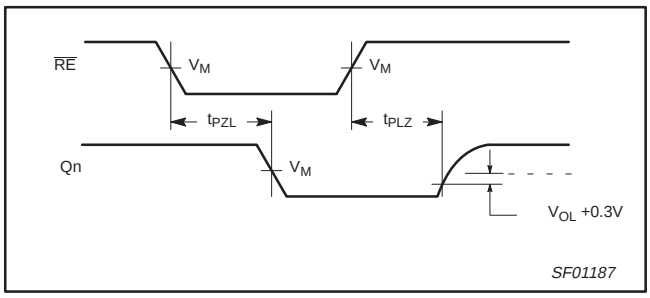
Waveform 3. Setup and Hold Times for Write Address to Write Enable and Data to Write Enable



Waveform 4. Propagation Delays for Read Address to Output

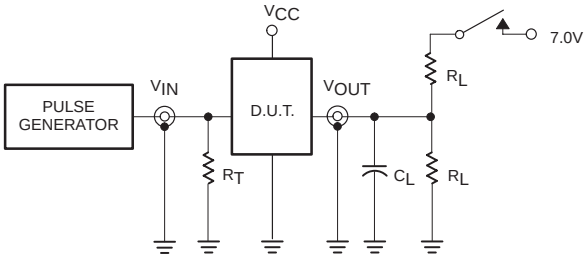


Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level

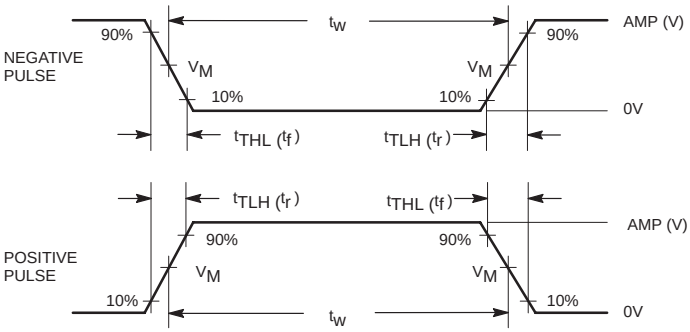


Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

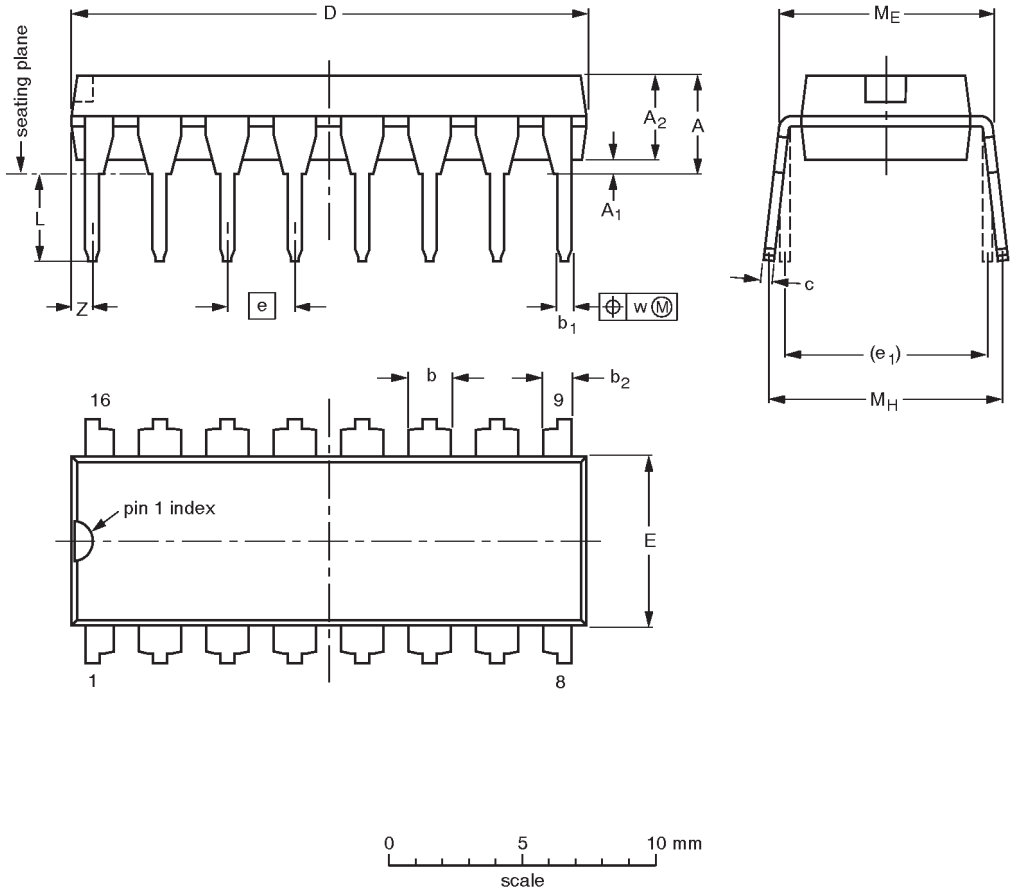
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

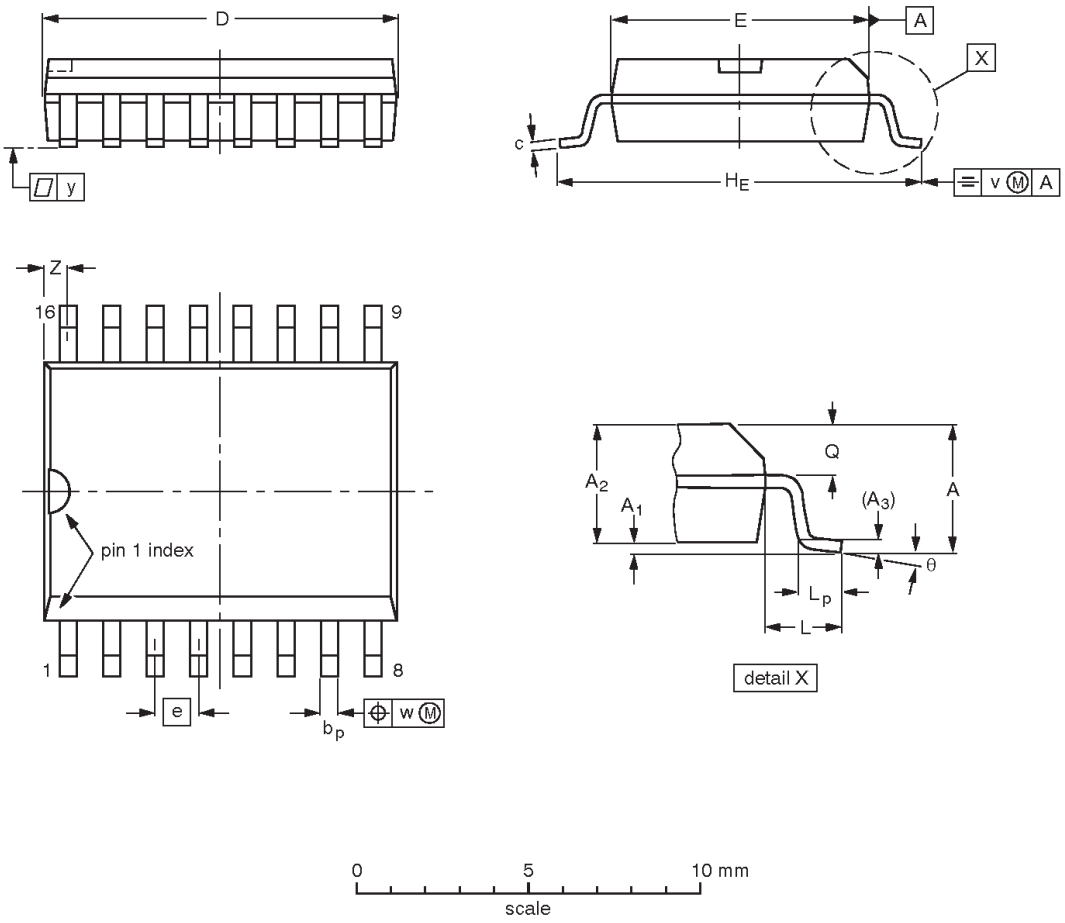
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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