

DATA SHEET

74F756

Octal inverter buffer (open-collector)

74F757

Octal buffer (open-collector)

74F760

Octal buffer (open-collector)

Product specification

1989 Nov 27

IC15 Data Handbook

Buffers

74F756/74F757/74F760

74F756 Octal Inverter Buffer (Open Collector)
 74F757 Octal Buffer (Open Collector)
 74F760 Octal Buffer (Open Collector)

FEATURES

- Octal bus interface
- Open collector versions of 74F240, 74F241 and 74F244

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables. $\overline{OE}a$ and $\overline{OE}b$ (or OEb for the 74F757), each controlling four of the outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	N74F756N, N74F757AN, N74F760N	SOT146-1
20-pin plastic SOL	N74F756D, N74F757AD, N74F760D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.67	20 μ A/1.0mA
$\overline{OE}a$, $\overline{OE}b$	Output enable input (active Low)	1.0/1.67	20 μ A/0.2mA
OEb	Output enable input (active High 74F757)	1.0/1.67	20 μ A/1.0mA
Yan, Ybn	Data outputs (74F757, 74F760)	OC/106.7	OC/64mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs (74F756)	OC/106.7	OC/64mA

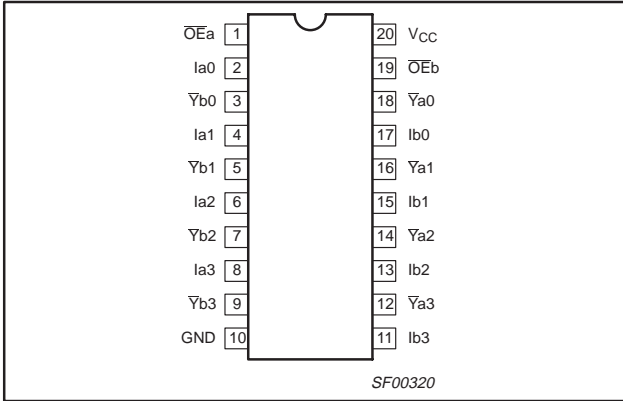
Notes:

One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the Low state.
 OC=Open Collector

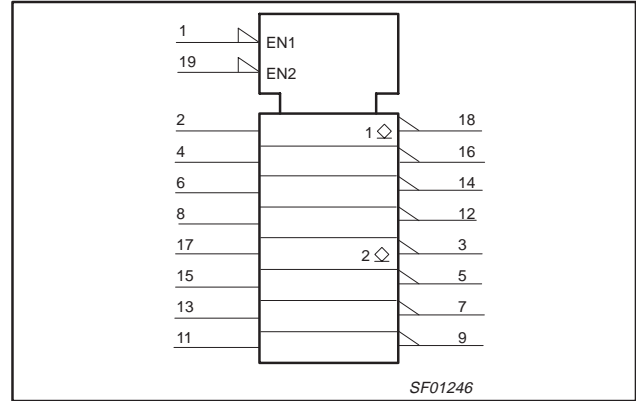
Buffers

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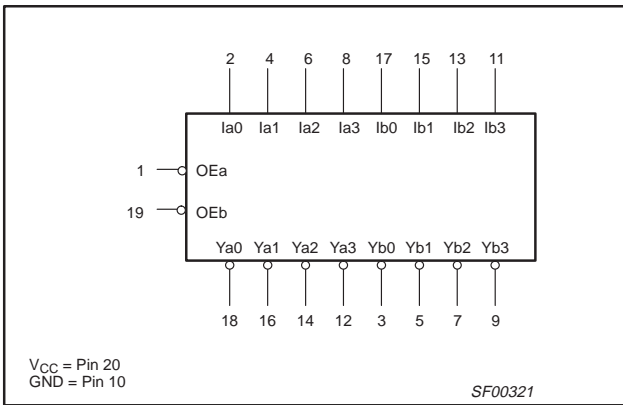
PIN CONFIGURATION for 74F756



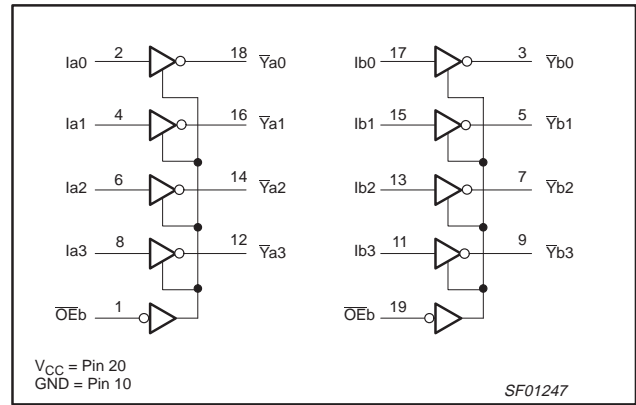
IEC/IEEE SYMBOL for 74F756



LOGIC SYMBOL for 74F756



LOGIC DIAGRAM for 74F756



FUNCTION TABLE for 74F756

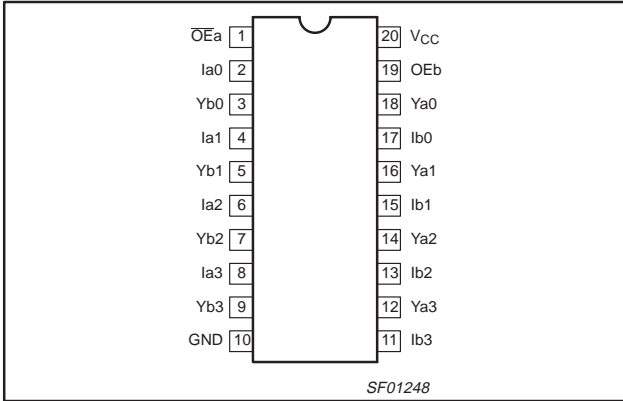
INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H (off)	H (off)

H = High voltage level
 L = Low voltage level
 X = Don't care

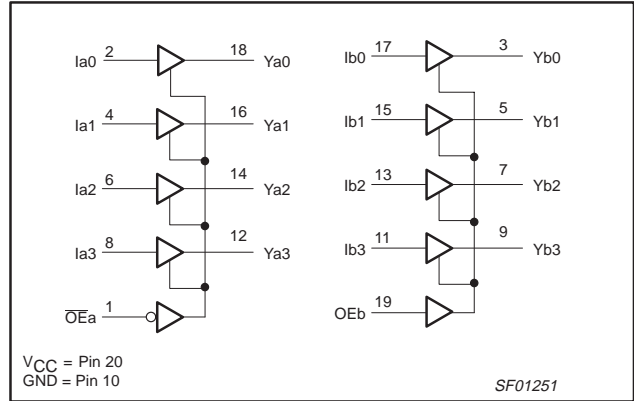
Buffers

74F756/74F757/74F760

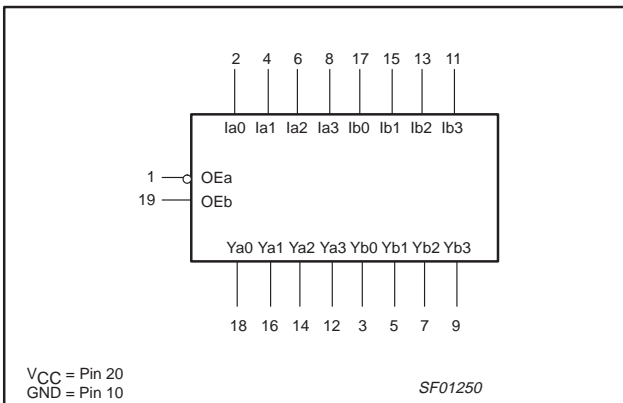
PIN CONFIGURATION for 74F757



LOGIC DIAGRAM for 74F757



LOGIC SYMBOL for 74F757

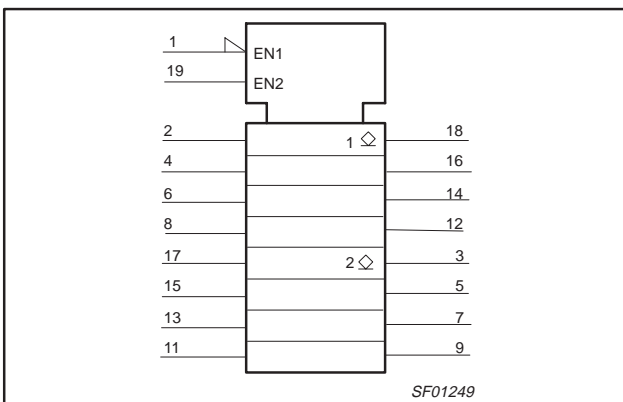


FUNCTION TABLE for 74F757

INPUTS				OUTPUTS	
OEa	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H (off)	H (off)

H = High voltage level
 L = Low voltage level
 X = Don't care

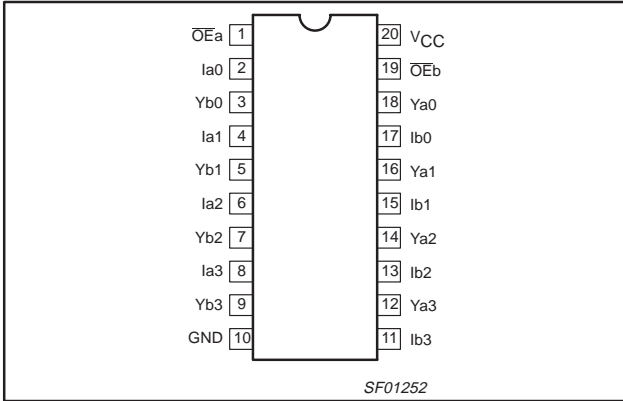
IEC/IEEE SYMBOL for 74F757



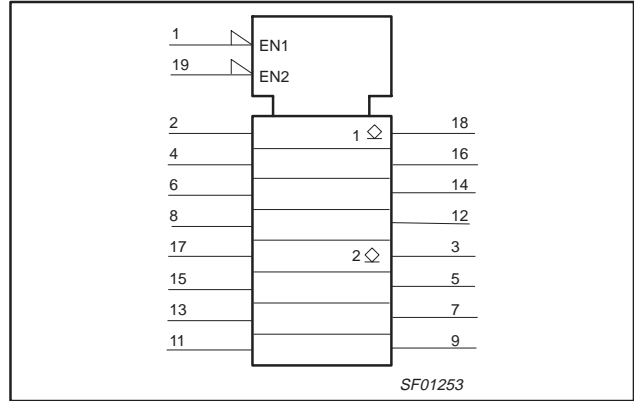
Buffers

74F756/74F757/74F760

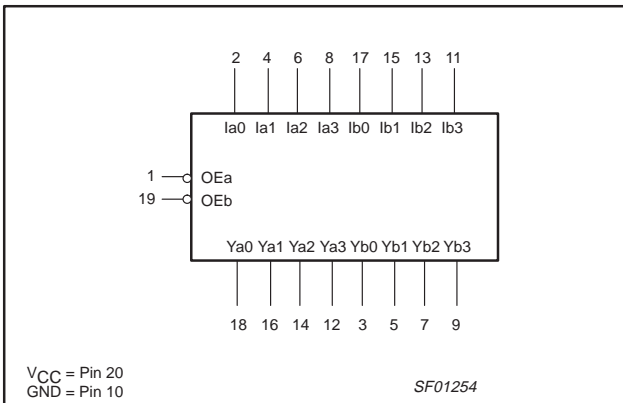
PIN CONFIGURATION for 74F760



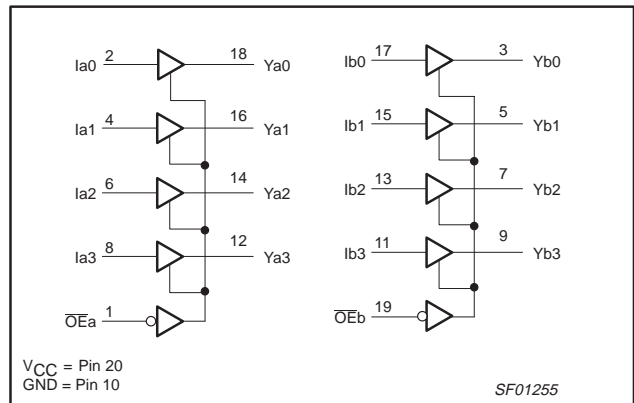
IEC/IEEE SYMBOL for 74F760



LOGIC SYMBOL for 74F760



LOGIC DIAGRAM for 74F760



FUNCTION TABLE for 74F760

INPUTS				OUTPUTS	
\overline{OEa}	Ia	\overline{OEb}	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

Buffers

74F756/74F757/74F760

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	-0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	128	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
V _{OH}	High-level output voltage			4.5	V
I _{OL}	Low-level output current			64	mA
T _{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			MIN	TYP ²	MAX		
I _{OH}	High-level output current	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, V _{OH} = MAX			250	μA	
V _{OL}	Low-level output voltage	I _{OL} = 48MAX		0.38	0.55	V	
		I _{OL} = 64mA	±10%V _{CC}	0.42	0.55	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		-0.73	-1.2	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			100	μA	
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V			-1.0	mA	
I _{CC}	Supply current (total)	V _{CC} = MAX	74F756	I _{CCH}	20	30	mA
				I _{CCL}	50	70	mA
			74F757	I _{CCH}	30	40	mA
				I _{CCL}	55	80	mA
			74F760	I _{CCH}	25	37	mA
				I _{CCL}	55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

Buffers

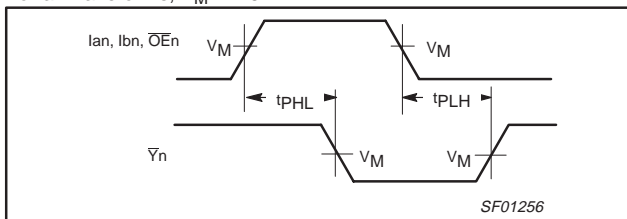
74F756/74F757/74F760

AC ELECTRICAL CHARACTERISTICS

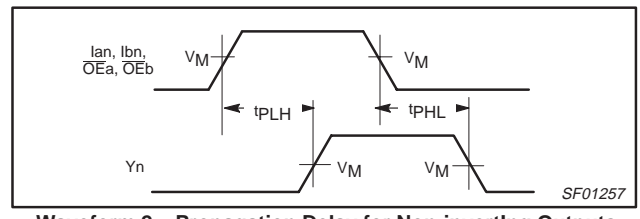
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to \bar{Y}_n	74F756	Waveform 1, 2	8.5	11.0	14.0	8.5	15.0	ns
t _{PLH} t _{PHL}	Propagation delay OE _n to \bar{Y}_n			1.0	3.0	6.0	1.0	6.5	
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F757	Waveform 1, 2	7.5	10.5	13.5	7.5	14.0	ns
t _{PLH} t _{PHL}	Propagation delay OE _a or OE _b to Y _n			3.0	5.5	8.5	3.0	9.0	
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F760	Waveform 1, 2	7.5	10.0	13.5	7.5	14.0	ns
t _{PLH} t _{PHL}	Propagation delay OE _n to Y _n			3.5	5.5	8.5	3.0	9.0	
t _{PLH} t _{PHL}	Propagation delay OE _n to Y _n	74F760	Waveform 1, 2	9.5	11.5	14.5	9.0	15.0	ns
t _{PLH} t _{PHL}	Propagation delay OE _n to Y _n			5.0	7.0	10.5	4.5	10.5	

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

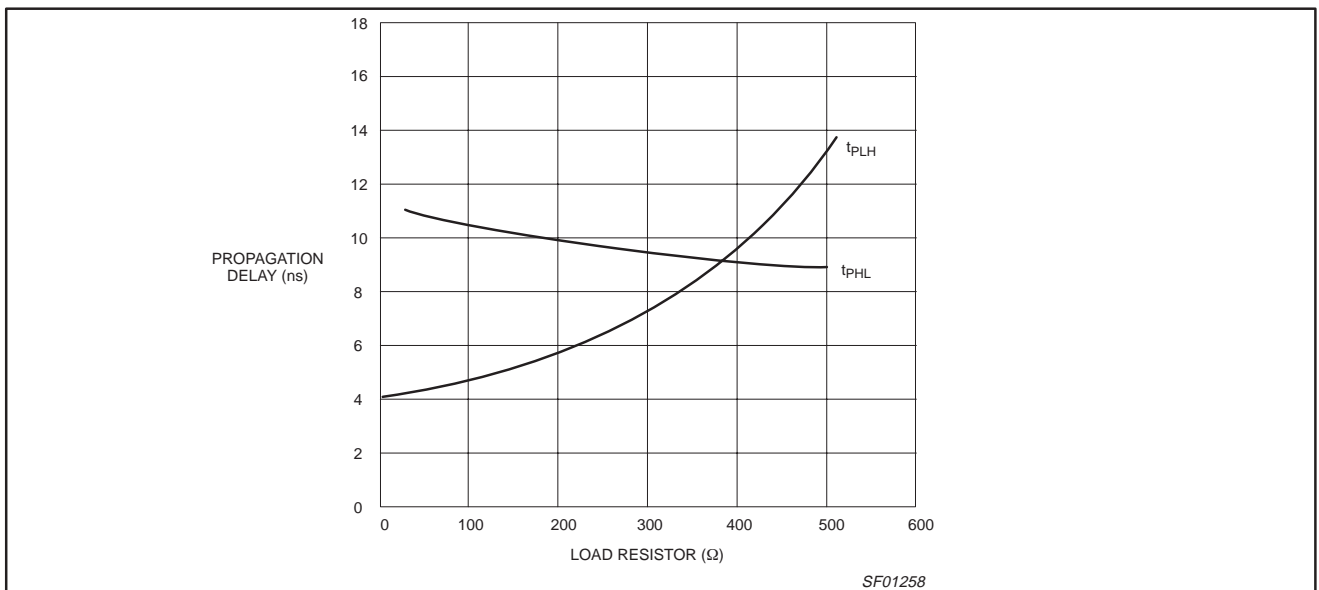


Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-inverting Outputs

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS



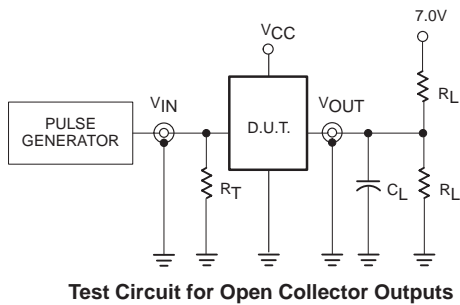
NOTE:

When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

Buffers

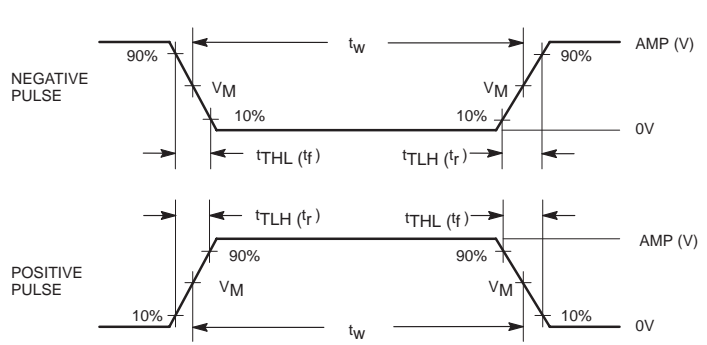
74F756/74F757/74F760

TEST CIRCUIT AND WAVEFORMS



DEFINITIONS:

- R_L = Load resistor; see AC electrical characteristics for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

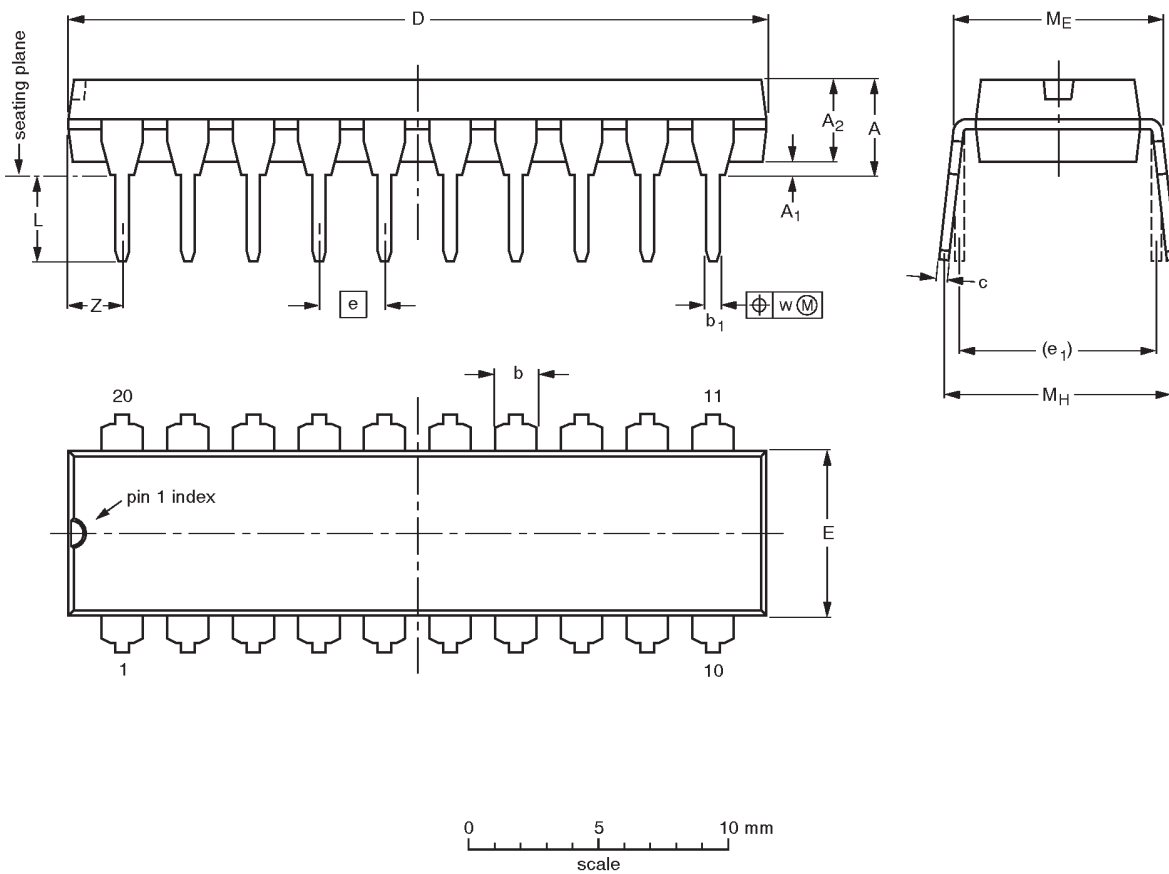
SF00027

Buffers

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74F760

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

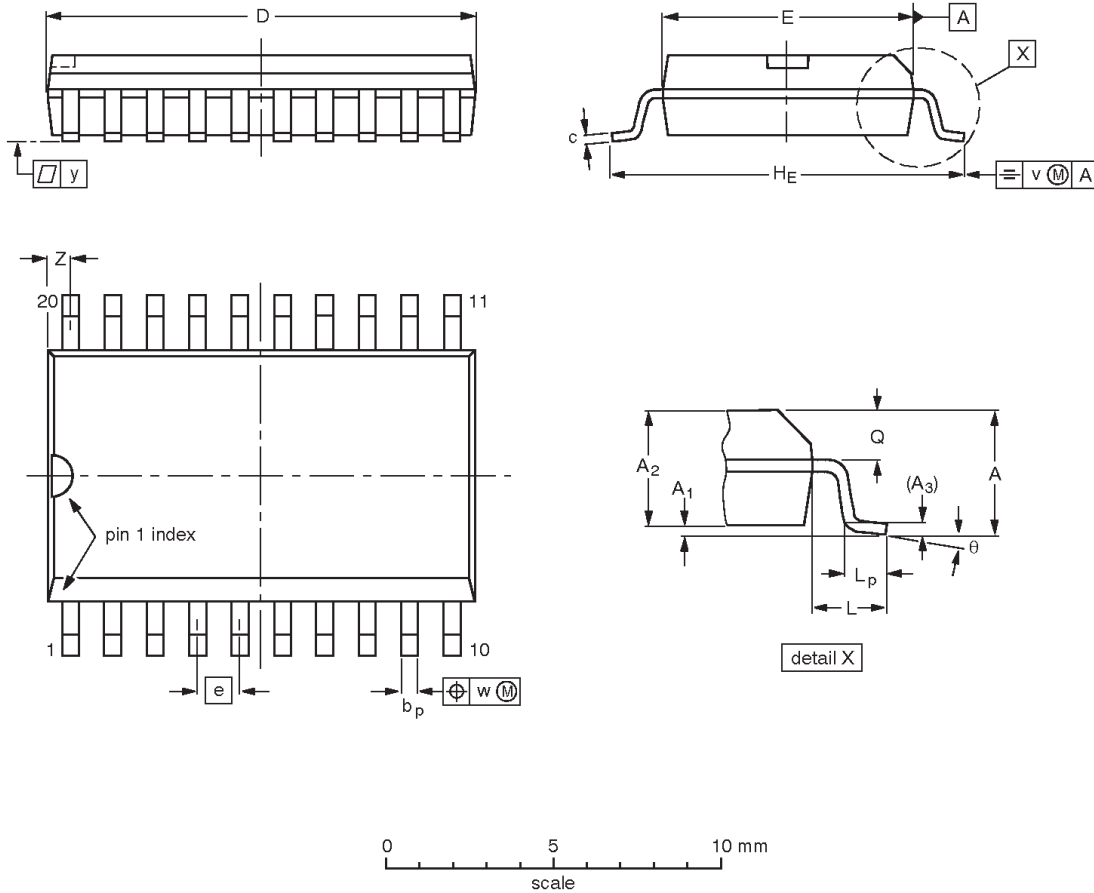
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Buffers

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	g° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT163-1	075E04	MS-013AC			-95-01-24 97-05-22

Buffers

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74F760

NOTES

Buffers

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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