DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4751V
LSI
Universal divider

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Universal divider

HEF4751V
LSI

DESCRIPTION

The HEF4751V is a universal divider (U.D.) intended for use in high performance phase lock loop frequency synthesizer systems. It consists of a chain of counters operating in a programmable feedback mode. Programmable feedback signals are generated for up to three external (fast) ÷ 10/11 prescaler.

The system comprising one HEF4751V U.D. together with prescalers is a fully programmable divider with a maximum configuration of: 5 decimal stages, a programmable mode M stage ($1 \leq M \leq 16$, non-decimal fraction channel selection), and a mode H stage (H = 1 or 2, stage for half channel offset).
Programming is performed in BCD code in a bit-parallel, digit-serial format.

To accommodate fixed or variable frequency offset, two numbers are applied in parallel, one being subtracted from the other to produce the internal programme.
The decade selection address is generated by an internal programme counter which may run continuously or on demand. Two or more universal dividers can be cascaded, each extra U.D. (in slave mode) adds two decades to the system. The combination retains the full programmability and features of a single U.D. The U.D. provides a fast output signal FF at output OFF, which can have a phase jitter of ± 1 system input period, to allow fast frequency locking. The slow output signal FS at output OFS, which is jitter-free, is used for fine phase control at a lower speed.

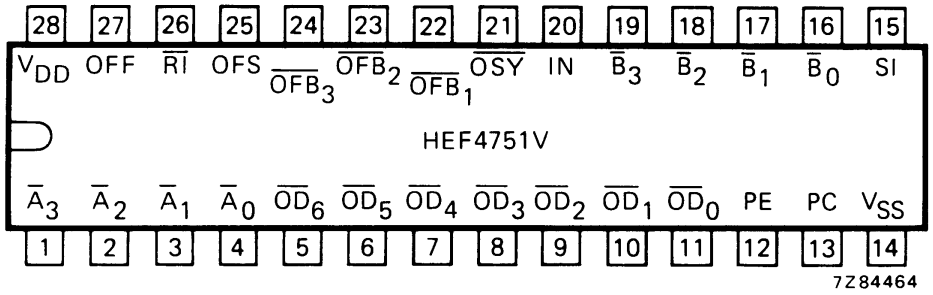


Fig.1 Pinning diagram.

HEF4751VP(N): 28-lead DIL; plastic (SOT117)
HEF4751VD(F): 28-lead DIL; ceramic (cerdip) (SOT135V)
HEF4751VT(D): 28-lead SO; plastic (SOT136A)
( ): Package Designator North America

SUPPLY VOLTAGE

RATING	RECOMMENDED OPERATING
–0,5 to + 18	4,5 to 12,5 V

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

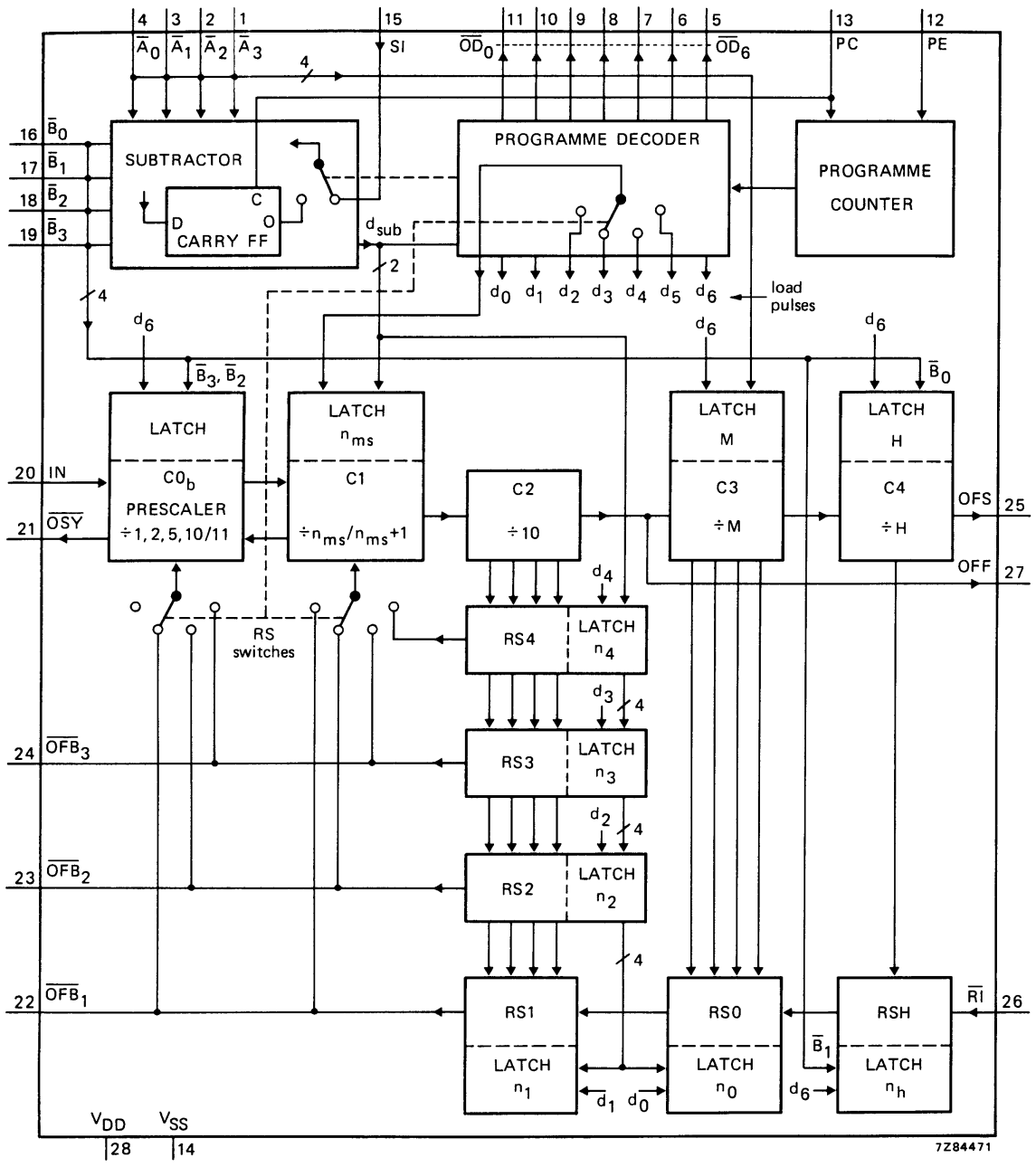
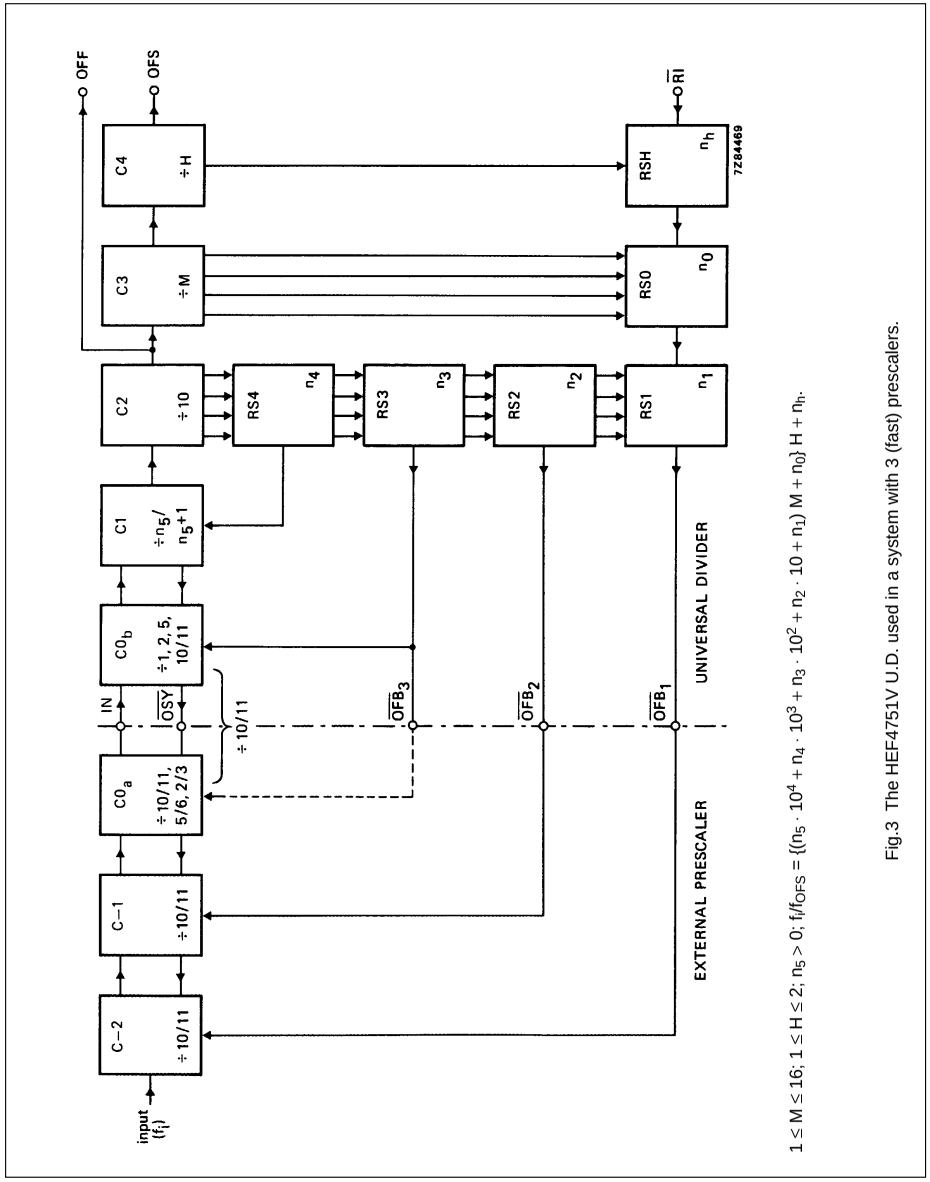


Fig.2 Block diagram.



$1 \leq M \leq 16$; $1 \leq H \leq 2$; $n_5 > 0$; $f_i/f_{OFS} = \{(n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1)\ M + n_0\}\ H + n_h$.

Fig.3 The HEF4751V U.D. used in a system with 3 (fast) prescalers.

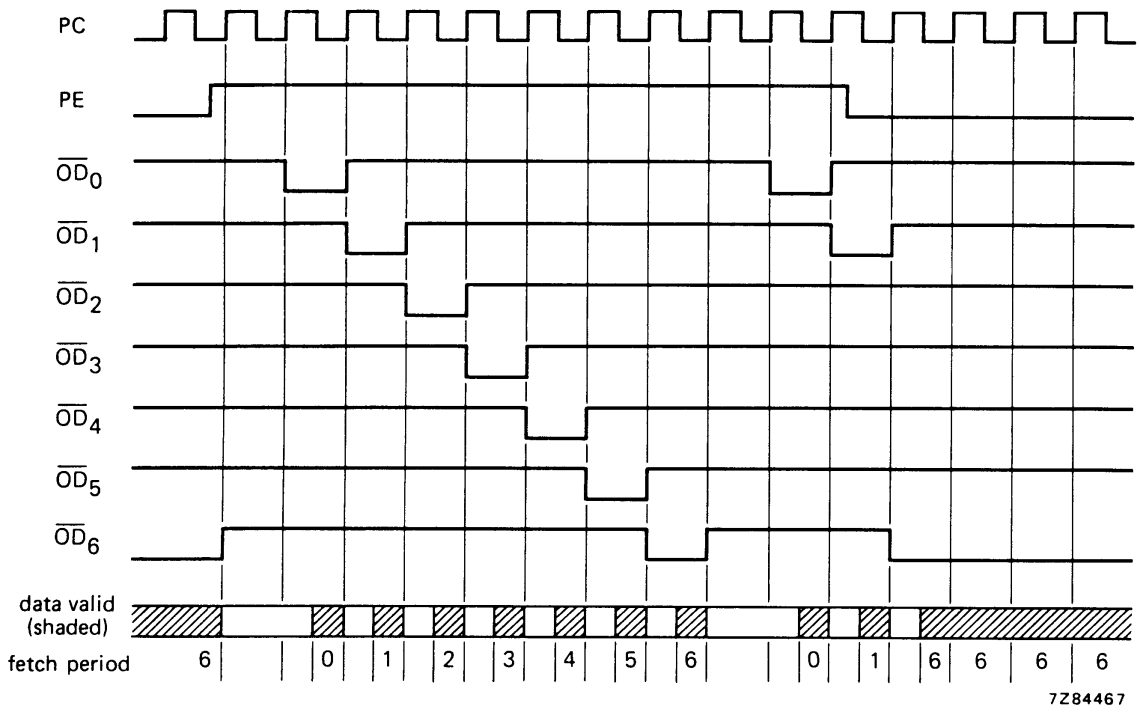


Fig.4 Timing diagram showing programme data inputs.

Allocation of data input

FETCH PERIOD	INPUTS								
	$\overline{A}_3$	$\overline{A}_2$	$\overline{A}_1$	$\overline{A}_0$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$	SI
0	n_{0A}				n_{0B}				b_{in}
1	n_{1A}				n_{1B}				X
2	n_{2A}				n_{2B}				X
3	n_{3A}				n_{3B}				X
4	n_{4A}				n_{4B}				X
5	n_{5A}				n_{5B}				X
6	M				$C0_b$ control		½ channel control		X

Allocation of data input $\overline{B}3$ to $\overline{B}0$ during fetch period 6

$\overline{B}_3$	$\overline{B}_2$	$C0_b$ DIVISION RATIO
L	L	1
L	H	2
H	L	5
H	H	10/11

$\overline{B}_1$	$\overline{B}_0$	½ CHANNEL CONFIGURATION
L	L	H = 1
L	H	H = 2; n_h = 0
H	H	H = 2; n_h = 1
H	L	test state

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

PROGRAMME DATA INPUT (see also Figs 3 and 4)

The programming process is timed and controlled by input PC and PE. When the programme enable (PE) input is HIGH; the positive edges of the programme clock (PC) signal step through the internal programme counter in a sequence of 8 states. Seven states define fetch periods, each indicated by a LOW signal at one of the corresponding data address outputs ($\overline{OD}_0$ to $\overline{OD}_6$). These data address signals may be used to address the external programme source. The data fetched from the programme source is applied to inputs $\overline{A}_0$ to $\overline{A}_3$ and $\overline{B}_0$ to $\overline{B}_3$. When PC is LOW in a fetch period an internal load pulse is generated, the data is valid during this time and has to be stable. When PE is LOW, the programming cyclus is interrupted on the first positive edge of PC. On the next negative edge at input PC fetch period 6 is entered. Data may enter asynchronously in fetch period 6.

Ten blocks in the U.D. need programme input signals (see Fig.2). Four of these ($C0_b$, C3, C4 and RSH) are concerned with the configuration of the U.D. and are programmed in fetch period 6. The remaining blocks (RS0 to RS4 and C1) are programmed with number P, consisting of six internal digits n_0 to n_5.

$$P = (n_5 \cdot 10^4 + n_4 \cdot 10^3 + n_3 \cdot 10^2 + n_2 \cdot 10 + n_1) \cdot M + n_0$$

These digits are formed by a substractor from two external numbers A and B and a borrow-in (b_{in}).

$P = A - B - b_{in}$ or if this result is negative;
$P = A - B - b_{in} + M \cdot 10^5$.

The numbers A and B, each consisting of six four bit digits n_{0A} to n_{5A} and n_{0B} to n_{5B}, are applied in fetch period 0 to 5 to the inputs $\overline{A}_0$ to $\overline{A}_3$ (data A) and $\overline{B}_0$ to $\overline{B}_3$ (data B) in binary coded negative logic.

$$A = (n_{5A} \cdot 10^4 + n_{4A} \cdot 10^3 + n_{3A} \cdot 10^2 + n_{2A} \cdot 10 + n_{1A}) \cdot M + n_{0A}.$$

$$B = (n_{5B} \cdot 10^4 + n_{4B} \cdot 10^3 + n_{3B} \cdot 10^2 + n_{2B} \cdot 10 + n_{1B}) \cdot M + n_{0B}.$$

Borrow-in (b_{in}) is applied via input SI in fetch period 0 (SI = HIGH: borrow, SI = LOW: no borrow).

Counter C1 is automatically programmed with the most significant non-zero digit (n_{ms}) from the internal digits n_5 to n_2 of number P. The counter chain C – 2 to C1 (see Fig.3) is fully programmable by the use of pulse rate feedback.

Rate feedback is generated by the rate selectors RS4 to RS0 and RSH, which are programmed with digits n_4 to n_0 and n_h respectively. In fetch period 6 the fractional counter C3, half channel counter C4 and $C0_b$ are programmed and configured via data B inputs. Counter C3 is programmed in fetch period 6 via data A inputs in negative logic (except all HIGH is understood as: M = 16). The counter C0 is a side steppable 10/11 counter composed of an internal part $C0_b$ and an external part $C0_a$. $C0_b$ is configured via $\overline{B}_3$ and $\overline{B}_2$ to a division ratio of 1 or 2 or 5 or 10/11; $C0_a$ must have the complementary ratio 10/11 or 5/6 or 2/3 or 1 respectively. In the latter case $C0_b$ comprises the whole C0 counter with internal feedback, $C0_a$ is then not required.

The half channel counter C4 is enabled with $\overline{B}_0$ = HIGH and disabled with $\overline{B}_0$ = LOW. With C4 enabled, a half channel offset can be programmed with input $\overline{B}_1$ = HIGH, and no offset with $\overline{B}_1$ = LOW.

FEEDBACK TO PRESCALERS (see also Figs 5 and 6)

The counters C1, C0, C–1 and C–2 are side-steppable counters, i.e. its division ratio may be increased by one, by applying a pulse to a control terminal for the duration of one division cycle. Counter C2 has 10 states, which are accessible as timing signals for the rate selectors RS1 to RS4. A rate selector, programmed with n (n_1 to n_4 in the U.D.) generates n of 10 basic timing periods an active signal. Since $n \leq 9$, 1 of 10 periods is always non-active. In this period RS1 transfers the output of rate selector RS0, which is timed by counter C3 and programmed with n_0. Similarly, RS0 transfers RSH output during one period of C3. Rate selector RSH is timed by C4 and programmed with n_h. In one of the two states of C4, if enabled, or always, if C4 is disabled, RSH transfers the LOW active signal at input $\overline{RI}$ to RS0. If $\overline{RI}$ is not used it must be connected to HIGH. The feedback output signals of RS1, RS2 and RS3 are externally available as active LOW signals at outputs $\overline{OFB}_1$, $\overline{OFB}_2$ and $\overline{OFB}_3$.

Output $\overline{OFB}_1$ is intended for the prescaler at the highest frequency (if present), $\overline{OFB}_2$ for the next (if present) and $\overline{OFB}_3$ for the lowest frequency prescaler (if present). A prescaler needs a feedback signal, which is timed on one of its own division cycles in a basic timing period. The timing signal at $\overline{OSY}$ is LOW during the last U.D. input period of a basic timing period and is suitable for timing of the feedback for the last external prescaler. The synchronization signal for a preceding prescaler is the OR-function of the sync. input and sync. output of the following prescaler (all sync. signals active LOW).

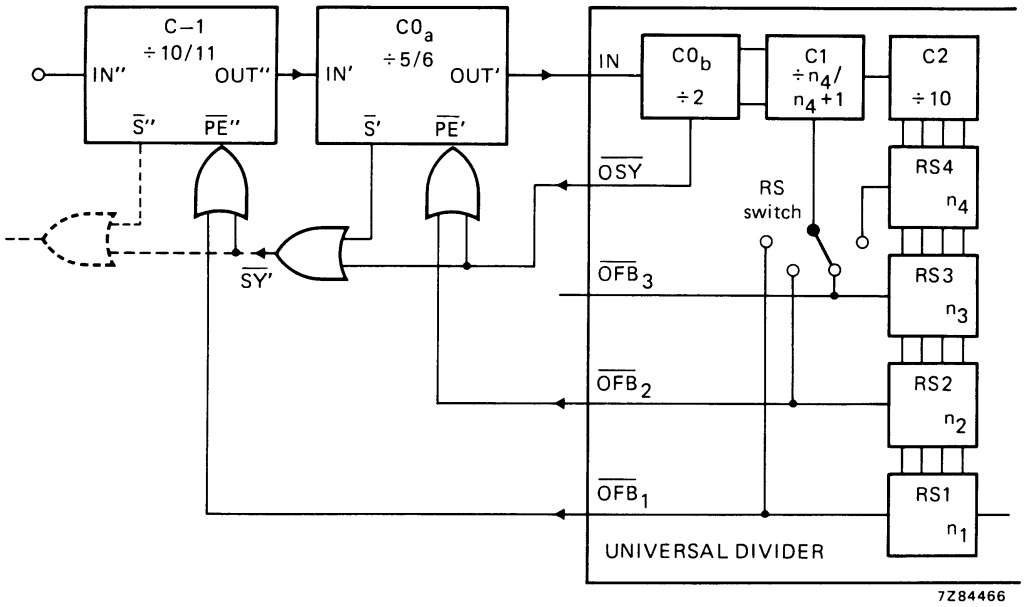


Fig.5 Block diagram showing feedback to prescalers.

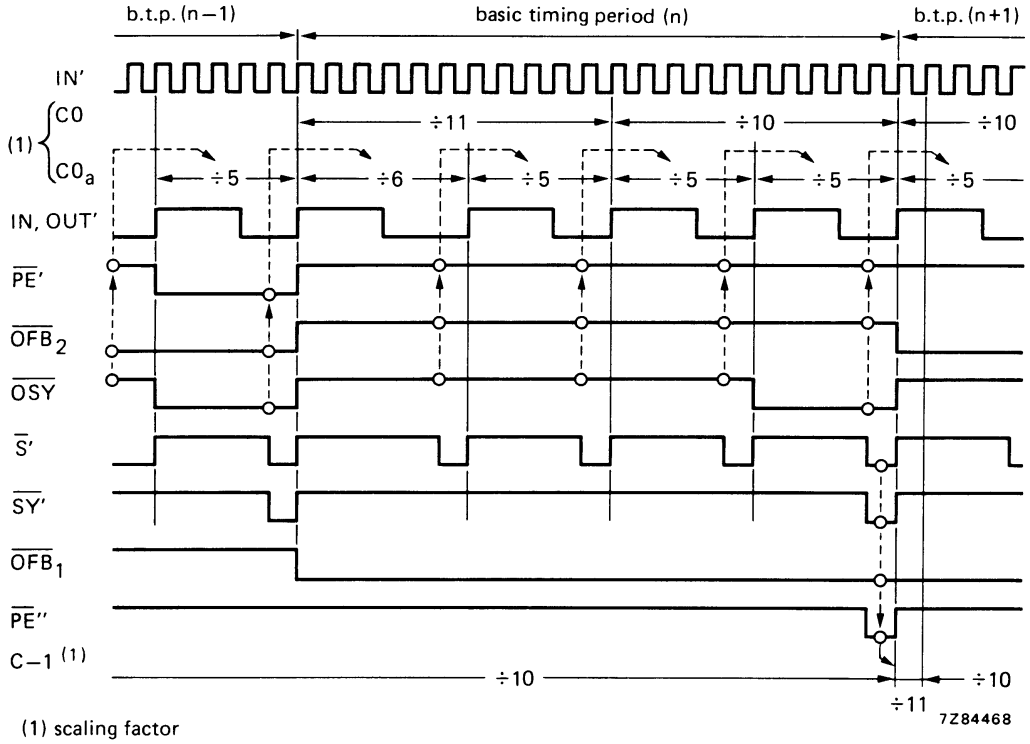


Fig.6 Timing diagram showing signals occurring in Fig.5.

CASCADING OF U.D.s (see also Fig. 8)

A U.D. is programmed into the 'slave' mode by the programme input data: $n_{2A} = 11$, $n_{2B} = 10$, $n_{3A} = n_{4A} = n_{3B} = n_{4B} = n_{5B} = 0$. A U.D. operating in the slave mode performs the function of two extra programmable stages C2' and C3' to a 'master' (not slave) mode operating U.D. More slave U.D.s may be used, every slave adding two lower significant digits to the system.

Output $\overline{OFB}_3$ is converted to the borrow output of the programme data subtractor, which is valid after fetch period 5. Input SI is the borrow input (both in master and in slave mode), which has to be valid in fetch period 0. Input SI has to be connected to output $\overline{OFB}_3$ of a following slave, if not present, to LOW. For proper transfer of the borrow from a lower to a higher significant U.D. subtractor, the U.D.s have to be programmed sequentially in order of significance or synchronously if the programme is repeated at least the number of U.D.s in the system.

Rate input $\overline{RI}$ and output OFS must be connected to rate output $\overline{OFB}_1$ and the input IN of the next slave U.D. The combination thus formed retains the full programmability and features of one U.D.

OUTPUT (see also Fig.7**)**

The normal output of the U.D. is the slow output OFS, which consists of evenly spaced LOW pulses. This output is intended for accurate phase comparison. If a better frequency acquisition time is required, the fast output OFF can be used. The output frequency on OFF is a factor $M \cdot H$ higher than the frequency on OFS. However, phase jitter of maximum $\pm$ 1 system input period occurs at OFF, since the division ratio of the counters preceding OFF are varied by slow feedback pulse trains from rate selectors following OFF.

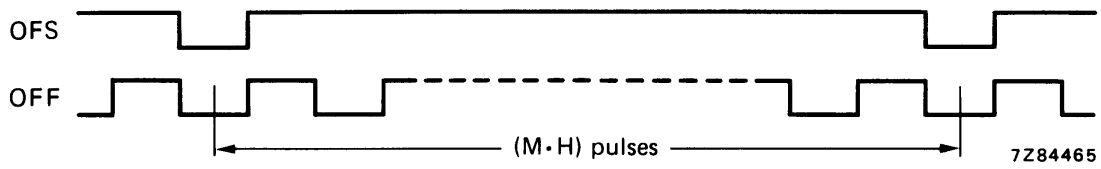


Fig.7 Timing diagram showing output pulses.

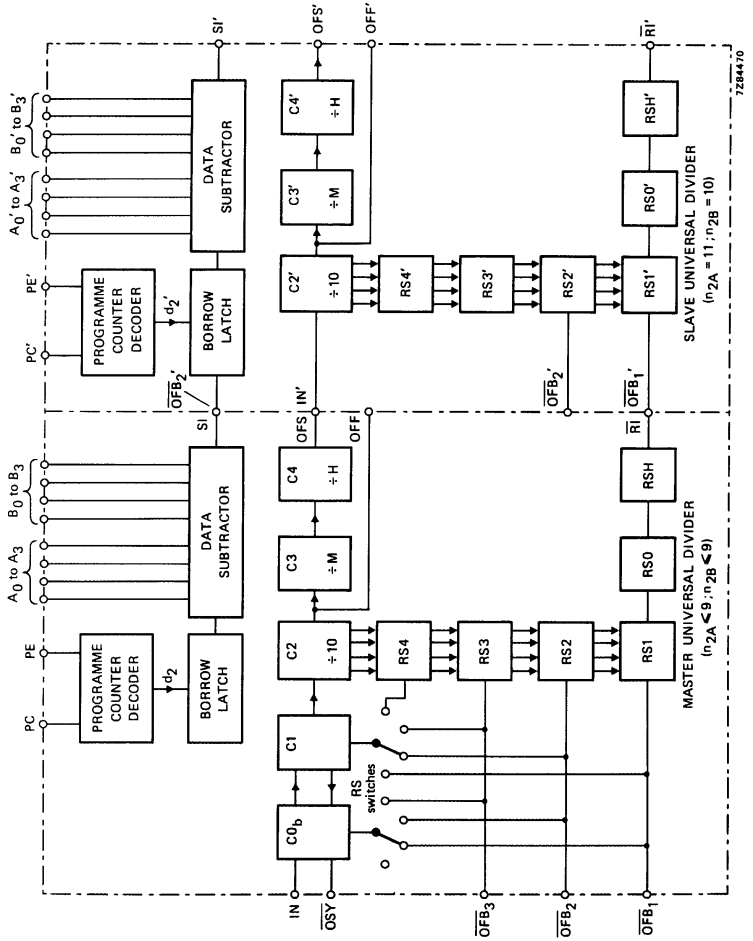


Fig.8 Block diagram showing cascading of U.Ds.

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)						
					−40		+ 25		+ 85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (sink)	4,75		0,4		1,6		1,4		1,1		mA
current LOW	5		0,4	I_{OL}	1,7		1,5		1,2		mA
	10		0,5		2,9		2,7		2,2		mA
Output (source)	5	4,6			1,0		0,85		0,55		mA
current HIGH	5	2,5			3,0		2,5		1,7		mA
	10	9,5		$-I_{OH}$	3,0		2,5		1,7		mA

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

PARAMETER	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Propagation delay	5	t_{PHL}		135	270	ns	C_L = 10 pF
IN → $\overline{OSY}$	10			45	90	ns	
HIGH to LOW							
Output transition times							
HIGH to LOW	5	t_{THL}		30	60	ns	C_L = 50 pF
	10			12	25	ns	
LOW to HIGH	5	t_{TLH}		45	90	ns	C_L = 50 pF
	10			20	40	ns	
Maximum input	5	f_{max}	4	8		MHz	δ = 50%
frequency; IN	10		12	24		MHz	$C0_b$ ratio > 1
Maximum input	5	f_{max}	2	4		MHz	δ = 50%
frequency; IN	10		6	12		MHz	$C0_b$ ratio = 1
Maximum input	5	f_{max}	0,15	0,3		MHz	
frequency; PC	10		0,5	1,0		MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,400\ f_i + \sum (f_o C_L) \times V_{DD}^2$	