

# DATA SHEET

## **FBL22041**

**3.3V BTL 7-bit Futurebus + transceiver  
(standard A-port)**

Product specification  
Supersedes data of 1998 Feb 02  
IC23 Data Handbook

1998 Aug 12

## 3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL22041

## FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10 $\Omega$ .
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low I<sub>CC</sub> current

- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port
- The A port includes a series resistor of 30 $\Omega$  making external terminating resistors unnecessary

## DESCRIPTION

The FBL22041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FBL22041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The FBL22041 is designed with a 30 $\Omega$  series resistance in both the HIGH and LOW states of the output.

The FBL22041 is pin and function compatible with FB2041 but operates at a 3.3V supply voltage, greatly reducing power consumption.

## QUICK REFERENCE DATA

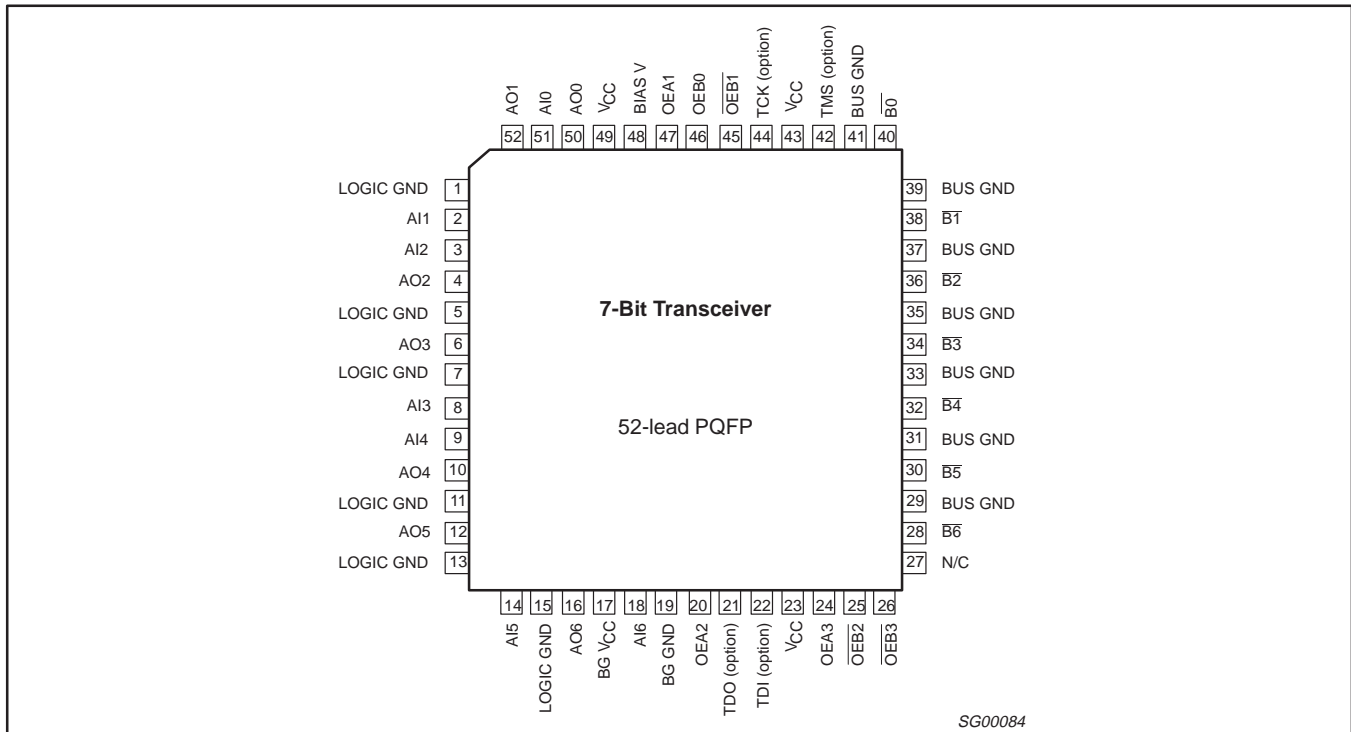
SYMBOL	PARAMETER	TYPICAL	UNIT	
t <sub>PLH</sub>	Propagation delay	4.1	ns	
t <sub>PHL</sub>	AIn to $\overline{Bn}$	3.6		
t <sub>PLH</sub>	Propagation delay	5.2	ns	
t <sub>PHL</sub>	$\overline{Bn}$ to AOn	5.1		
C <sub>OB</sub>	Output capacitance ( $\overline{B0}$ - $\overline{B6}$ only)	6	pF	
I <sub>OL</sub>	Output current ( $\overline{B0}$ - $\overline{B6}$ only)	100	mA	
I <sub>CC</sub>	Supply Current	Standby	6.0	mA
		AIn to $\overline{Bn}$ (outputs Low or High)	5.1	
		$\overline{Bn}$ to AOn (outputs Low)	13.4	
		$\overline{Bn}$ to AOn (outputs High)	10.6	

## ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V <sub>CC</sub> = 3.3V $\pm$ 10%; T <sub>amb</sub> = 0 to +70°C	DWG No.
52-pin Plastic Quad Flatpack	FBL22041BB	SOT379-1

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The B-port interfaces to "Backplane Transceiver Logic" (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/ $\overline{OEB1}$ , output drivers for bits 1–2–3 are enabled with OEA2/ $\overline{OEB2}$  and output drivers for bits 4–5–6 are enabled with OEA3/ $\overline{OEB3}$ .

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when V<sub>CC</sub> is below 1.3V.

The B-port has an output enable, OEB0, which affects all seven drivers. When OEB0 is High and  $\overline{OEBn}$  is Low the output driver will be enabled. When OEB0 is Low or if  $\overline{OEBn}$  is High, the B-port drivers will be inactive and at the level of the backplane signal.

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**PIN DESCRIPTION**

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
ai0 – ai6	51, 2, 3, 8, 9, 14, 18	Input	Data inputs (TTL)
aO0 – aO6	50, 52, 4, 6, 10, 12, 16	Output	3-state outputs (TTL)
b $\bar{0}$ – b $\bar{6}$	40, 38, 36, 34, 32, 30, 28	i/o	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the Bn outputs when High
OEB1	45	Input	Enables the B0 output when Low
OEB2	25	Input	Enables the B1 – B3 outputs when Low
OEB3	26	Input	Enables the B4 – B6 outputs when Low
OEA1	47	Input	Enables the A0 outputs when High
OEA2	20	Input	Enables the A1 – A3 outputs when High
OEA3	24	Input	Enables the A4 – A6 outputs when High
bus gnd	41, 39, 37, 35, 33, 31, 29	GND	Bus ground (0V)
LOGIC gnd	1, 5, 7, 11, 13, 15	GND	Logic ground (0V)
LOGIC/bus V <sub>CC</sub>	23, 43, 49	Power	Positive supply voltage
BG V <sub>CC</sub>	17	Power	Positive supply voltage BAND GAP
BIAS V	48	Power	Positive supply voltage
TMS	42	Input	Test Mode Select (no-connect)
Tck	44	Input	Test Clock (no-connect)
Tdi	22	Input	Test Data In (shorted to TDO)
Tdo	21	Output	Test Data Out (TDI)
BG GND	19	GND	BAND GAP GROUND (0V)

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## FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	Bn*	OEB0	OEB1	OEB2	OEB3	OEA1	OEA2	OEA3	AOn	Bn*
AIn to Bn	L	—	H	L	L	L	L	L	L	Z	H**
	H	—	H	L	L	L	L	L	L	Z	L
	L	—	H	L	L	L	H	H	H	L	H**
	H	—	H	L	L	L	H	H	H	H	L
AI0 to B0	L	—	H	L	X	X	L	L	L	Z	H**
	H	—	H	L	X	X	L	L	L	Z	L
	L	—	H	L	X	X	H	H	H	L	H**
	H	—	H	L	X	X	H	H	H	H	L
AI1 – AI3 to B1 – B3	L	—	H	X	L	X	L	L	L	Z	H**
	H	—	H	X	L	X	L	L	L	Z	L
	L	—	H	X	L	X	H	H	H	L	H**
	H	—	H	X	L	X	H	H	H	H	L
AI4 – AI6 to B4 – B6	L	—	H	X	X	L	L	L	L	Z	H**
	H	—	H	X	X	L	L	L	L	Z	L
	L	—	H	X	X	L	H	H	H	L	H**
	H	—	H	X	X	L	H	H	H	H	L
Disable Bn outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	H	H	X	X	X	X	H**
Disable B0 outputs	X	X	H	H	X	X	X	X	X	X	H**
Disable B1 – B3 outputs	X	X	H	X	H	X	X	X	X	X	H**
Disable B4 – B6 outputs	X	X	H	X	X	H	X	X	X	X	H**
Bn to AOn	X	L	L	X	X	X	H	H	H	H	Input
	X	H	L	X	X	X	H	H	H	L	Input
	X	L	X	H	H	H	H	H	H	H	Input
	X	H	X	H	H	H	H	H	H	L	Input
B0 to AO0	X	L	L	X	X	X	H	X	X	H	Input
	X	H	L	X	X	X	H	X	X	L	Input
	X	L	X	H	H	H	H	X	X	H	Input
	X	H	X	H	H	H	H	X	X	L	Input
B1 – B3 to AO1 – AO3	X	L	L	X	X	X	X	H	X	H	Input
	X	H	L	X	X	X	X	H	X	L	Input
	X	L	X	H	H	H	X	H	X	H	Input
	X	H	X	H	H	H	X	H	X	L	Input
B4 – B6 to AO4 – AO6	X	L	L	X	X	X	X	X	H	H	Input
	X	H	L	X	X	X	X	X	H	L	Input
	X	L	X	H	H	H	X	X	H	H	Input
	X	H	X	H	H	H	X	X	H	L	Input
Disable AOn outputs	X	X	X	X	X	X	L	L	L	Z	X
Disable AO0 outputs	X	X	X	X	X	X	L	X	X	Z	X
Disable AO1 – AO3 outputs	X	X	X	X	X	X	X	L	X	Z	X
Disable AO4 – AO6 outputs	X	X	X	X	X	X	X	X	L	Z	X

## NOTES:

H = High voltage level

L = Low voltage level

X = Don't care

Z = High-impedance (OFF) state

— = Input not externally driven

H\*\* = Goes to level of pull-up voltage

B\* = Precaution should be taken to ensure B inputs do not float.  
If they do, they are equal to Low state.

Z = High-impedance (OFF) state

— = Input not externally driven

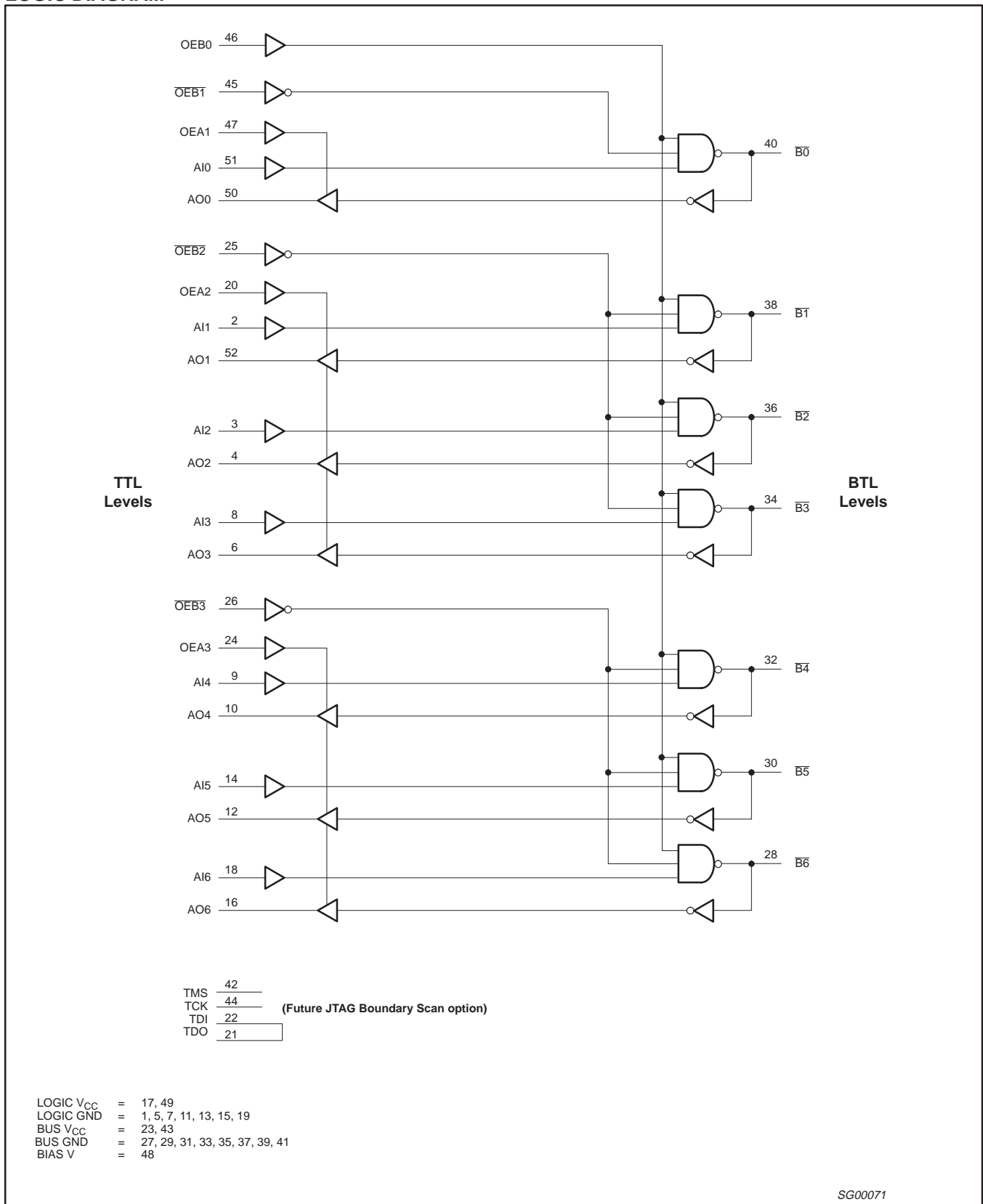
H\*\* = Goes to level of pull-up voltage

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LOGIC DIAGRAM



## 3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

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**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +4.6	V
$V_{IN}$	Input voltage	A10 – A16, OE $\overline{B}$ 0, $\overline{OEB}$ n, OEAn	-0.5 to +7.0	V
		$\overline{B}$ 0 – $\overline{B}$ 6	-0.5 to +3.5	
$I_{IN}$	Input current	$V_{IN} < 0$	-50	
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to +7.0	V
$I_{OUT}$	Current applied to output in Low output state/High output state	A00 – A06	48, -24	mA
		$\overline{B}$ 0 – $\overline{B}$ 6	200	
$T_{STG}$	Storage temperature		-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER		COMMERCIAL LIMITS $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = 0$ to $+70^\circ\text{C}$			UNIT
			MIN	TYP	MAX	
$V_{CC}$	Supply voltage		3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage	Except $\overline{B}$ 0– $\overline{B}$ 6	2.0			V
		$\overline{B}$ 0 – $\overline{B}$ 6	1.62	1.55		
$V_{IL}$	Low-level input voltage	Except $\overline{B}$ 0– $\overline{B}$ 6			0.8	V
		$\overline{B}$ 0 – $\overline{B}$ 6			1.47	
$I_{IK}$	Input clamp current				-18	mA
$I_{OH}$	High-level output current	A00 – A06			-12	mA
$I_{OL}$	Low-level output current	A00 – A06			12	mA
		$\overline{B}$ 0 – $\overline{B}$ 6			100	
$C_{OB}$	Output capacitance on B port			6	7	pF
$T_{amb}$	Operating free-air temperature range		0		+70	°C

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## LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	TYP	MAX	
$V_{BIASV}$	Bias pin voltage	Voltage difference between the Bias voltage and $V_{CC}$ after the PCB is plugged in.	-	-	0.5	V
$I_{BIASV}$	Bias pin ( $I_{BIASV}$ ) input DC current	$V_{CC} = 0\text{ V}$ , Bias $V = 3.6\text{ V}$			1.2	mA
		$V_{CC} = 3.3\text{ V}$ , Bias $V = 3.6\text{ V}$			10	$\mu\text{A}$
$\overline{V_{Bn}}$	Bus voltage during prebias	$\overline{B0} - \overline{B8} = 0\text{ V}$ , Bias $V = 3.3\text{ V}$	1.62		2.1	V
$I_{LM}$	Fall current during prebias	$\overline{B0} - \overline{B8} = 2\text{ V}$ , Bias $V = 1.3$ to $2.5\text{ V}$			1	$\mu\text{A}$
$I_{HM}$	Rise current during prebias	$\overline{B0} - \overline{B8} = 1\text{ V}$ , Bias $V = 3$ to $3.6\text{ V}$	-1			$\mu\text{A}$
$\overline{I_{BnPEAK}}$	Peak bus current during insertion	$V_{CC} = 0$ to $3.3\text{ V}$ , $\overline{B0} - \overline{B8} = 0$ to $2.0\text{ V}$ , Bias $V = 2.7$ to $3.6\text{ V}$ , $OEB0 = 0.8\text{ V}$ , $t_r = 2\text{ ns}$			10	mA
$I_{OLOFF}$	Power up current	$V_{CC} = 0$ to $3.3\text{ V}$ , $OEB0 = 0.8\text{ V}$			100	$\mu\text{A}$
		$V_{CC} = 0$ to $1.2\text{ V}$ , $OEB0 = 0$ to $5\text{ V}$			100	
$t_{GR}$	Input glitch rejection	$V_{CC} = 3.3\text{ V}$	1.0	1.35		ns

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
$I_{OH}$	High level output current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 1.9\text{ V}$			100	$\mu\text{A}$
$I_{OFF}$	Power-off output current	$\overline{B0} - \overline{B6}$	$V_{CC} = 0\text{ V}$ , $V_{IL} = \text{MAX}$ , $V_{OH} = 1.9\text{ V}$			100	$\mu\text{A}$
$V_{OH}$	High-level output voltage	AO0 – AO6 <sup>3</sup>	$V_{CC} = \text{MIN}$ to $\text{MAX}$ ; $I_{OH} = -100\mu\text{A}$	$V_{CC}$			V
			$V_{CC} = \text{MIN}$ ; $I_{OH} = -4\text{ mA}$	2.4			V
			$V_{CC} = \text{MIN}$ ; $I_{OH} = -12\text{ mA}$	2.0			V
$V_{OL}$	Low-level output voltage	AO0 – AO6 <sup>3</sup>	$V_{CC} = \text{MIN}$ ; $I_{OL} = 4\text{ mA}$			0.4	V
			$V_{CC} = \text{MIN}$ ; $I_{OL} = 12\text{ mA}$			0.8	V
		$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MIN}$ , $I_{OL} = 4\text{ mA}$	0.5			V
			$V_{CC} = \text{MIN}$ , $I_{OL} = 100\text{ mA}$	0.75	1.0	1.20	V
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}$ , $I_I = I_{IK} = -18\text{ mA}$		-0.85	-1.2	V
$I_I$	Input leakage current	Control pins	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND			$\pm 1.0$	$\mu\text{A}$
		Control/A10 – A16	$V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$			10	
		A10 – A16	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$			1	
		Note 4	$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$			-5	
$I_{IH}$	High-level input current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_I = 1.9\text{ V}$			100	$\mu\text{A}$
			$V_{CC} = \text{MAX}$ , $V_I = 3.5\text{ V}$ , note 5	100			mA
			$V_{CC} = \text{MAX}$ , $V_I = 3.75\text{ V}$ @ $-40^\circ\text{C}$	100			mA
$I_{IL}$	Low-level input current	$\overline{B0} - \overline{B6}$	$V_{CC} = \text{MAX}$ , $V_I = 0.75\text{ V}$			-100	$\mu\text{A}$
$I_{OZH}$	Off-state output current	AO0 – AO6	$V_{CC} = \text{MAX}$ , $V_O = 3\text{ V}$			5	$\mu\text{A}$
$I_{OZL}$	Off-state output current	AO0 – AO6	$V_{CC} = \text{MAX}$ , $V_O = 0.5\text{ V}$			-5	$\mu\text{A}$
$I_{CC}$	Supply current (total)	$I_{CCZ}$ (standby)	$V_{CC} = \text{MAX}$		6.0	13.0	mA
		$I_{CCB}$ , A1n to $\overline{Bn}$	$V_{CC} = \text{MAX}$ , outputs Low or High		5.1	10.0	
		$I_{CCA}$ , $\overline{Bn}$ to AOn	$V_{CC} = \text{MAX}$ , outputs Low		13.4	19.5	
		$I_{CCA}$ , $\overline{Bn}$ to AOn	$V_{CC} = \text{MAX}$ , outputs High		10.6	16.0	

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .
- Due to test equipment limitations, actual test conditions are  $V_{IH} = 1.8\text{ V}$  and  $V_{IL} = 1.3\text{ V}$  for the B side.
- Unused pins are at  $V_{CC}$  or GND.
- For B port input voltage between 3 and 5 volt;  $I_{IH}$  will be greater than 100mA but the part will continue to function normally (clamping circuit is active).



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## AC ELECTRICAL CHARACTERISTICS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, R_L = 500\Omega$			$T_{amb} = 0 \text{ to } 70^{\circ}\text{C}, V_{CC} = 3.3\text{V}\pm 10\%, C_L = 50\text{pF}, R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay, $\overline{Bn}$ to AOn	Waveform 1, 2	4.2 4.1	5.2 5.1	6.2 6.1	3.9 3.9	7.0 6.8	ns
$t_{PZH}$ $t_{PZL}$	Output enable time, OEA to AOn	Waveform 4, 5	5.8 2.7	7.1 4.5	8.5 8.0	5.4 2.5	9.4 8.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output disable time, OEA to AOn	Waveform 4, 5	3.9 3.7	5.2 4.8	6.5 6.0	3.6 3.3	7.0 7.3	ns
$t_{TLH}$ $t_{THL}$	Transition time, AOn Port (10% to 90% or 90% to 10%)	Test Circuit and Waveforms	0.8 0.6	1.6 1.1	2.8 1.7	0.7 0.5	3.0 2.0	ns
$t_{sk(o)}$	Output skew between receivers in same package <sup>1</sup>	Waveform 3		0.4	1.5		1.5	ns
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V}, C_D = 30\text{pF}, R_U = 9\Omega$			$T_{amb} = 0 \text{ to } 70^{\circ}\text{C}, V_{CC} = 3.3\text{V}\pm 10\%, C_D = 30\text{pF}, R_U = 9\Omega$		
			MIN	TYP	MAX	MIN	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.2 2.9	4.1 3.6	5.0 4.4	2.9 2.7	5.8 4.9	ns
$t_{PLH}$ $t_{PHL}$	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.9 3.5	4.7 4.4	5.5 5.4	3.5 3.2	6.4 5.9	ns
$t_{PLH}$ $t_{PHL}$	Enable/disable time, OEB1 to $\overline{Bn}$	Waveform 1	4.1 3.0	5.0 3.9	5.9 4.8	3.8 2.6	6.6 5.5	ns
$t_{TLH}$ $t_{THL}$	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{sk(o)}$	Output skew between drivers in same package <sup>1</sup>	Waveform 3		0.3	1.4		1.4	ns
SYMBOL	PARAMETER	TEST CONDITION	$R_U = 16.5\Omega$			$R_U = 16.5\Omega$		UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay, AIn to $\overline{Bn}$	Waveform 1, 2	3.2 2.9	4.1 3.6	5.0 4.9	2.9 2.6	5.8 4.9	ns
$t_{PLH}$ $t_{PHL}$	Enable/disable time, OEB0 to $\overline{Bn}$	Waveform 2	3.9 3.5	4.7 4.4	5.5 5.4	3.5 3.2	6.4 5.9	ns
$t_{PLH}$ $t_{PHL}$	Enable/disable time, OEB1 to $\overline{Bn}$	Waveform 1	4.1 3.0	5.0 3.9	5.9 4.8	3.8 2.6	6.6 5.5	ns
$t_{TLH}$ $t_{THL}$	Transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms	1.3 0.4	1.9 0.8	2.8 1.4	1.2 0.4	3.0 1.5	ns
$t_{sk(o)}$	Output skew between drivers in same package <sup>1</sup>	Waveform 3		0.3	1.4		1.4	ns

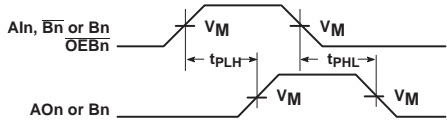
## NOTES:

- $|t_{pN\text{actual}} - t_{pM\text{actual}}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature,  $V_{CC}$ , loading, etc.).

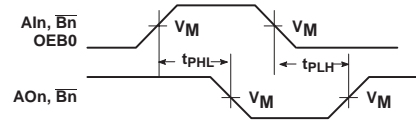
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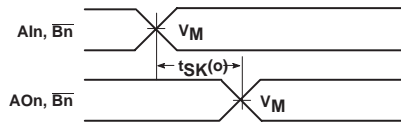
AC WAVEFORMS



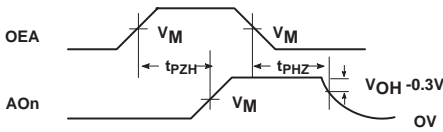
Waveform 1. Propagation Delay for Data or Output Enable to Output



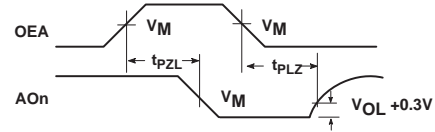
Waveform 2. Propagation Delay for Data or Output Enable to Output



Waveform 3. Output Skews



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

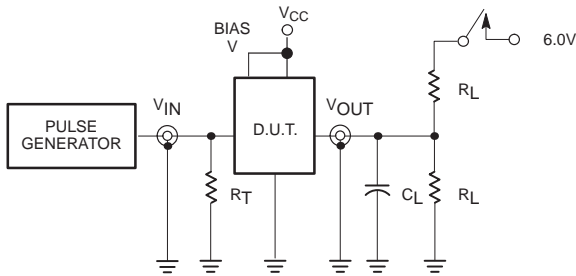
NOTE:  $V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others.

SG00086

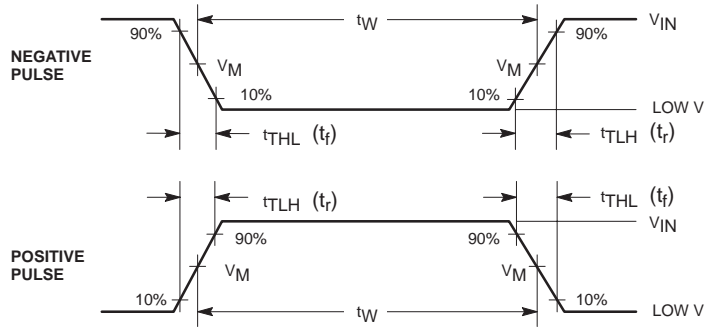
# 3.3V BTL 7-bit Futurebus+ transceiver (standard A-port)

FBL22041

## TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs on A Port



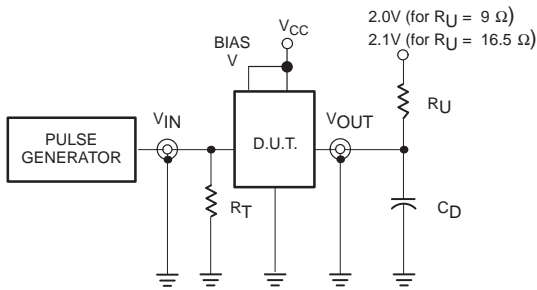
$V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others.

### Input Pulse Definitions

### SWITCH POSITION FOR ALL A-PORTS

TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	OPEN
$t_{PLZ}$ , $t_{PZL}$	CLOSED
$t_{PHZ}$ , $t_{PZH}$	GND

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	$t_W$	$t_{TLH}$	$t_{THL}$
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.5ns	2.5ns



Test Circuit for Outputs on B Port

### DEFINITIONS:

- $R_L$  = Load Resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.
- $C_D$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_U$  = Pull up resistor; see AC CHARACTERISTICS for value.

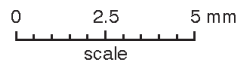
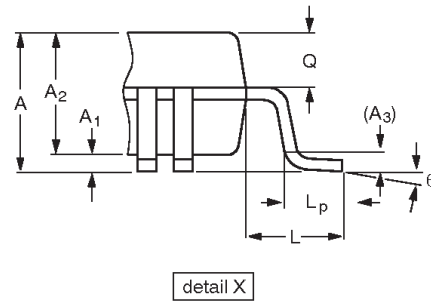
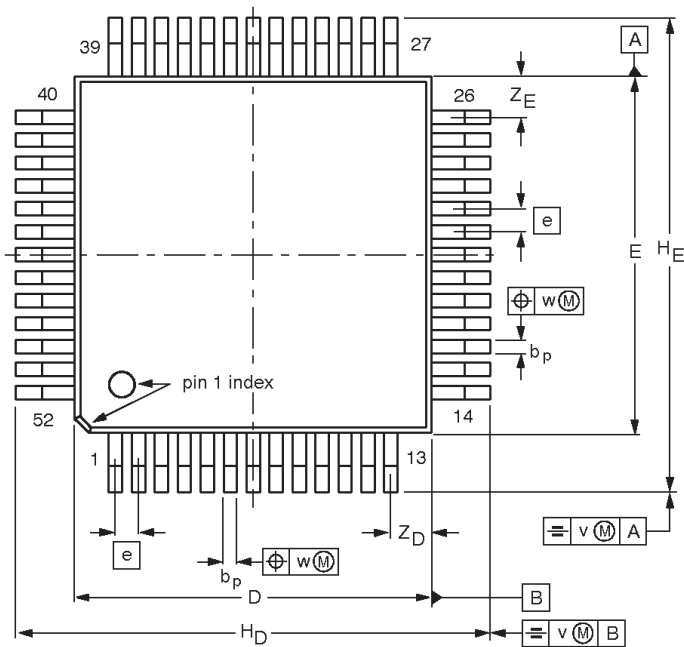
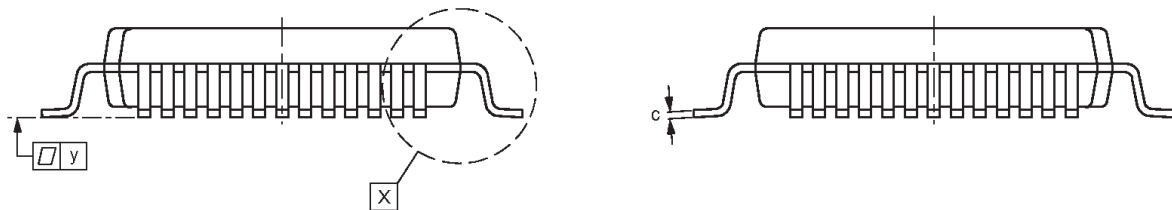
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3.3V BTL 7-bit Futurebus + transceiver (standard A-port)

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**QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm**

**SOT379-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	1.05 0.90	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1		MO-108				95-02-04

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3.3V BTL 7-bit Futurebus + transceiver (standard A-port)

FBL22041

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**NOTES**

## 3.3V BTL 7-bit Futurebus + transceiver (standard A-Port)

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**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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