INTEGRATED CIRCUITS

DATA SHEET

SSTL16877

14-bit SSTL_2 registered driver with differential clock inputs

Product specification
Supersedes data of 2000 Apr 11

2000 Apr 20

Philips Semiconductors

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14-bit SSTL_2 registered driver with differential clock inputs

SSTL16877

FEATURES

- Stub-series terminated logic for 2.5 V VDDQ (SSTL_2)
- Optimized for DDR (Double Data Rate) SDRAM applications
- Supports SSTL_2 signal inputs and outputs
- Flow-through architecture optimizes PCB layout
- Meets SSTL_2 class I and class II specifications
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Full DDR solution provided when used with PCK877 and CBT3867

DESCRIPTION

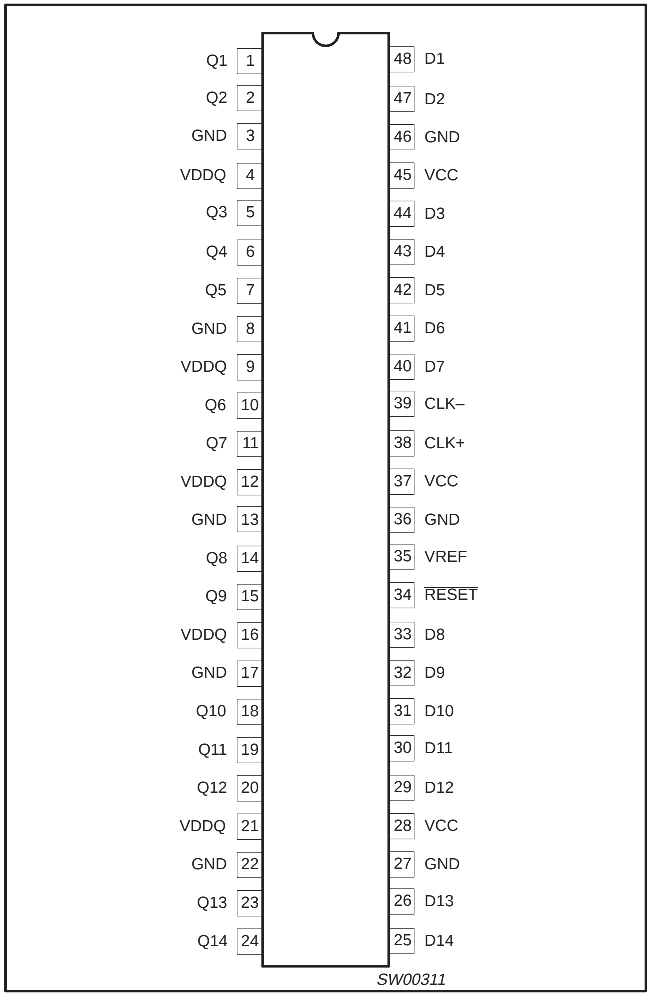
The SSTL16877 is a 14-bit SSTL_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V. V_{DDQ} must not exceed V_{CC}. Inputs are SSTL_2 type with V_{REF} normally at 0.5*V_{DDQ}. The outputs support class I which can be used for standard stub-series applications or capacitive loads. Master reset ($\overline{RESET}$) asynchronously resets all registers to zero.

The SSTL16877 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM or SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 166 MHz will have a burst rate of 333 MHz. The modules require between 23 and 27 registered control and address lines, so two 14-bit wide devices will be used on each module. The SSTL16877 is intended to be used for SSTL_2 input and output signals.

The device data inputs consist of differential receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential to be compatible with DRAM devices that are installed on the DIMM. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CLK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device must support an asynchronous input pin (reset), which when held to the LOW state will assume that all registers are reset to the LOW state and all outputs drive a LOW signal as well.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay; CLK to Qn	C_L = 30 pF; V_{DDQ} = 2.5 V	2.4	ns
C_I	Input capacitance	V_{CC} = 2.5 V	2.9	pF

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacity in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

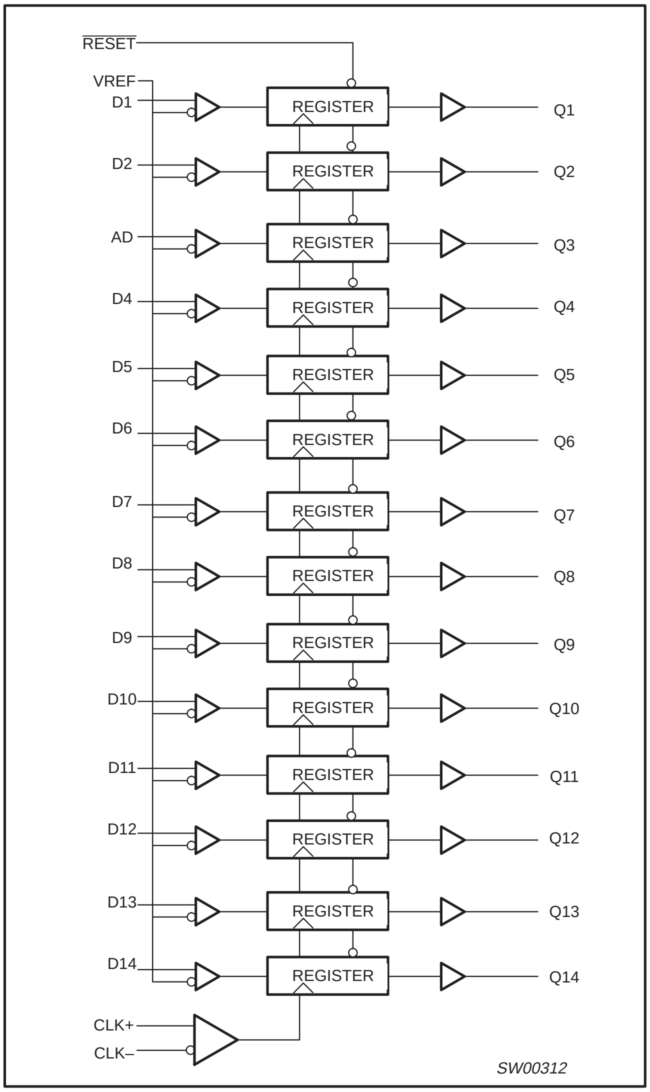
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic TSSOP Type I	0°C to +70°C	SSTL16877 DGG	SOT362-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
34	$\overline{\text{RESET}}$	LVCMOS asynchronous master reset (Active LOW)
48, 47, 44, 43, 42, 41, 40, 33, 32, 31, 30, 29, 26, 25	D1 – D14	SSTL_2 data inputs
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q1 – Q14	SSTL_2 data outputs
35	VREF	SSTL_2 input reference level
3, 8, 13, 17, 22, 27, 36, 46	GND	Ground (0 V)
28, 37, 45	V_{CC}	Positive supply voltage
4, 9, 12, 16, 21	V_{DDQ}	Output supply voltage
38 39	CLK+ CLK–	Differential clock inputs

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUT
$\overline{\text{RESET}}$	$\overline{\text{CLK}}$	CLK	D	Q
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	L or H	X	Q_0

H = High voltage level
L = High voltage level
↓ = High-to-Low transition
↑ = Low-to-High transition
X = Don't care

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		–0.5	+4.6	V
I_{IK}	DC input diode current	$V_I < 0$		–50	mA
V_I	DC input voltage[3]		–0.5	V_{DDQ} + 0.5	V
I_{OK}	DC output diode current	$V_O < 0$		–50	mA
V_{OUT}	DC output voltage[3]	Note 3	–0.5	V_{DDQ} + 0.5	V
I_{OUT}	DC output current	V_O = 0 to V_{DDQ}		±50	mA
	Continuous current[4]	V_{CC}, V_{DDQ}, or GND		±100	
T_{STG}	Storage temperature range		–65	+150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. The continuous current at V_{CC}, V_{DDQ}, or GND should not exceed ±100 mA.

RECOMMENDED OPERATING CONDITIONS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.3	2.5	2.7	V
V_{DDQ}	Output supply voltage		2.3	2.5	2.7	V
V_{REF}	Reference voltage (V_{REF} = 0.5 x V_{DDQ})		1.15	1.25	1.35	V
V_{TT}	Termination voltage		V_{REF} – 40 mV	V_{REF}	V_{REF} + 40 mV	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	AC HIGH-level input voltage	All inputs	V_{REF} + 350 mV			V
V_{IL}	AC LOW-level input voltage	All inputs			V_{REF} – 350 mV	V
V_{IH}	DC HIGH-level input voltage	All inputs	V_{REF} + 180 mV		V_{DDQ} + 0.5 V	V
V_{IL}	DC LOW-level input voltage	All inputs	V_{SS} – 0.5 V		V_{REF} – 180 mV	V
I_{OH}	HIGH-level output current				–20	mA
I_{OL}	LOW-level output current				20	mA
Tamb	Operating free-air temperature range		0		70	°C

NOTE:
1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = 0°C to +70°C MIN	TYP[2]	MAX	UNIT
V_{IK}	I/O supply voltage	V_{CC} = 2.3 V; I_I = –18 mA				–1.2	V
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 V to 2.7 V; I_{OH} = –100 µA		V_{CC} – 0.2	2.3		V
		V_{CC} = 2.3 V; I_{OH} = –8 mA		1.95	2.2		
		V_{CC} = 2.3 V; I_{OH} = –16 mA		1.95	2.1		
V_{OL}	LOW level output voltage	V_{CC} = 2.3 V to 2.7 V; I_{OL} = –100 µA			0.002	0.2	V
		V_{CC} = 2.3 V; I_{OL} = –8 mA			0.14	0.35	
		V_{CC} = 2.3 V; I_{OL} = –16 mA			0.30	0.35	
V_{CMR}	CLK, $\overline{CLK}$	Common mode range for reliable performance		0.97		1.53	V
V_{PP}	CLK, $\overline{CLK}$	Minimum peak-to-peak input to ensure logic state		360			mV
I_I	Data inputs, $\overline{RESET}$	V_{CC} = 2.7 V ; V_I = 1.7 V or 0.8 V	V_{REF} = 1.15V or 1.35V		0.01	±5	µA
		V_{CC} = 2.7 V ; V_I = 2.7 V or 0 V			0.01	±5	
	CLK, $\overline{CLK}$	V_{CC} = 2.7 V ; V_I = 1.7 V or 0.8 V	V_{REF} = 1.15V or 1.35V		0.05	±5	µA
		V_{CC} = 2.7 V ; V_I = 2.7 V or 0 V			0.05	±5	
	V_{REF}	V_{CC} = 2.7 V	V_{REF} = 1.15V or 1.35V		0.05	±5	µA
I_{CC}	Quiescent supply current CLK and $\overline{CLK}$ in opposite state[1]	V_{CC} = 2.7 V ; V_I = 1.7 V or 0.8 V			12	25	mA
		V_{CC} = 2.7 V ; V_I = 2.7 V or 0 V			10	25	

NOTES:
1. When CLK and $\overline{CLK}$ are HIGH, typical I_{CC} = 25 mA.
2. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C (unless otherwise specified).

TIMING REQUIREMENTS

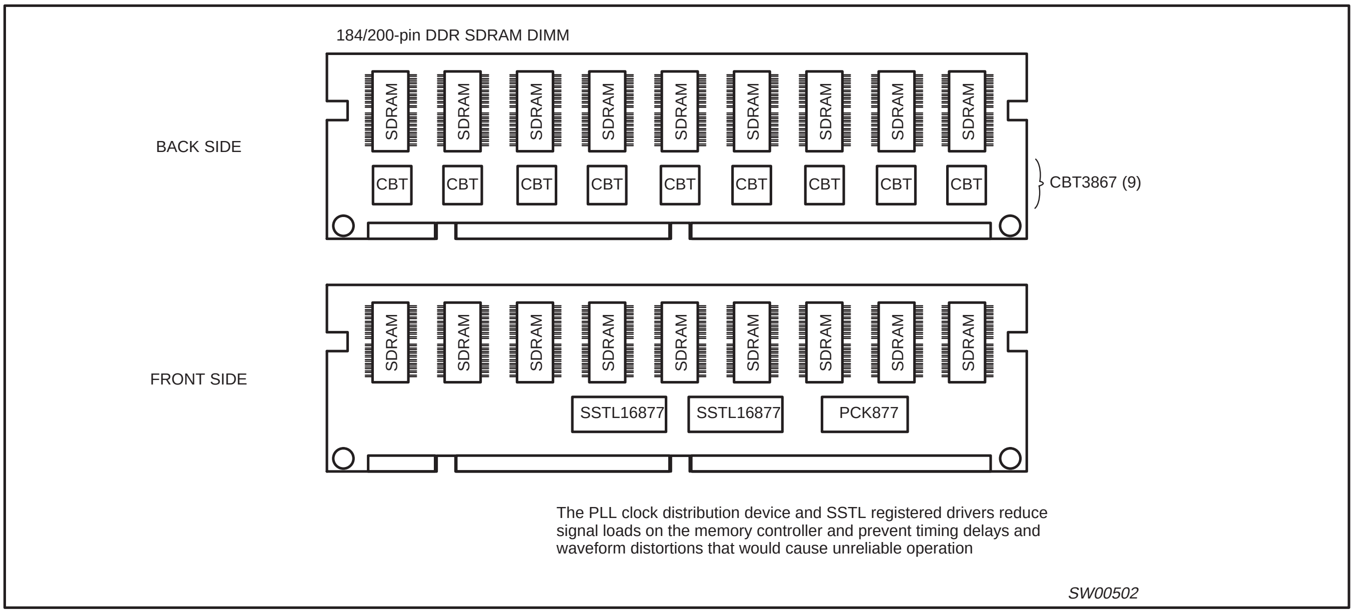
Over recommended operating conditions; T_{amb} = 0°C to +70°C (unless otherwise noted) (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS V_{CC} = 2.5 V ±0.2 V		UNIT
			MIN	MAX	
f_{clock}	Clock frequency			200	MHz
t_w	Pulse duration, CLK, $\overline{CLK}$ HIGH or LOW		1.0		ns
t_{su}	Setup time	Data before CLK↑, $\overline{CLK}$↓	0.2		ns
		$\overline{RESET}$ HIGH before CLK↑, $\overline{CLK}$↓	0.8		
t_h	Hold time		1.2		ns

SWITCHING CHARACTERISTICS

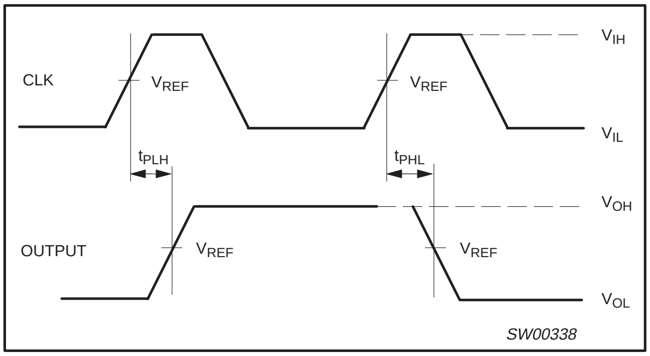
Over recommended operating conditions; T_{amb} = 0°C to +70°C; V_{DDQ} = 2.3 – 2.7 V and V_{DDQ} does not exceed V_{CC}.
Class I, V_{REF} = V_{TT} = V_{DDQ} x 0.5 and C_L = 10 pF (unless otherwise noted) (see Figure 1)

SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS V_{CC} = 2.5 V ±0.2 V		UNIT
			MIN	MAX	
f_{max}	Maximum clock frequency		200		MHz
t_{PLH}/t_{PHL}	CLK and $\overline{CLK}$	Q	1.0	3.5	ns
t_{PHL}	$\overline{RESET}$	Q	2.0	4.0	ns

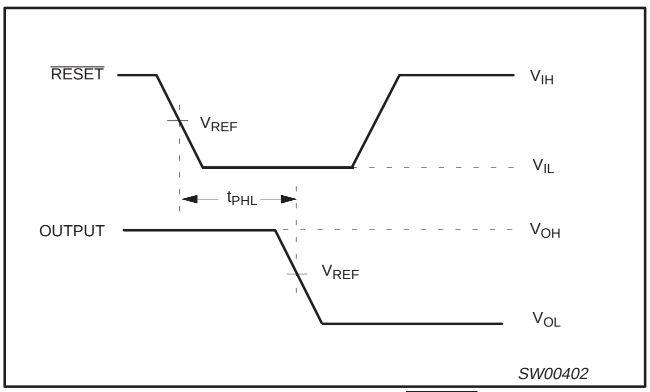


PARAMETER MEASUREMENT INFORMATION

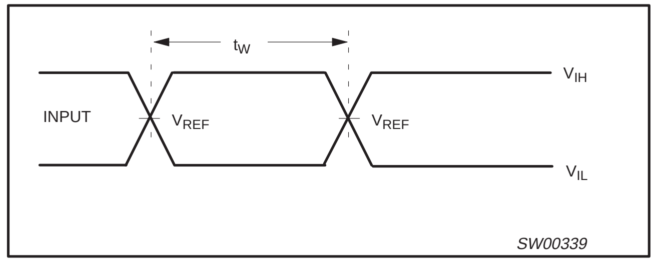
AC WAVEFORMS



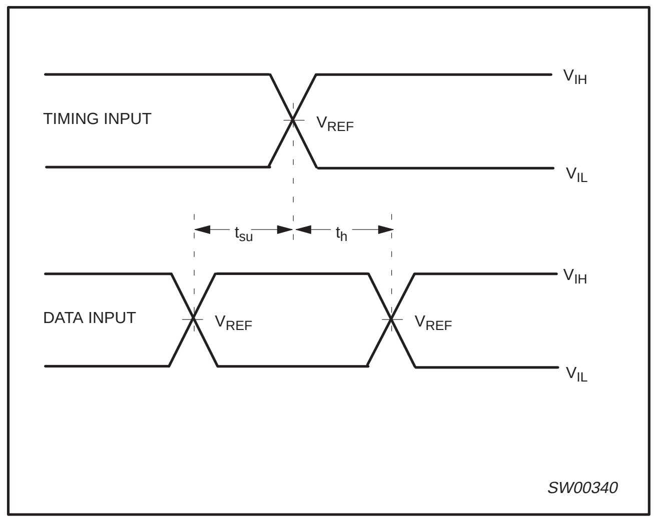
Waveform 1. Propagation delay times inverting and non-inverting outputs



Waveform 2. Propagation delay $\overline{RESET}$ to output.

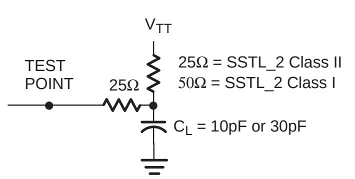


Waveform 3. Pulse duration



Waveform 4. Setup and hold times

TEST CIRCUIT



NOTES:
C_L includes probe and jig capacitance
All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10MHz, Z_O = 50Ω, t_r ≤ 1.25ns/V, t_f 1.25ns/V.
The outputs are measured one at a time with one transition per measurement.
$V_{TT} = V_{REF} = V_{DDQ} \times 0.5$

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Figure 1. Load circuitry

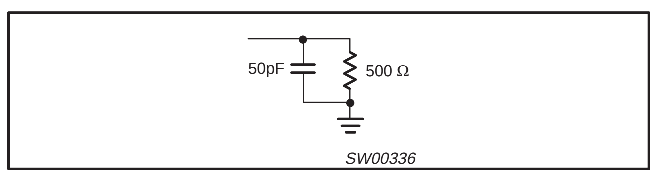


Figure 2.

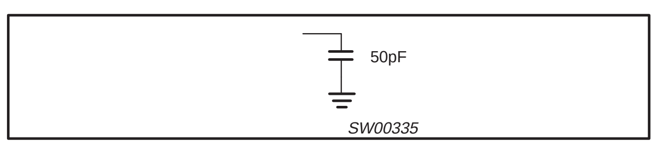
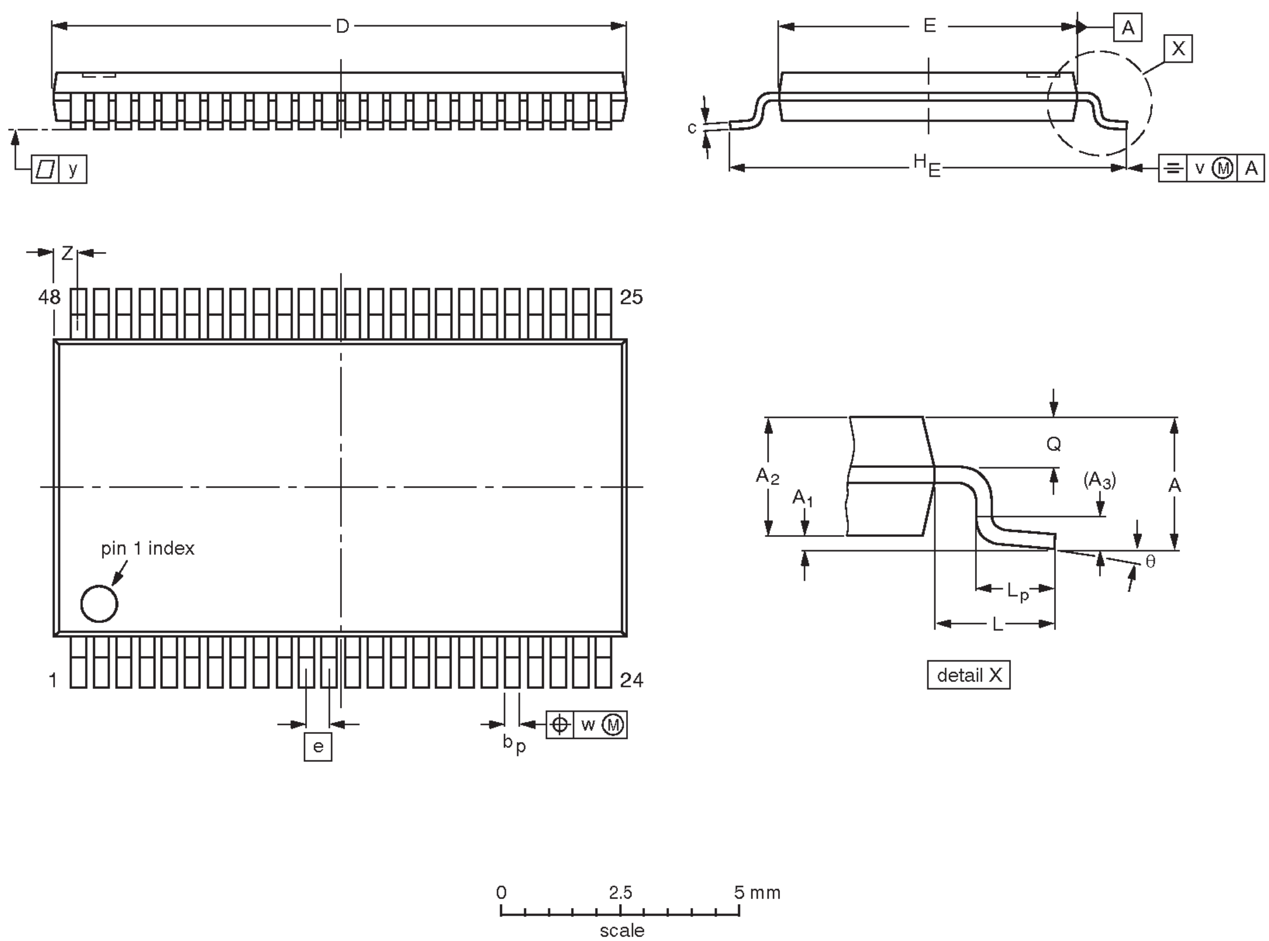


Figure 3.

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153					~~95-02-10~~ 99-12-27

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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