Three quadrant triacs high commutation

BTA204W series B and C

GENERAL DESCRIPTION

Passivated high commutation triacs in a plastic envelope suitable for surface mounting intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. These devices will commutate the full rated rms current at the maximum rated junction temperature without the aid of a snubber.
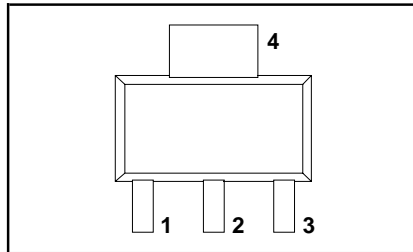
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BTA204W- **BTA204W-**	**500B** **500C**	**600B** **600C**	**800B** **800C**	
V_{DRM}	Repetitive peak off-state voltages	500	600	800	V
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	10	A

PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION

SYMBOL
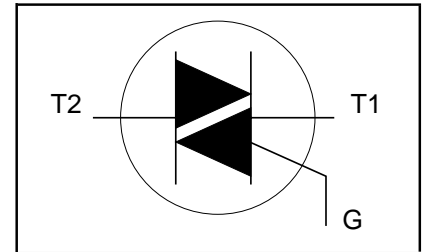
LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-500 500[1]	**-600** 600[1]	**-800** 800	V
V_{DRM}	Repetitive peak off-state voltages		-				V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108\ °C$	-	1			A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25\ °C$ prior to surge					
		t = 20 ms	-	10			A
		t = 16.7 ms	-	11			A
I^2t	I^2t for fusing	t = 10 ms	-	0.5			A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5\ A$; $I_G = 0.2\ A$; $dI_G/dt = 0.2\ A/\mu s$		100			$A/\mu s$
I_{GM}	Peak gate current		-	2			A
V_{GM}	Peak gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
T_{stg}	Storage temperature		-40	150			°C
T_j	Operating junction temperature		-	125			°C

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1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/μs.

Three quadrant triacs
high commutation

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\,j\text{-}sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\,j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint	-	156	-	K/W
		pcb mounted; pad area as in fig:2	-	70	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.		UNIT
		BTA204W-			**...B**	**...C**	
I_{GT}	Gate trigger current[2]	V_D = 12 V; I_T = 0.1 A					
		T2+ G+	-	-	50	35	mA
		T2+ G-	-	-	50	35	mA
		T2- G-	-	-	50	35	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
		T2+ G+	-	-	30	20	mA
		T2+ G-	-	-	45	30	mA
		T2- G-	-	-	30	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A	-	-	30	20	mA
V_T	On-state voltage	I_T = 2 A	-	1.2	1.5		V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A	-	0.7	1.5		V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 ˚C	0.25	0.4	-		V
I_D	Off-state leakage current	V_D = $V_{DRM(max)}$; T_j = 125 ˚C	-	0.1	0.5		mA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.		TYP.	UNIT
		BTA204W-	**...B**	**...C**		
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 ˚C; exponential waveform; gate open circuit	1000	1000	-	V/µs
dI_{com}/dt	Critical rate of change of commutating current	V_{DM} = 400 V; T_j = 125 ˚C; $I_{T(RMS)}$ = 1 A; dV_{com}/dt = 20V/µs; gate open circuit	6	3	-	A/ms
t_{gt}	Gate controlled turn-on time	I_{TM} = 12 A; V_D = $V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	-	2	µs

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2 Device does not trigger in the T2-, G+ quadrant.
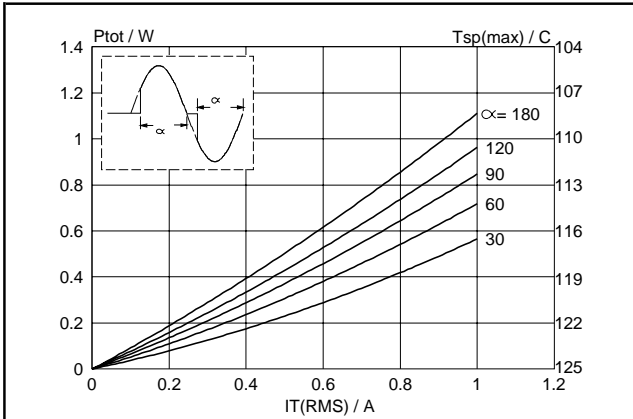
Fig.1. Maximum on-state dissipation, P_{tot}, versus rms
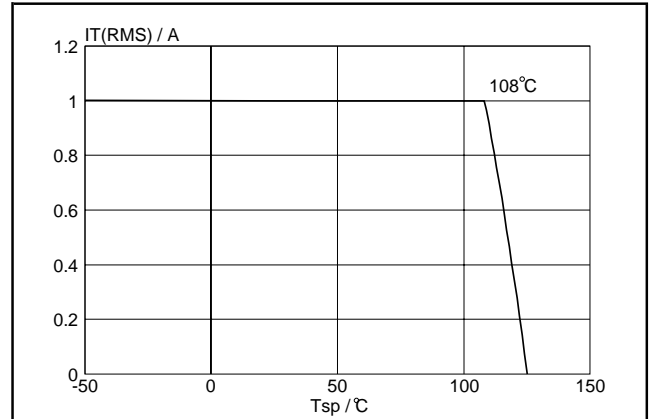on-state current, $I_{T(RMS)}$, where α = conduction angle.

Fig.4. Maximum permissible rms current $I_{T(RMS)}$,
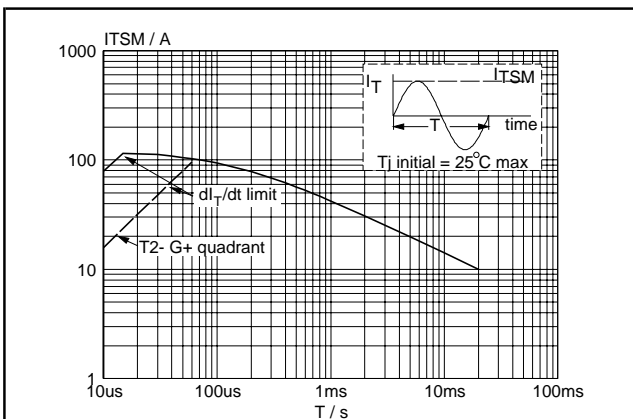versus solder point temperature T_{sp}.

Fig.2.   Maximum permissible non-repetitive peak
on-state current I_{TSM}, versus pulse width t_p, for
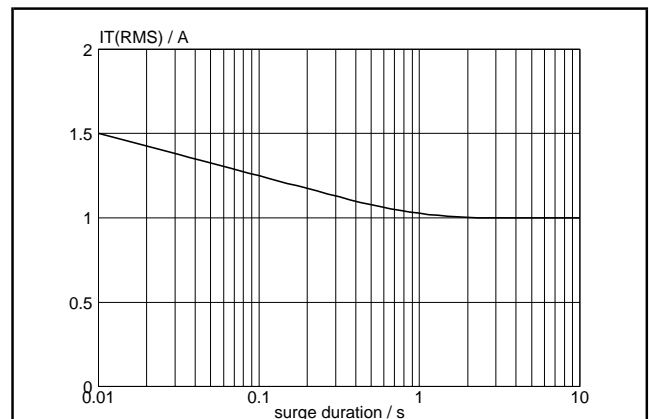sinusoidal currents, $t_p \leq 20ms$.

Fig.5.   Maximum permissible repetitive rms on-state
current $I_{T(RMS)}$, versus surge duration, for sinusoidal
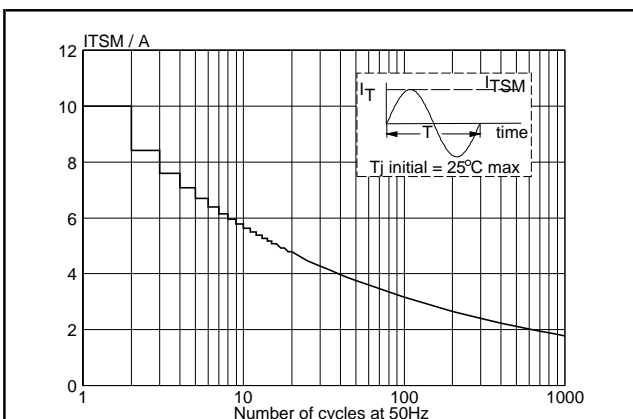currents, $f = 50$ Hz; $T_{sp} \leq 108°C$.

Fig.3. Maximum permissible non-repetitive peak
on-state current I_{TSM}, versus number of cycles, for
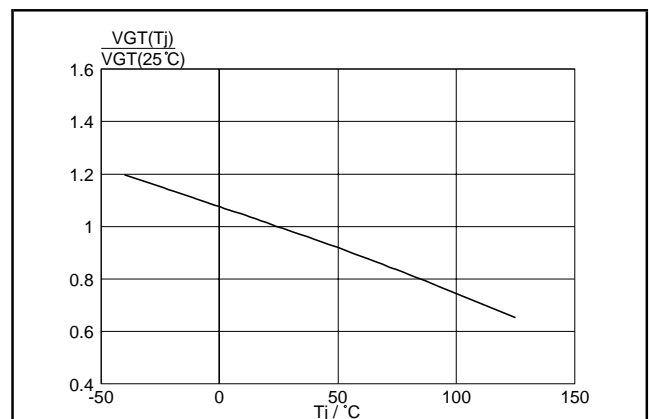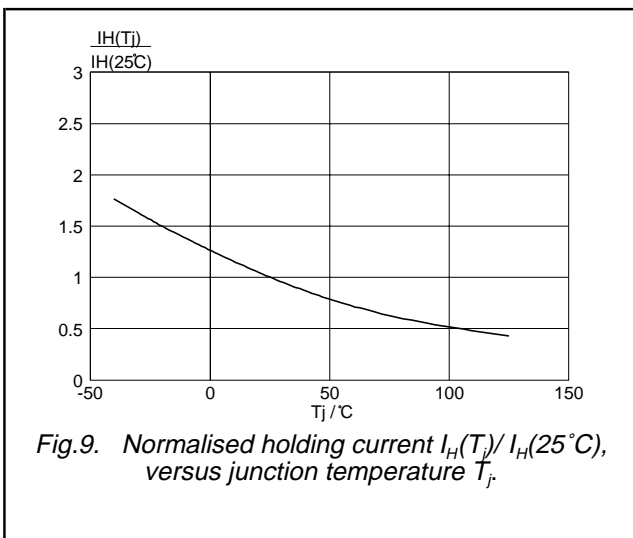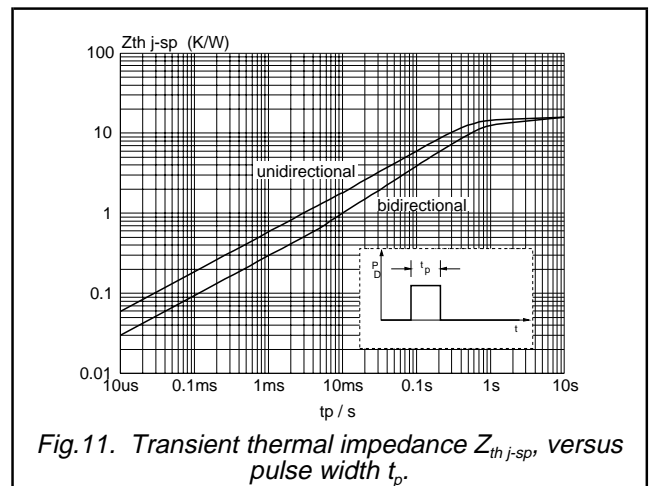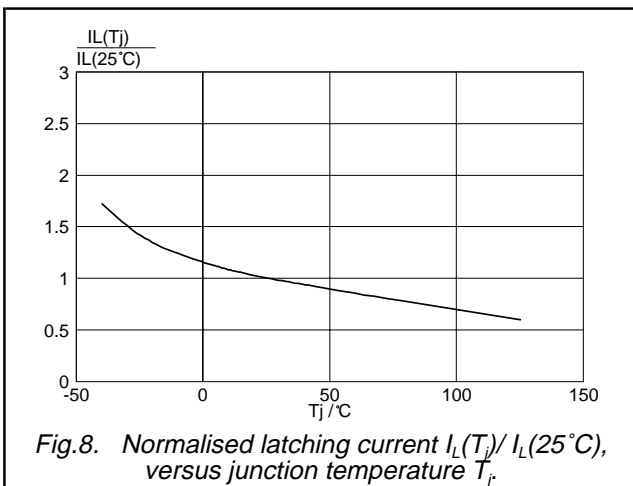sinusoidal currents, $f = 50$ Hz.

Fig.6. Normalised gate trigger voltage
$V_{GT}(T_j)/V_{GT}(25°C)$, versus junction temperature T_j.

*Fig.7.   Normalised gate trigger current
$I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.*

Fig.10. Typical and maximum on-state characteristic.

*Fig.8.   Normalised latching current $I_L(T_j)/ I_L(25°C)$,
versus junction temperature T_j.*

*Fig.11. Transient thermal impedance $Z_{th\,j\text{-}sp}$, versus
pulse width t_p.*

*Fig.9.   Normalised holding current $I_H(T_j)/ I_H(25°C)$,
versus junction temperature T_j.*

MOUNTING INSTRUCTIONS

Dimensions in mm.

Fig.12. soldering pattern for surface mounting SOT223.

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

Fig.13. SOT223 surface mounting package.
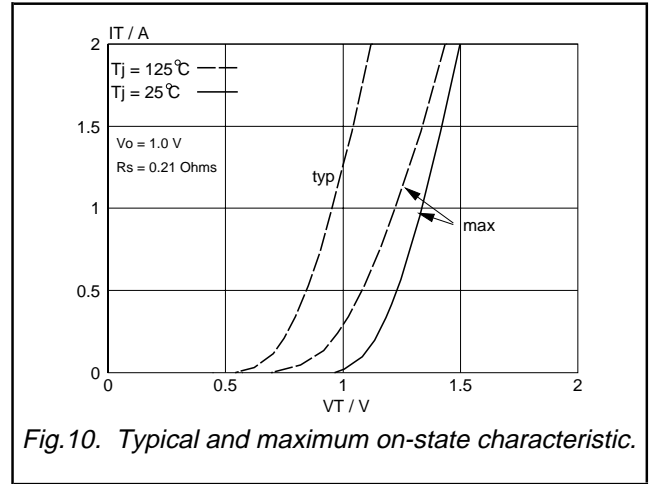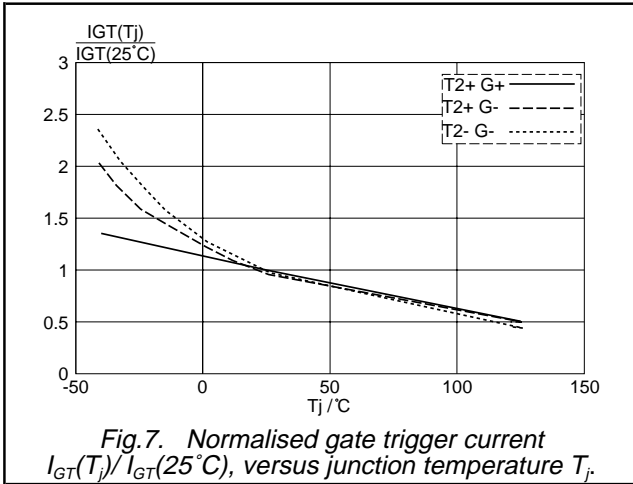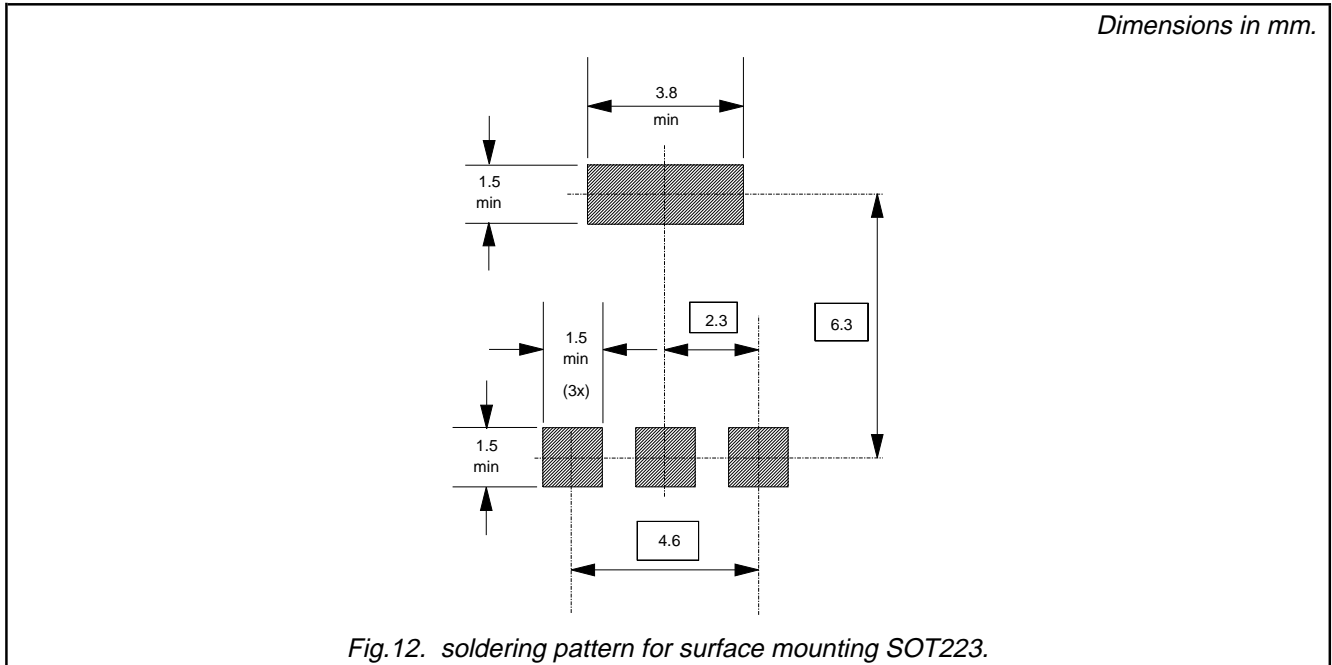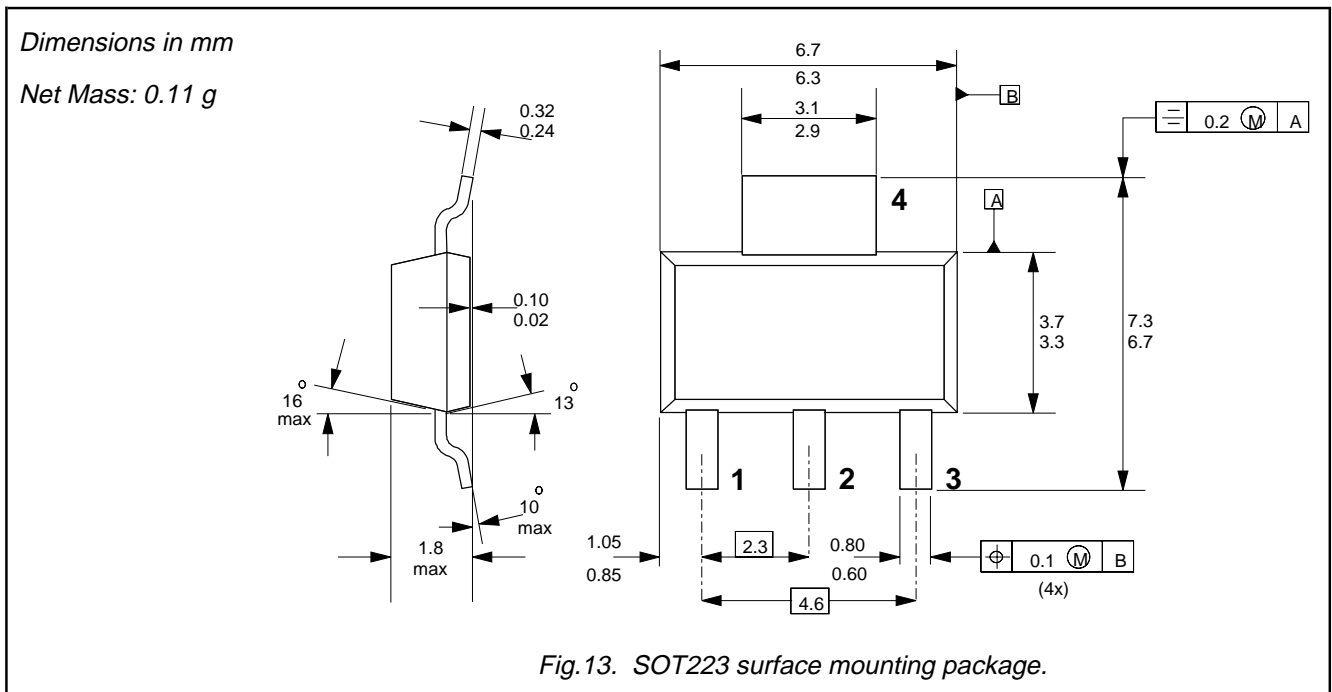
Notes
1. For further information, refer to Philips publication SC18 " SMD Footprint Design and Soldering Guidelines".
   Order code: 9397 750 00505.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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