

# Thyristors logic level for RCD/ GFI/ LCCB applications

## BT168W series

### GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in Residual Current Devices/ Ground Fault Interrupters/ Leakage Current Circuit Breakers (RCD/ GFI/ LCCB) applications where a minimum  $I_{GT}$  limit is needed. These devices may be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

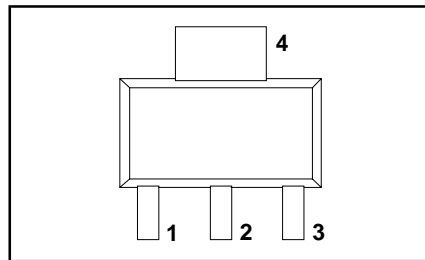
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	MAX.	UNIT
	<b>BT168</b>	<b>BW</b>	<b>DW</b>	<b>EW</b>	<b>GW</b>	
$V_{DRM}$ , $V_{RRM}$	Repetitive peak off-state voltages	200	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.6	0.6	0.6	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	1	1	1	A
$I_{TSM}$	Non-repetitive peak on-state current	8	8	8	8	A

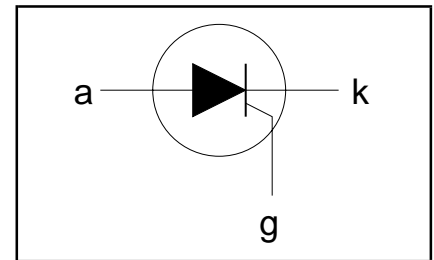
### PINNING - SOT223

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

### PIN CONFIGURATION



### SYMBOL



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.				UNIT
				B	D	E	G	
$V_{DRM}$ , $V_{RRM}$	Repetitive peak off-state voltages		-	200 <sup>1</sup>	400 <sup>1</sup>	500 <sup>1</sup>	600 <sup>1</sup>	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112^\circ\text{C}$	-	0.63				A
$I_{T(RMS)}$	RMS on-state current	all conduction angles $t = 10\text{ ms}$	-	1				A
$I_{TSM}$	Non-repetitive peak on-state current	$t = 8.3\text{ ms}$	-	8				A
		half sine wave; $T_j = 25^\circ\text{C}$ prior to surge	-	9				A
$I^2t$	$I^2t$ for fusing	$T_j = 25^\circ\text{C}$ prior to surge $t = 10\text{ ms}$	-	0.32				A <sup>2</sup> s
$dl_T/dt$	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$	-	50				A/ $\mu\text{s}$
$I_{GM}$	Peak gate current		-	1				A
$V_{GM}$	Peak gate voltage		-	5				V
$V_{RGM}$	Peak reverse gate voltage		-	5				V
$P_{GM}$	Peak gate power		-	2				W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.1				W
$T_{stg}$	Storage temperature		-40	150				$^\circ\text{C}$
$T_j$	Operating junction temperature		-	125				$^\circ\text{C}$

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu\text{s}$ .

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### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint pcb mounted, pad area as in fig:14	-	156 70	-	K/W K/W

### STATIC CHARACTERISTICS

 $T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; gate open circuit	20	50	200	$\mu\text{A}$
$I_L$	Latching current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$	-	2	6	mA
$I_H$	Holding current	$V_D = 12\text{ V}$ ; $I_{GT} = 0.5\text{ mA}$ ; $R_{GK} = 1\text{ k}\Omega$	-	2	5	mA
$V_T$	On-state voltage	$I_T = 2\text{ A}$	-	1.35	1.5	V
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; gate open circuit	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$ ; $I_T = 10\text{ mA}$ ; $T_j = 125\text{ °C}$ ; gate open circuit	0.2	0.3	-	V
$I_D, I_R$	Off-state leakage current	$V_D = V_{DRM(max)}$ ; $V_R = V_{RRM(max)}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$	-	0.05	0.1	mA

### DYNAMIC CHARACTERISTICS

 $T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; exponential waveform; $R_{GK} = 1\text{ k}\Omega$	-	25	-	V/ $\mu\text{s}$
$t_{gt}$	Gate controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 10\text{ mA}$ ; $di_G/dt = 0.1\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$
$t_q$	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $di_{TM}/dt = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK} = 1\text{ k}\Omega$	-	100	-	$\mu\text{s}$

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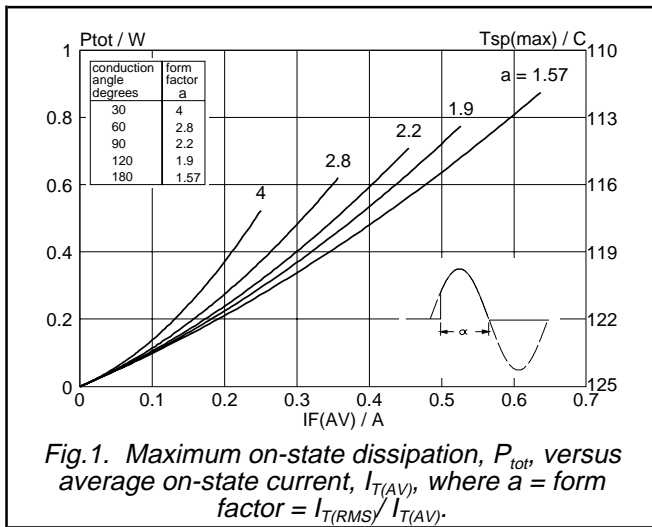


Fig.1. Maximum on-state dissipation,  $P_{tot}$  versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

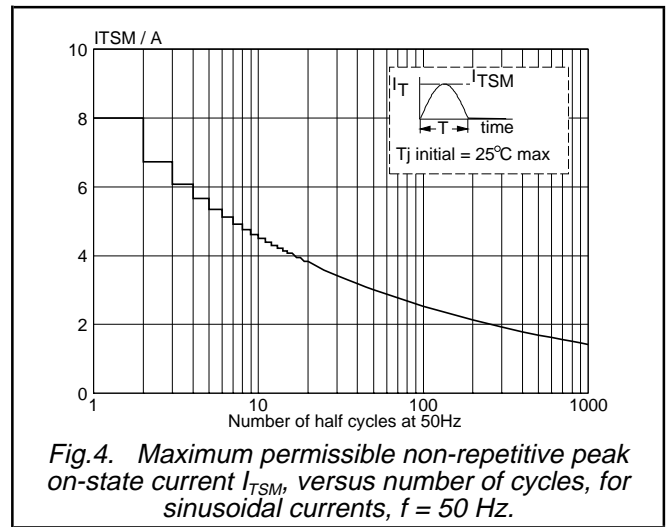


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50 \text{ Hz}$ .

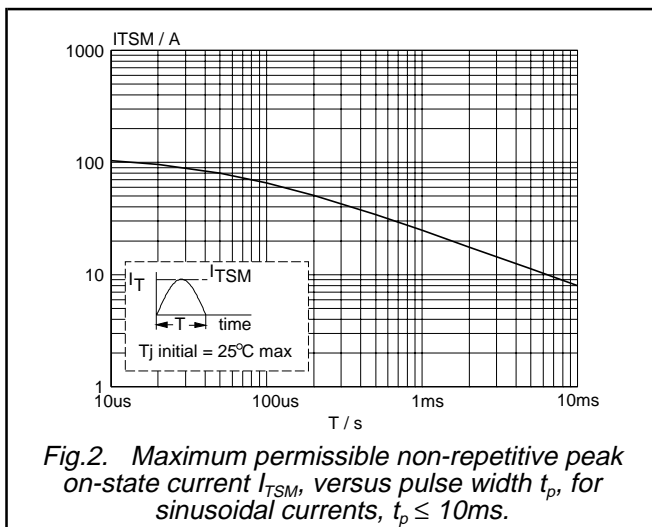


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10\text{ms}$ .

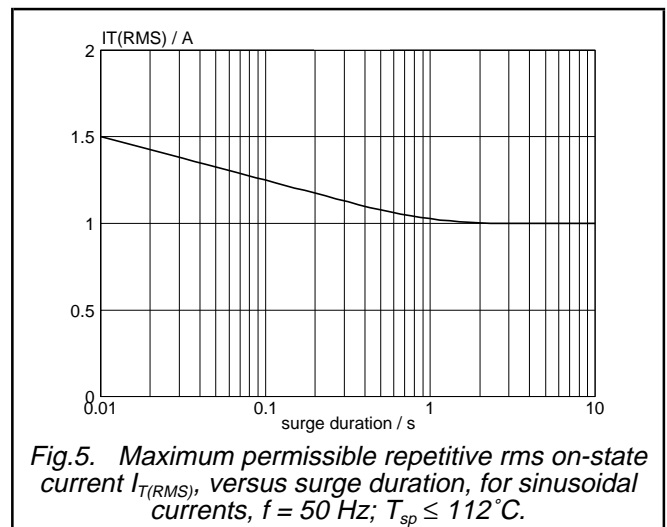


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50 \text{ Hz}$ ;  $T_{sp} \leq 112^\circ\text{C}$ .

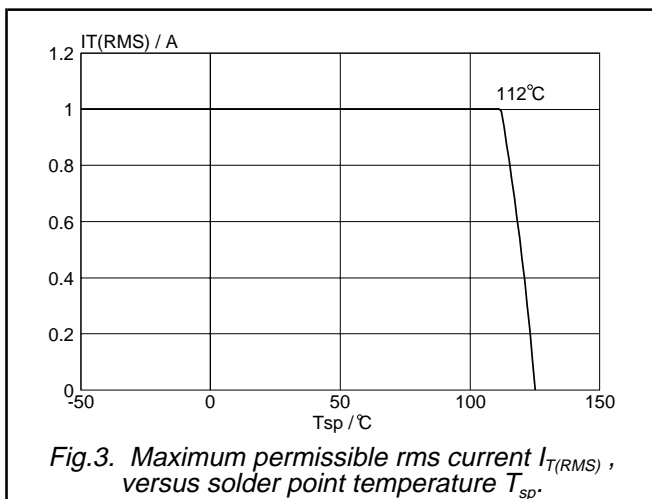


Fig.3. Maximum permissible rms current  $I_{T(RMS)}$ , versus solder point temperature  $T_{sp}$ .

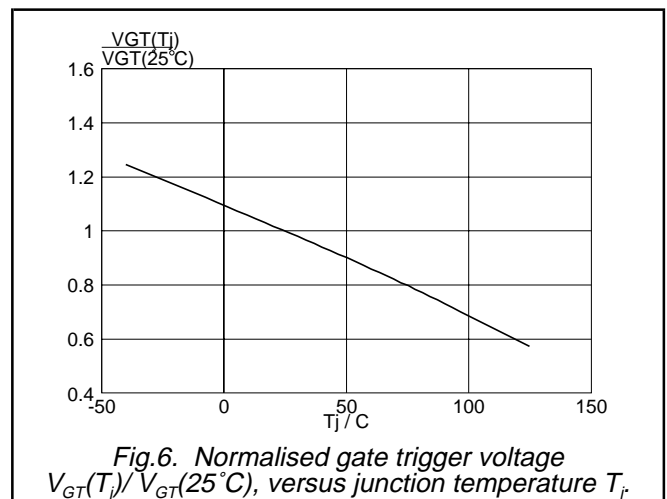
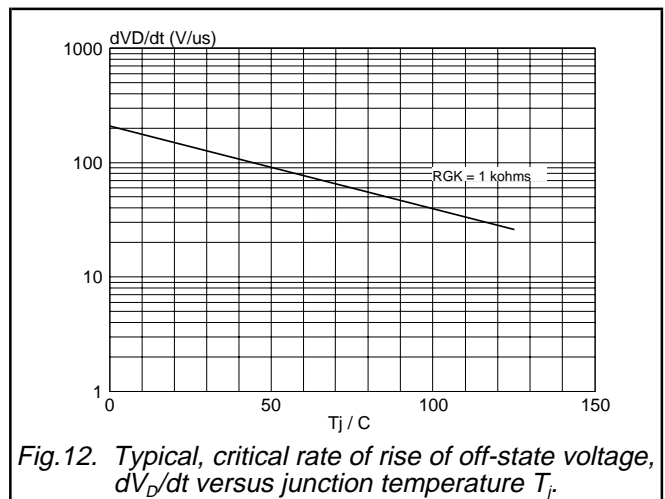
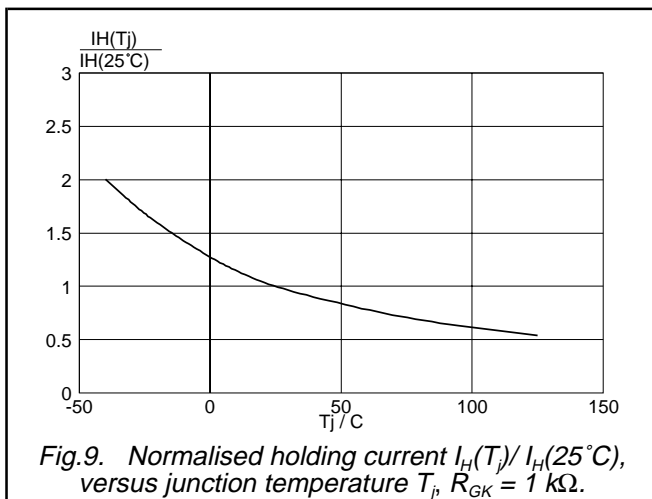
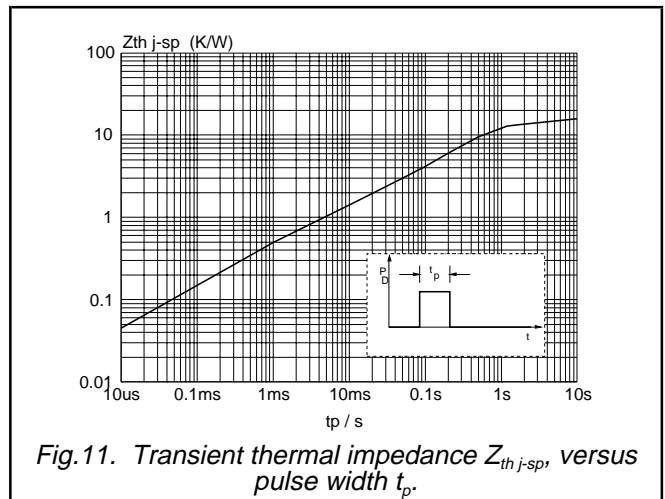
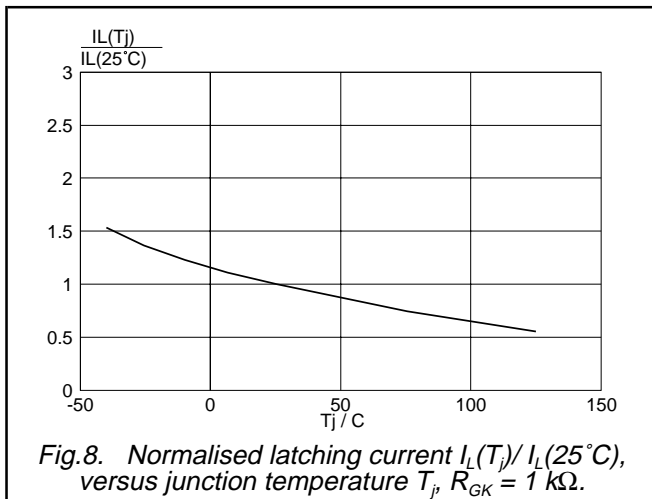
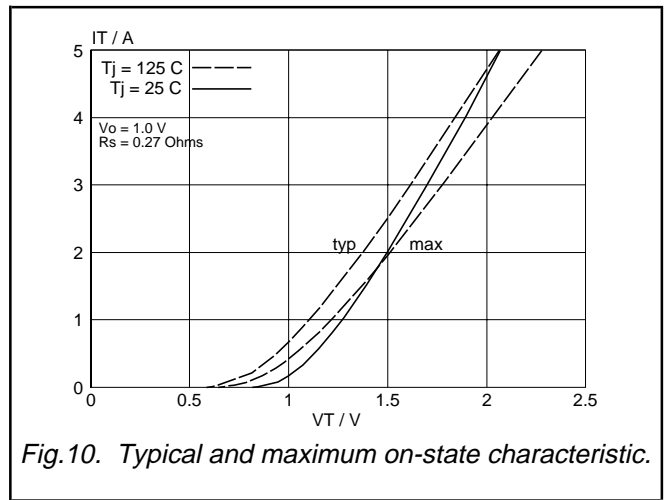
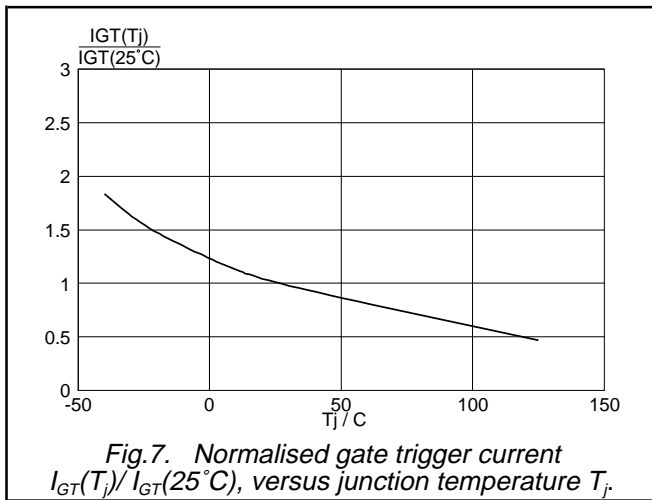


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

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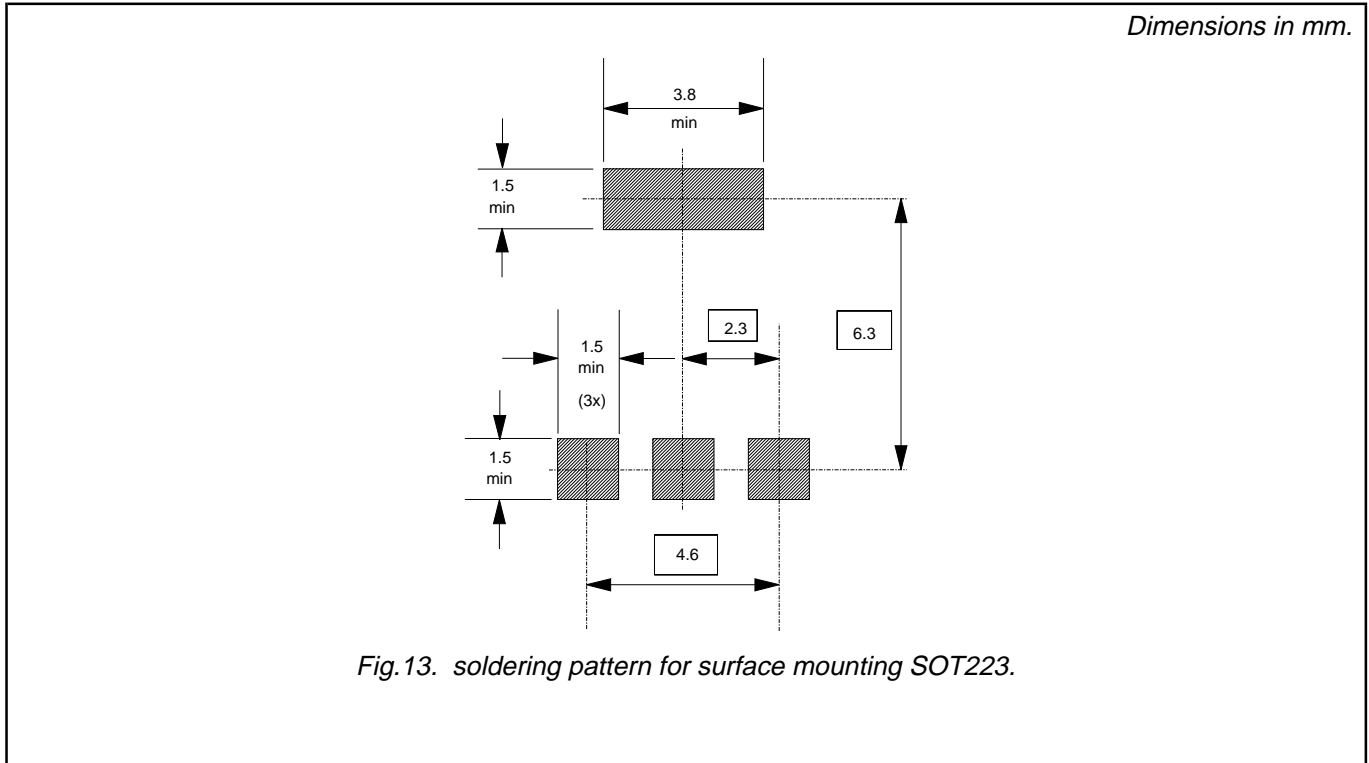
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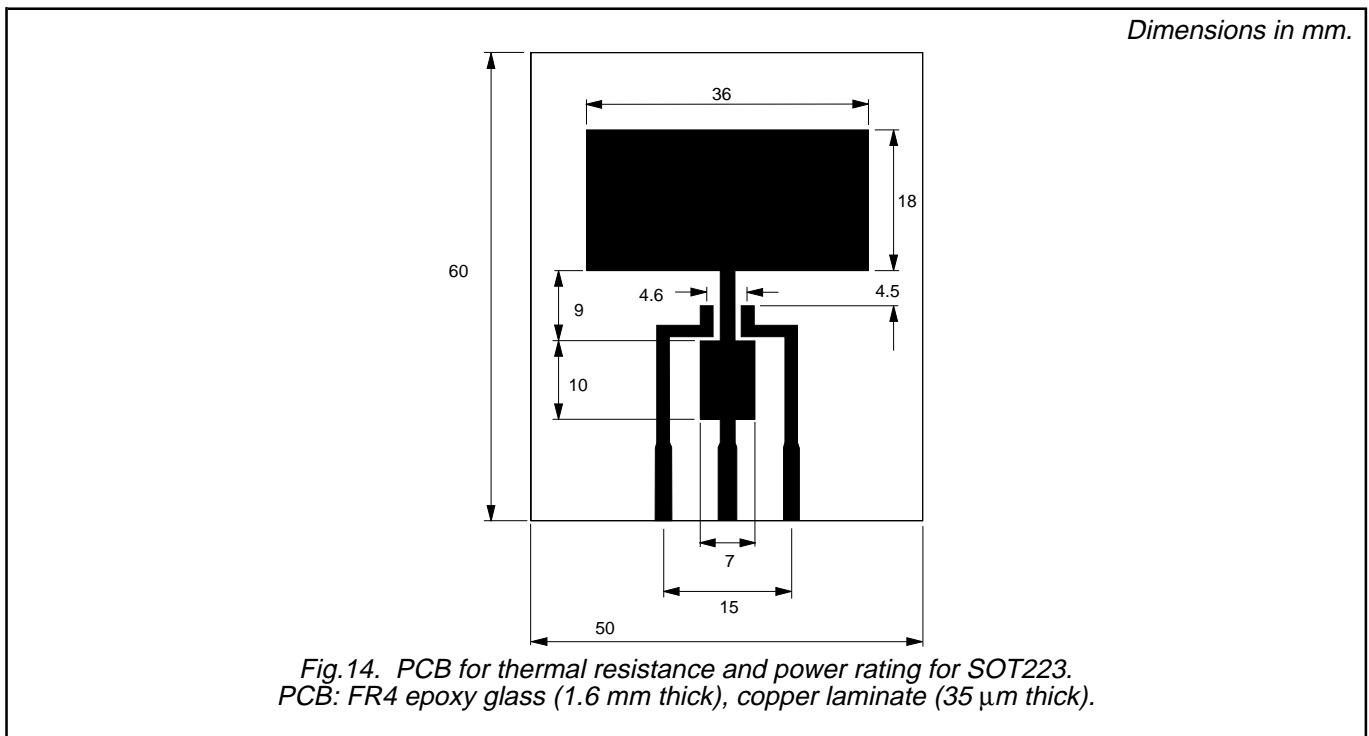
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**MOUNTING INSTRUCTIONS**



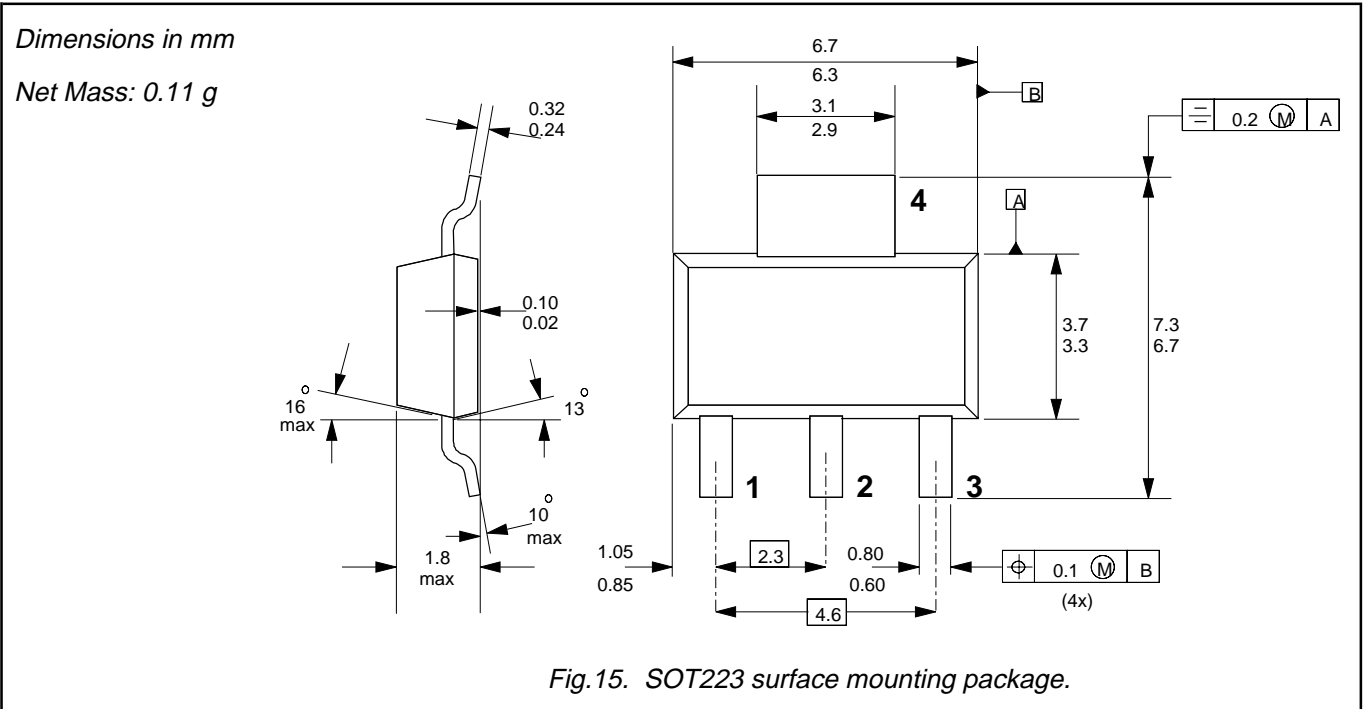
**PRINTED CIRCUIT BOARD**



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**MECHANICAL DATA**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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