

DATA SHEET

BST82

N-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

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DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in SOT23 envelope and designed for use as Surface Mounted Device (SMD) in thin and thick-film circuits for telephone ringer and for application with relay, high-speed and line-transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No second breakdown
- Low $R_{DS(on)}$

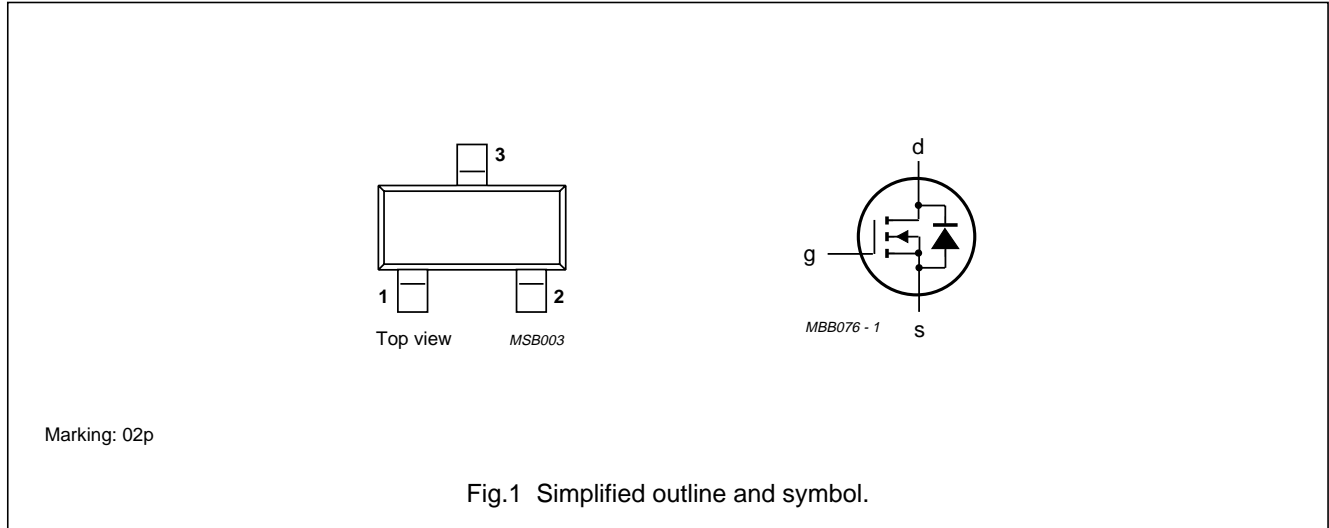
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	300 mW
Drain-source ON-resistance $I_D = 150$ mA; $V_{GS} = 5$ V	$R_{DS(on)}$	typ.	7 Ω
		max.	10 Ω
Transfer admittance $I_D = 175$ mA; $V_{DS} = 5$ V	$ Y_{fs} $	typ.	150 mS

PINNING - SOT23

- 1 = gate
- 2 = source
- 3 = drain

PIN CONFIGURATION



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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	80 V
Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms)	$V_{DS(SM)}$	max.	100 V
Gate-source voltage (open drain)	$\pm V_{GSO}$	max.	20 V
Drain current (DC)	I_D	max.	175 mA
Drain current (peak)	I_{DM}	max.	600 mA
Total power dissipation up to $T_{amb} = 25$ °C (note 1)	P_{tot}	max.	300 mW
Storage temperature range	T_{stg}		-65 to + 150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient (note 1)	$R_{th\ j-a}$	=	430 K/W
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Note

1. Transistors mounted on a ceramic substrate of 7 mm x 5 mm x 0.7 mm.

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CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified

Drain-source breakdown voltage

$$I_D = 10\ \mu\text{A}; V_{GS} = 0$$

$$V_{(BR)DSS} \quad \text{min.} \quad 80\ \text{V}$$

Drain-source leakage current

$$V_{DS} = 60\ \text{V}; V_{GS} = 0$$

$$I_{DSS} \quad \text{max.} \quad 1.0\ \mu\text{A}$$

Gate-source leakage current

$$V_{GS} = 20\ \text{V}; V_{DS} = 0$$

$$I_{GSS} \quad \text{max.} \quad 100\ \text{nA}$$

Gate-source cut-off voltage

$$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$$

$$V_{(P)GS} \quad \begin{array}{l} \text{min.} \\ \text{max.} \end{array} \quad \begin{array}{l} 1.5\ \text{V} \\ 3.5\ \text{V} \end{array}$$

Drain-source ON-resistance

$$I_D = 150\ \text{mA}; V_{GS} = 5\ \text{V}$$

$$R_{DS(on)} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 7\ \Omega \\ 10\ \Omega \end{array}$$

Transfer admittance

$$I_D = 175\ \text{mA}; V_{DS} = 5\ \text{V}$$

$$|Y_{fs}| \quad \text{typ.} \quad 150\ \text{mS}$$

Input capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{iss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 15\ \text{pF} \\ 30\ \text{pF} \end{array}$$

Output capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{oss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 13\ \text{pF} \\ 20\ \text{pF} \end{array}$$

Feedback capacitance at $f = 1\ \text{MHz}$

$$V_{DS} = 10\ \text{V}; V_{GS} = 0$$

$$C_{rss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 3\ \text{pF} \\ 6\ \text{pF} \end{array}$$

Switching times (see Figs 2 and 3)

$$I_D = 175\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$$

$$t_{on} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 4\ \text{ns} \\ 10\ \text{ns} \end{array}$$

$$t_{off} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 4\ \text{ns} \\ 10\ \text{ns} \end{array}$$

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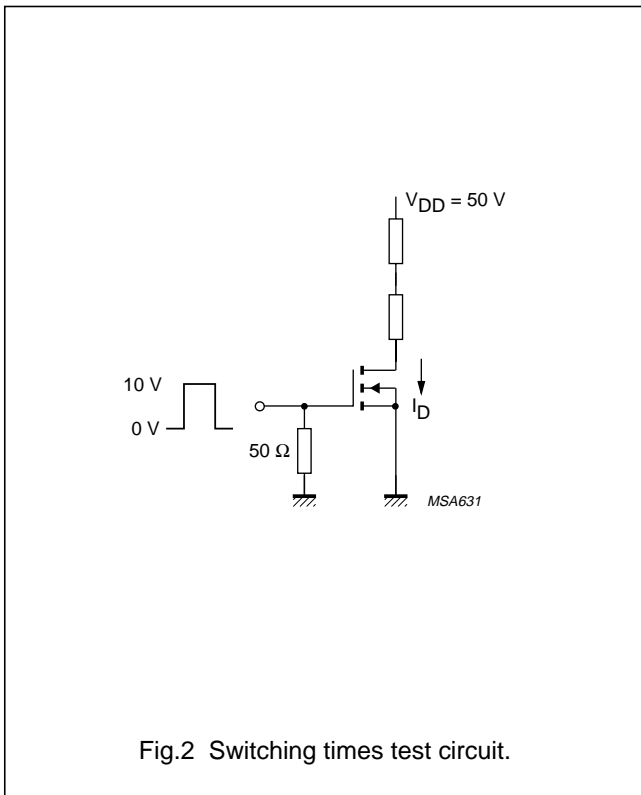


Fig.2 Switching times test circuit.

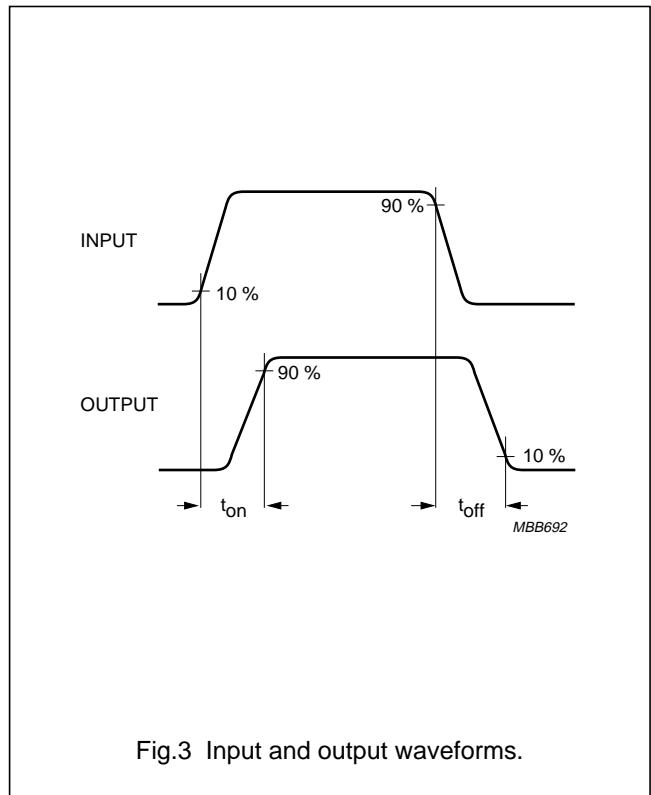


Fig.3 Input and output waveforms.

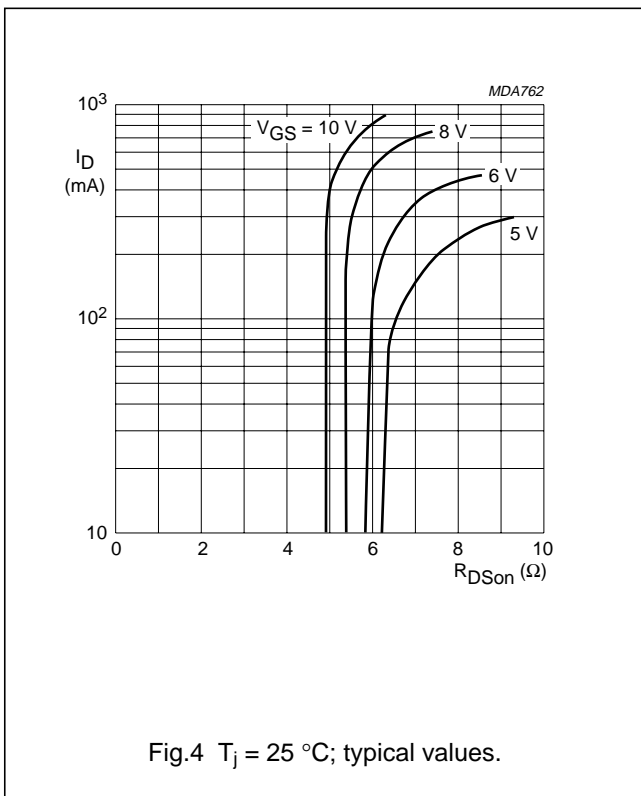


Fig.4 T_j = 25 °C; typical values.

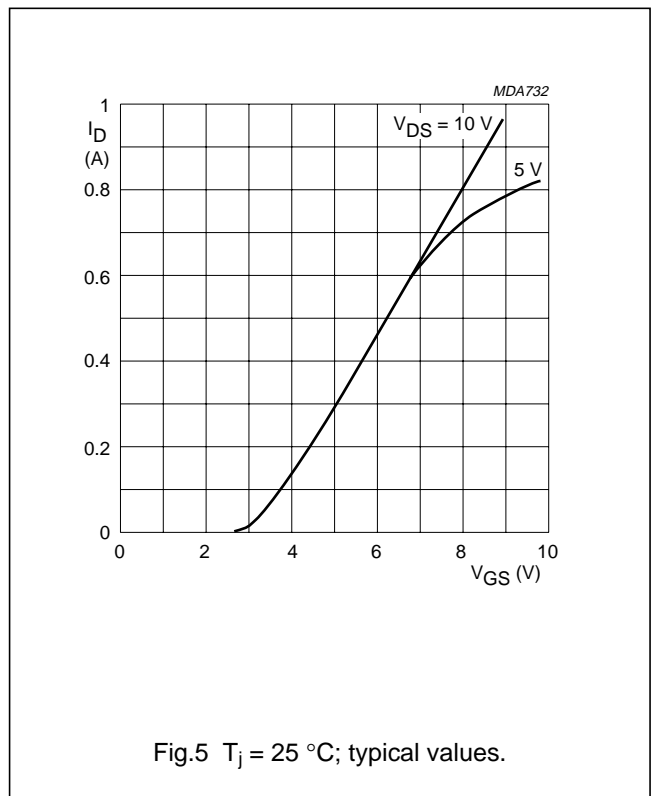
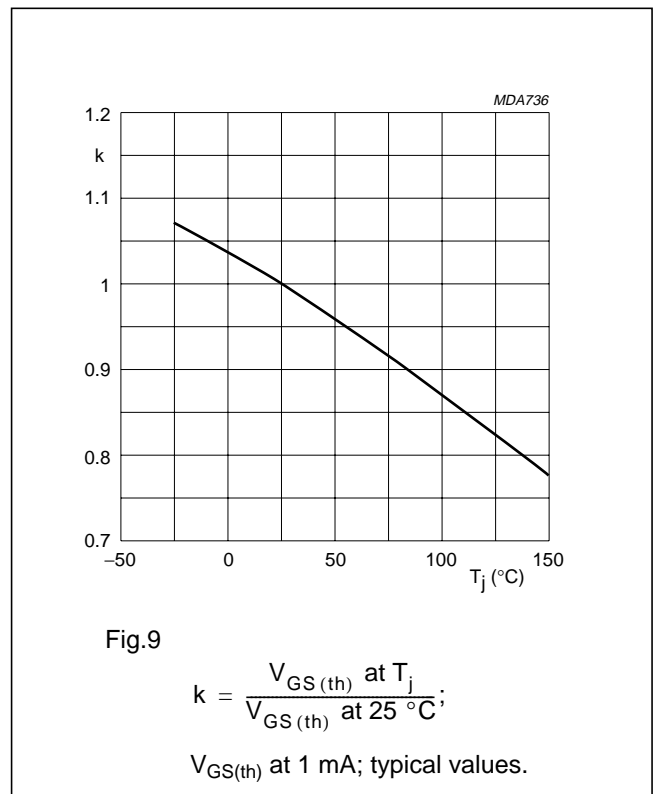
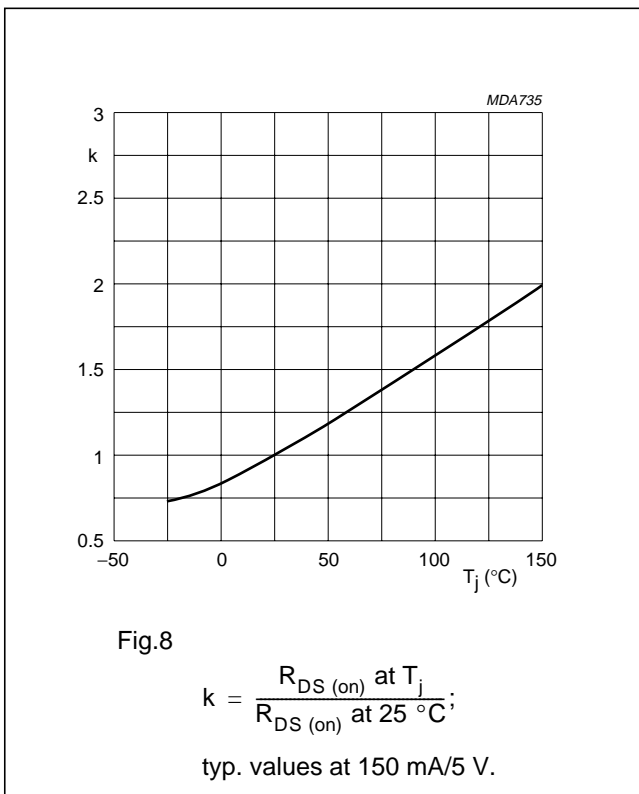
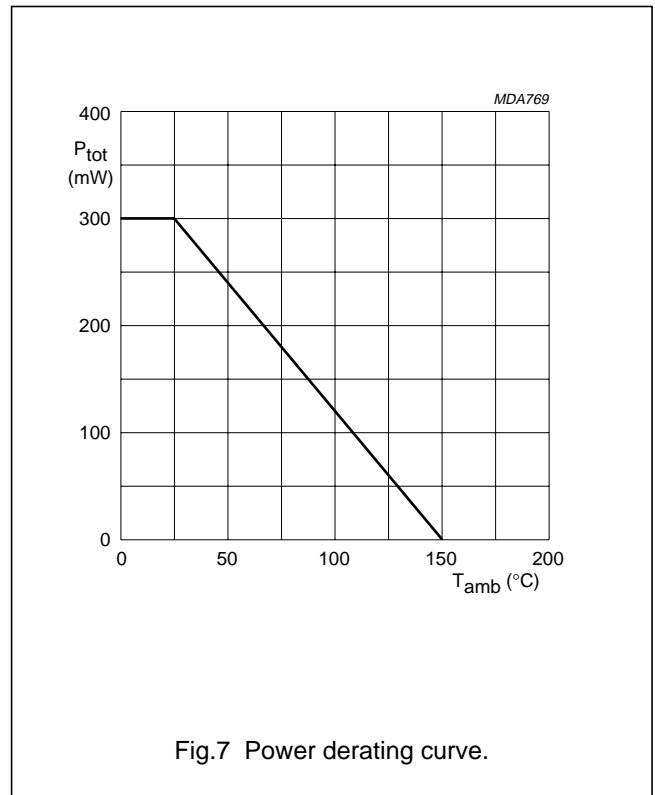
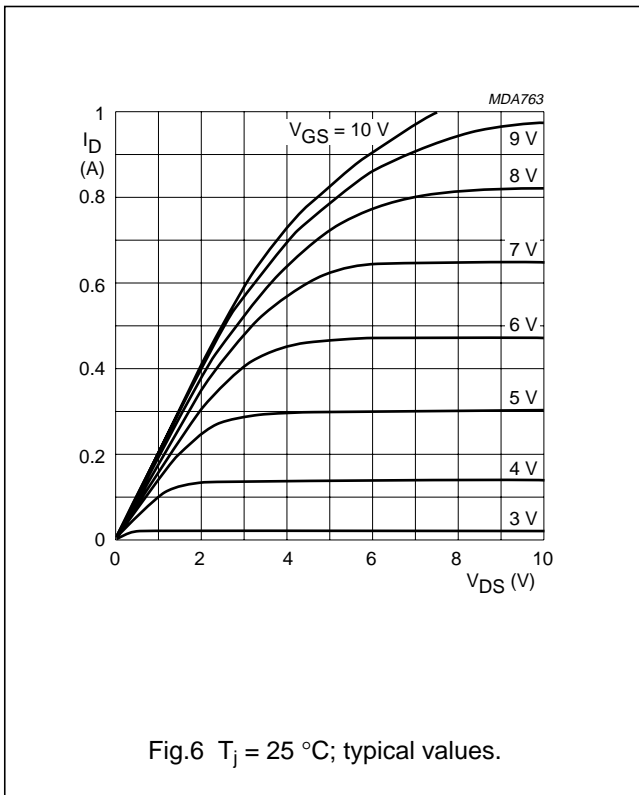


Fig.5 T_j = 25 °C; typical values.

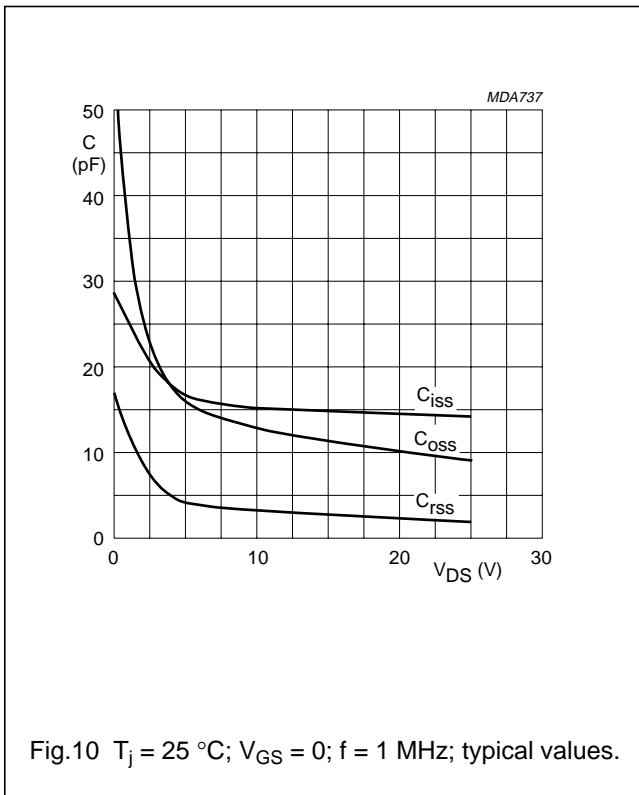
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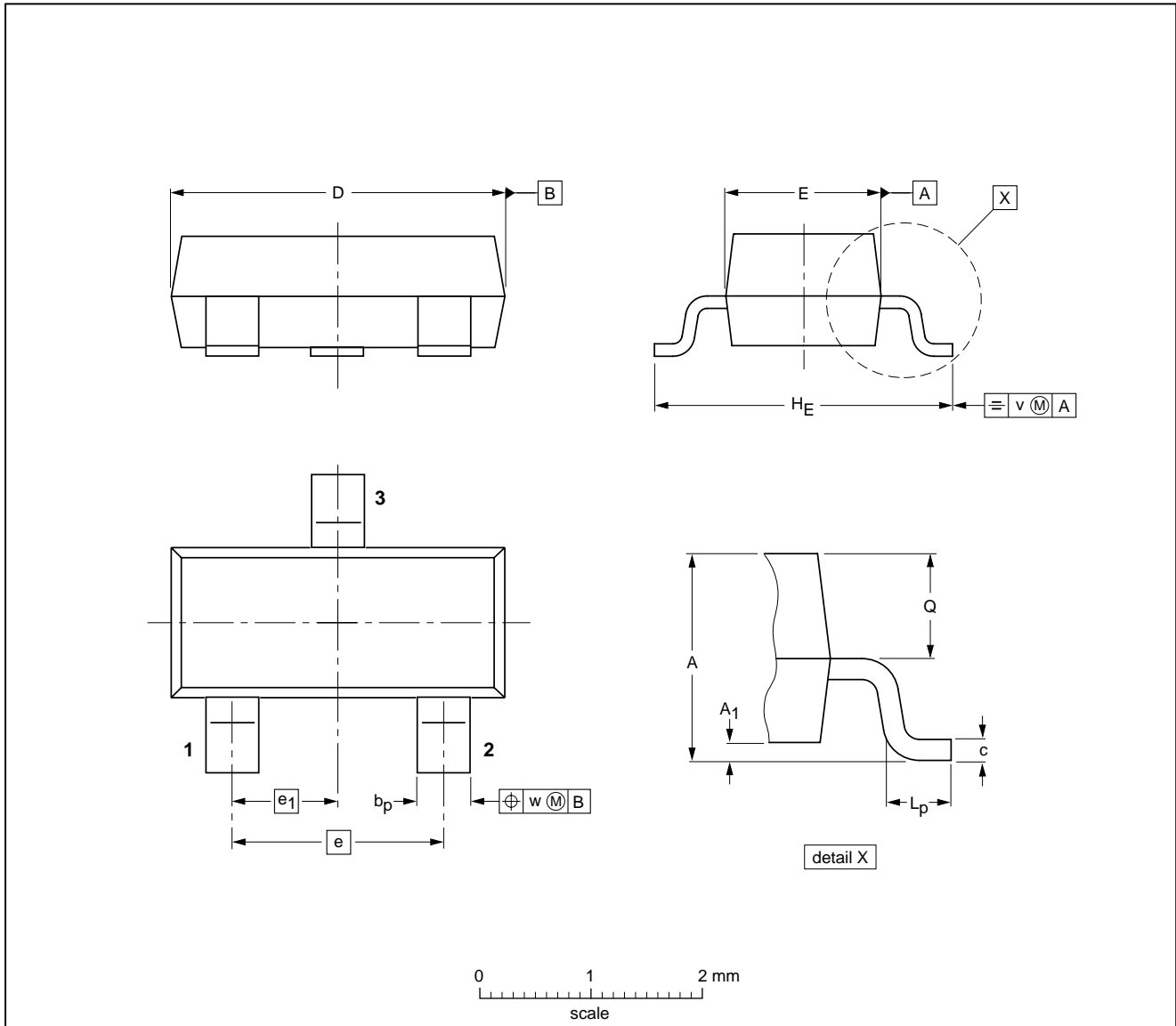
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PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

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BST82**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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