

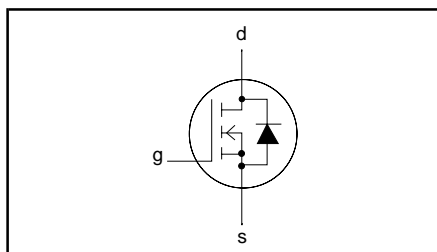
N-channel TrenchMOS™ transistor Logic level FET

PHN1018

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Low-profile surface mount package
- Logic level compatible

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 25\text{ V}$
$I_D = 9.6\text{ A}$
$R_{DS(ON)} \leq 18\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$)
$R_{DS(ON)} \leq 21\text{ m}\Omega$ ($V_{GS} = 5\text{ V}$)

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a surface mounting plastic package using 'trench' technology.

Application:-

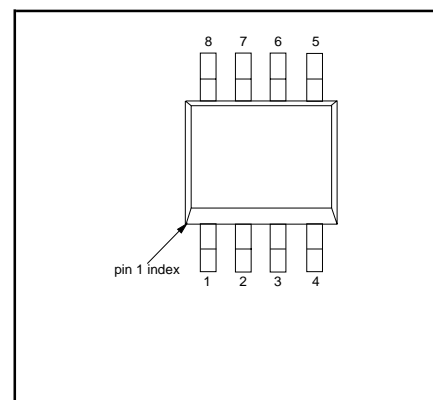
- High frequency computer motherboard d.c. to d.c. converters

The PHN1018 is supplied in the SOT96-1 (SO8) surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96-1 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	25	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	Gate-source voltage (DC)	-	-	± 15	V
V_{GSM}	Gate-source voltage (pulse peak value)	-	-	± 20	V
I_D	Drain current ($t_p \leq 10\text{ s}$)	$T_a = 25\text{ }^\circ\text{C}$ $T_a = 70\text{ }^\circ\text{C}$	-	9.6 7.7	A A
I_{DM}	Drain current (pulse peak value)	$T_a = 25\text{ }^\circ\text{C}$	-	38	A
P_{tot}	Total power dissipation	$T_a = 25\text{ }^\circ\text{C}$ $T_a = 70\text{ }^\circ\text{C}$	-	2.5 1.6	W W
T_j, T_{stg}	Operating junction and storage temperature	-	- 55	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board, $t \leq 10\text{ sec}$	-	50	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Surface mounted, FR4 board	150	-	K/W

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ELECTRICAL CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55 °C	25 22	- -	- -	V V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 150 °C T _j = -55 °C	1 0.6 -	1.5 - -	2 - 2.3	V V V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A V _{GS} = 5 V; I _D = 10 A V _{GS} = 5 V; I _D = 10 A; T _j = 150 °C	- - -	13 18 -	18 21 36	mΩ mΩ mΩ
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 10 A	8	25	-	S
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V	-	10	100	nA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 25 V; V _{GS} = 0 V; T _j = 150 °C	-	0.05	10 500	μA μA
Q _{g(tot)}	Total gate charge	I _D = 10 A; V _{DD} = 15 V; V _{GS} = 5 V	-	17	-	nC
Q _{gs}	Gate-source charge		-	4	-	nC
Q _{gd}	Gate-drain (Miller) charge		-	6	-	nC
t _{d on}	Turn-on delay time	V _{DD} = 15 V; I _D = 25 A;	-	6.4	12	ns
t _r	Turn-on rise time	V _{GS} = 10 V; R _G = 5 Ω	-	62	75	ns
t _{d off}	Turn-off delay time	Resistive load	-	50	75	ns
t _f	Turn-off fall time		-	30	45	ns
L _d	Internal drain inductance	Drain leads to centre of die	-	1	-	nH
L _s	Internal source inductance	Source leads to source bond pad	-	3	-	nH
C _{ISS}	Input capacitance	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz	-	1050	-	pF
C _{OSS}	Output capacitance		-	330	-	pF
C _{rSS}	Feedback capacitance		-	220	-	pF

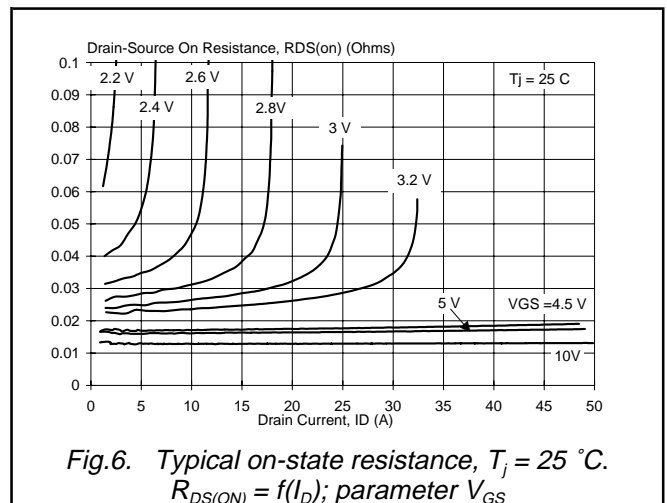
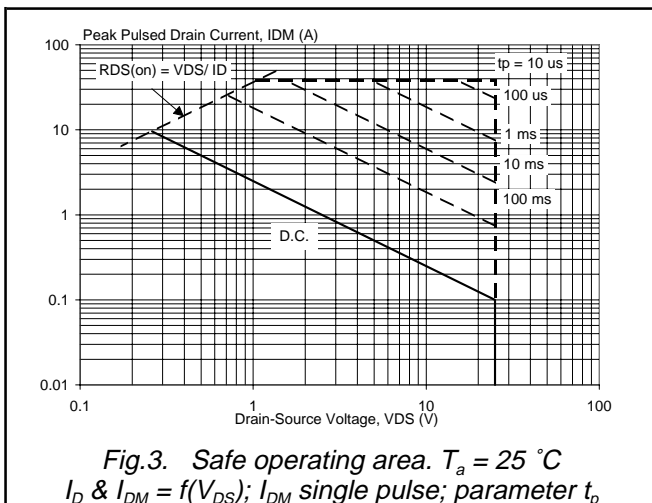
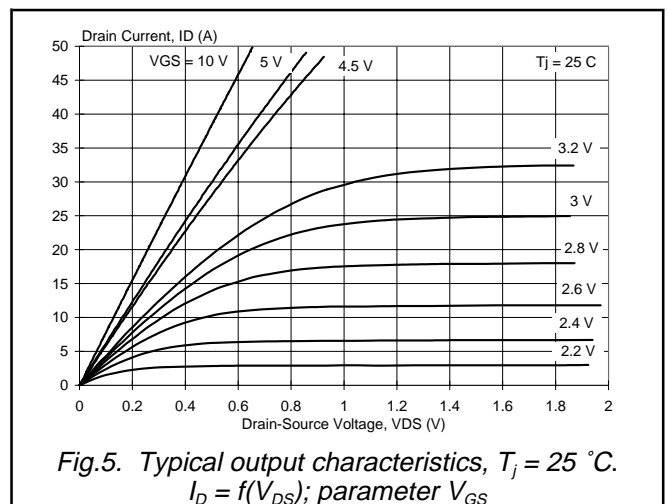
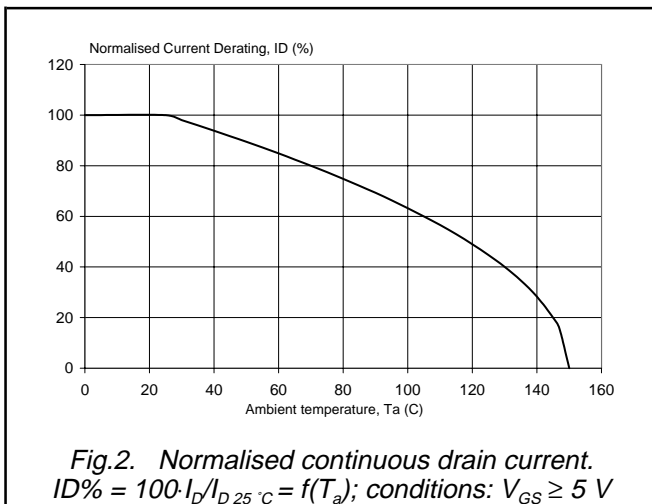
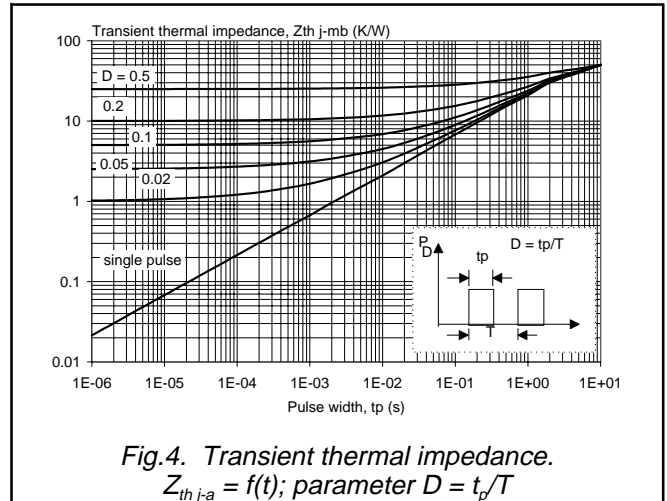
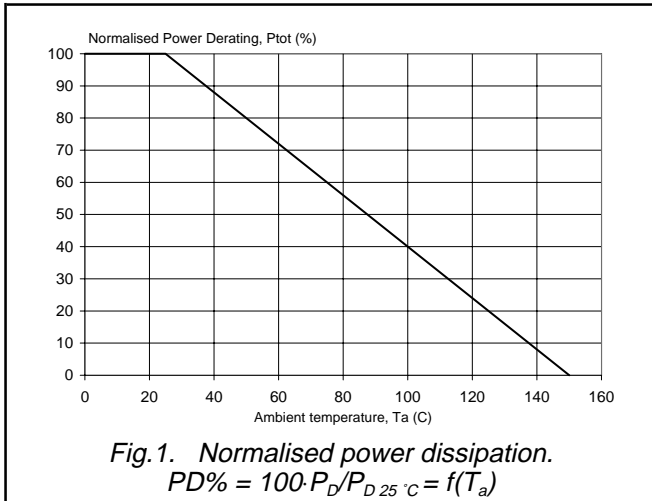
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous source current (body diode)	T _a = 25 °C, t _p ≤ 10 s	-	-	9.6	A
I _{DRM}	Pulsed source current (body diode)		-	-	38	A
V _{SD}	Diode forward voltage	I _F = 10 A; V _{GS} = 0 V	-	0.83	1.2	V
t _{rr}	Reverse recovery time	I _F = 10 A; -di _F /dt = 100 A/μs;	-	100	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = 0 V; V _R = 25 V	-	0.13	-	μC

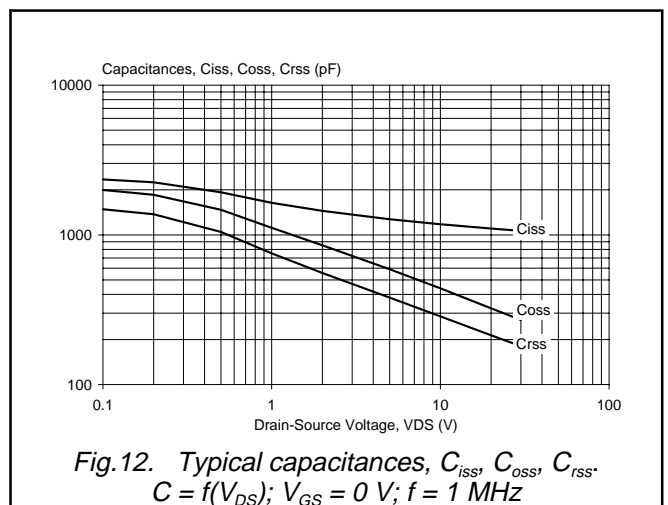
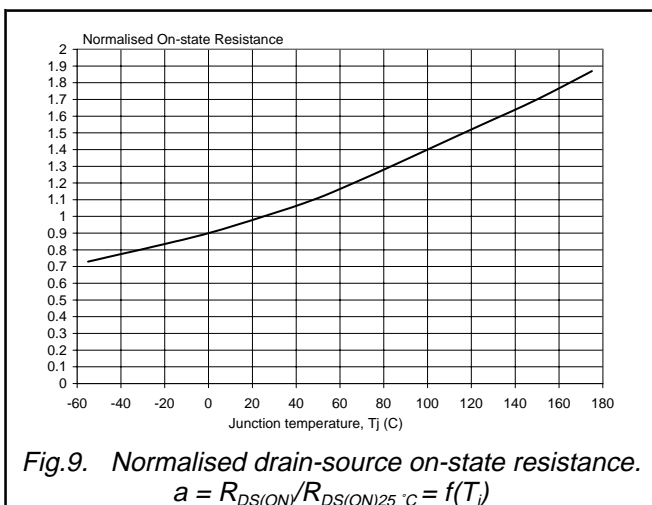
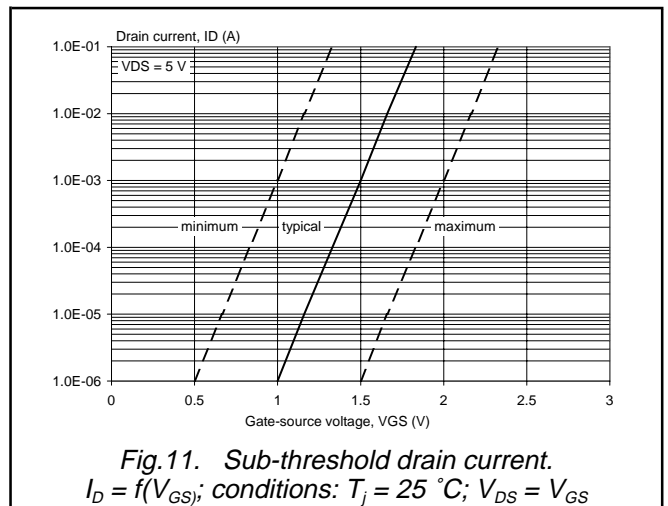
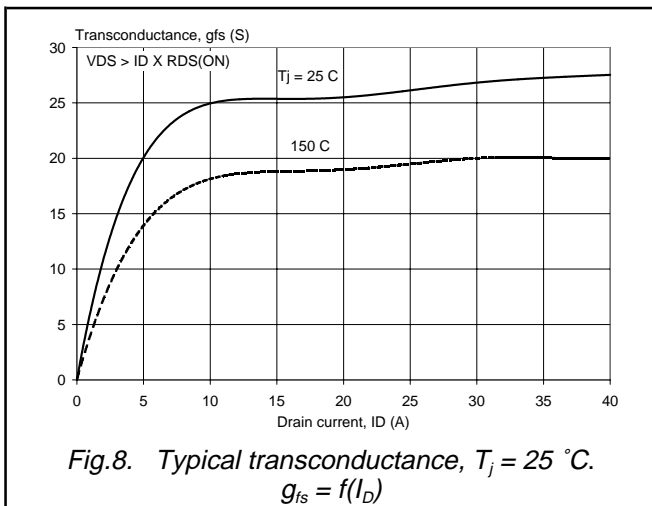
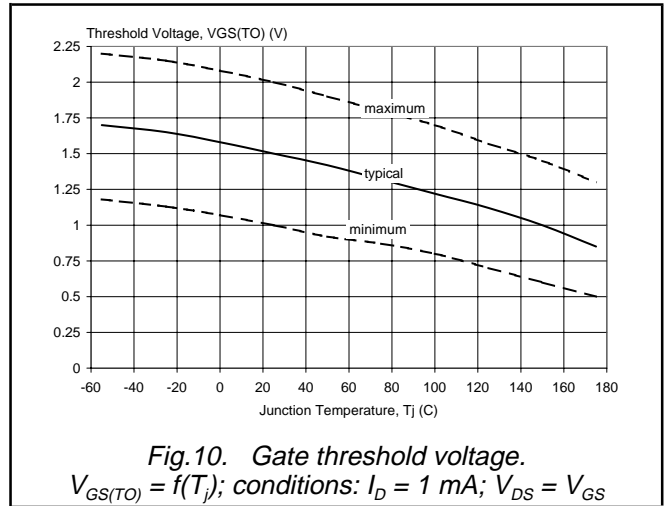
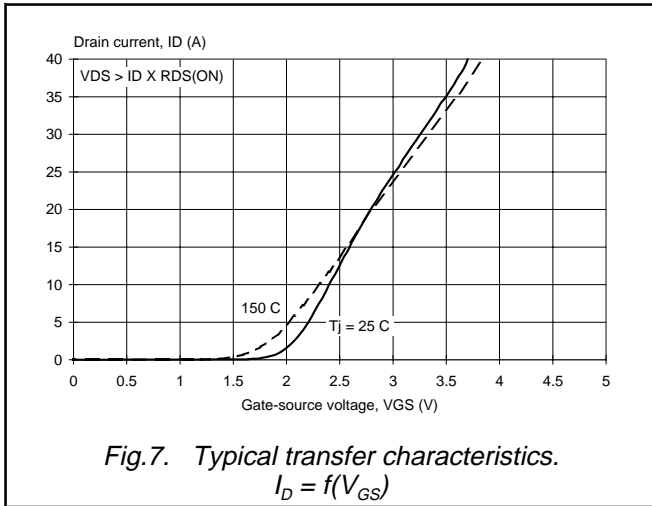
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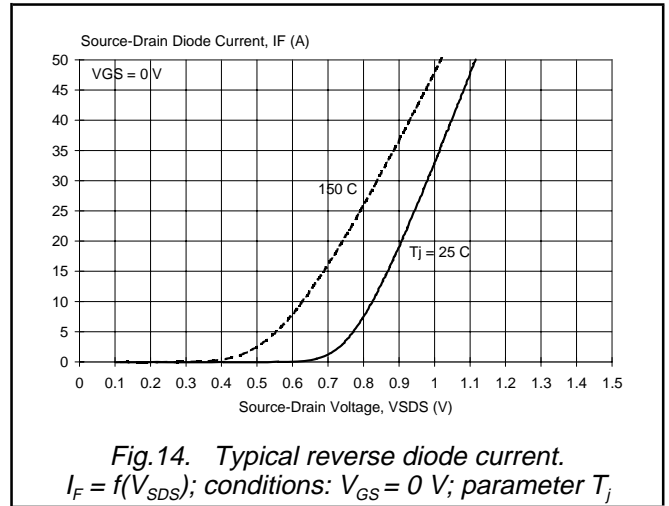
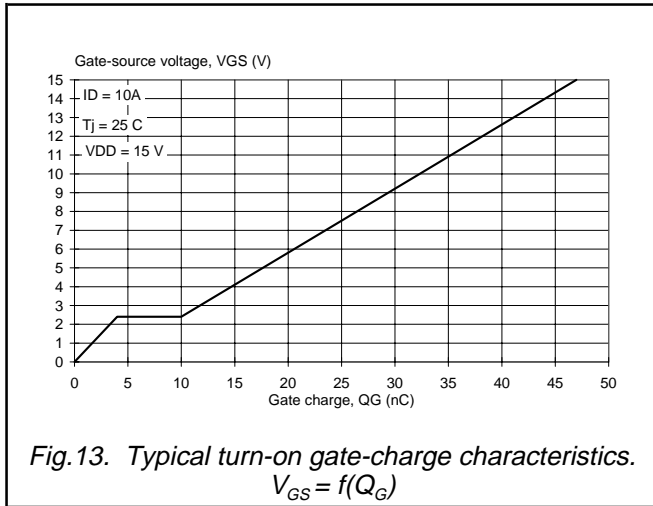
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MECHANICAL DATA

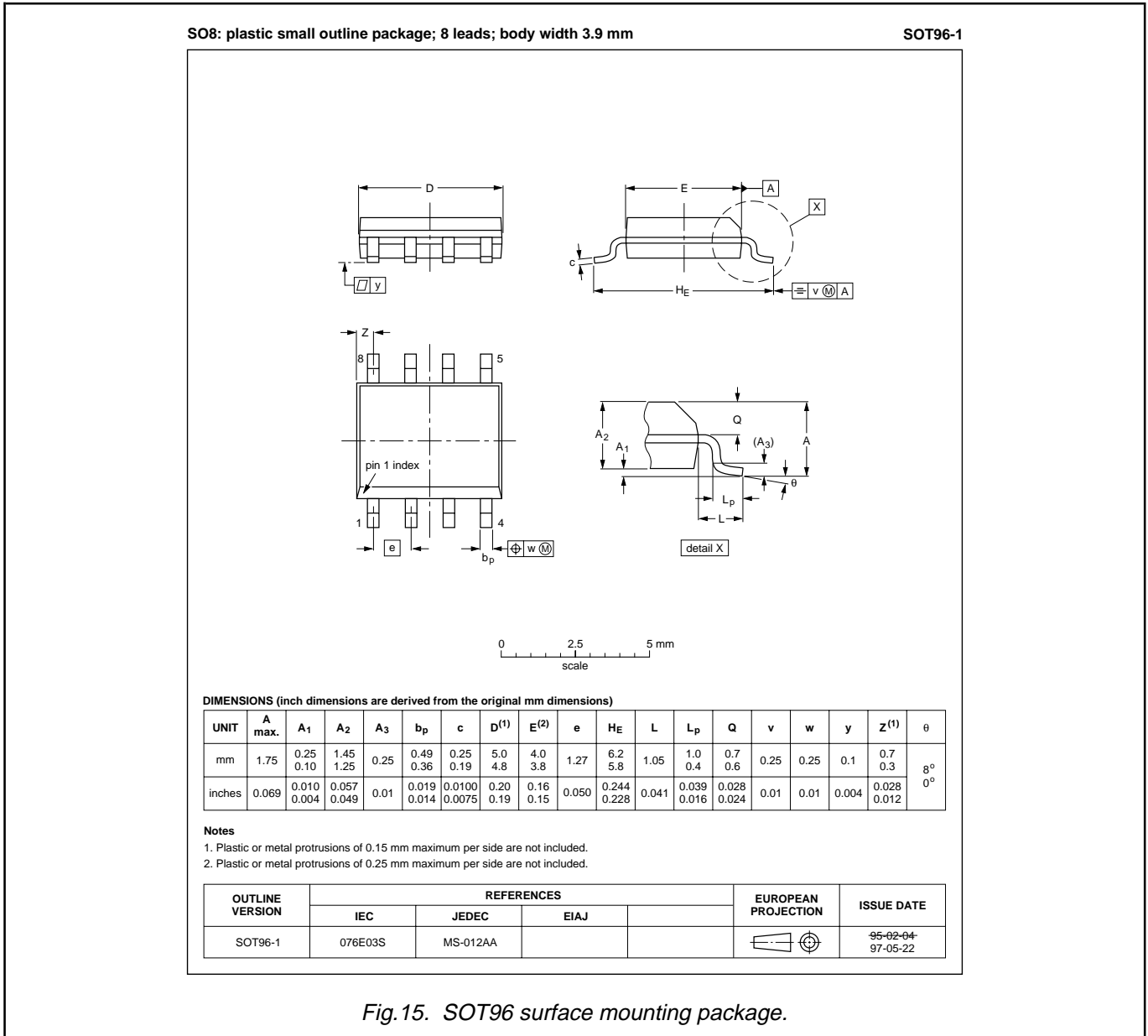


Fig. 15. SOT96 surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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