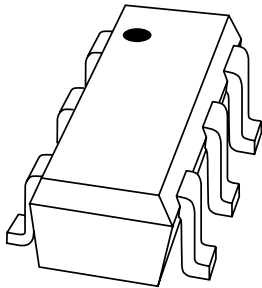


# DATA SHEET



## **BGA2031/1** MMIC variable gain amplifier

Preliminary specification

2000 Feb 17

# MMIC variable gain amplifier

# BGA2031/1

### FEATURES

- High gain
- Excellent adjacent channel power rejection
- Small SMD package
- Low dissipation.

### APPLICATIONS

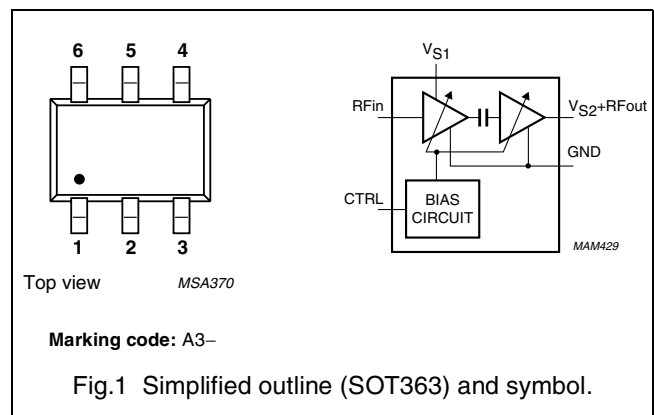
- General purpose variable gain amplifier for low voltage and medium power
- Driver for power amplifiers in systems that require good linearity, such as CDMA, both cellular band (850 MHz) and PCS (1.9 GHz). This is because of the high output power and good linearity.

### DESCRIPTION

Silicon Monolithic Microwave Integrated Circuit (MMIC) 2 stage variable gain amplifier in double polysilicon technology in a 6-pin SOT363 plastic SMD package for low voltage medium power applications.

### PINNING

PIN	DESCRIPTION
1	RF in
2	CTRL
3	V <sub>S1</sub>
4	V <sub>S2</sub> + RF out
5	GND
6	GND



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V <sub>S1</sub> , V <sub>S2</sub>	supply voltages		3	3.3	V
I <sub>S</sub>	supply current into pin 3 + pin 4	V <sub>CTRL</sub> = 0	0	10	μA
		V <sub>CTRL</sub> = 2.7 V; V <sub>S</sub> = 3 V	51	63	mA
		V <sub>CTRL</sub> = 2.4 V; V <sub>S</sub> = 3 V	30	37	mA
P <sub>L</sub>	load power	at 1 dB gain compression point; f = 1.9 GHz	13	–	dBm
ACPR	adjacent channel power rejection	f = 1.9 GHz; P <sub>L</sub> = 10 dBm	49	–	dBc
		f = 836 MHz; P <sub>L</sub> = 8 dBm	48	–	dBc
G <sub>p</sub>	power gain	f = 1.9 GHz; P <sub>L</sub> = 12 dBm	23	–	dB
		f = 836 MHz; P <sub>L</sub> = 8 dBm	24	–	dB
ΔG	gain control range	f = 836 MHz; P <sub>L</sub> = 8 dBm	62	–	dB

### CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

MMIC variable gain amplifier

BGA2031/1

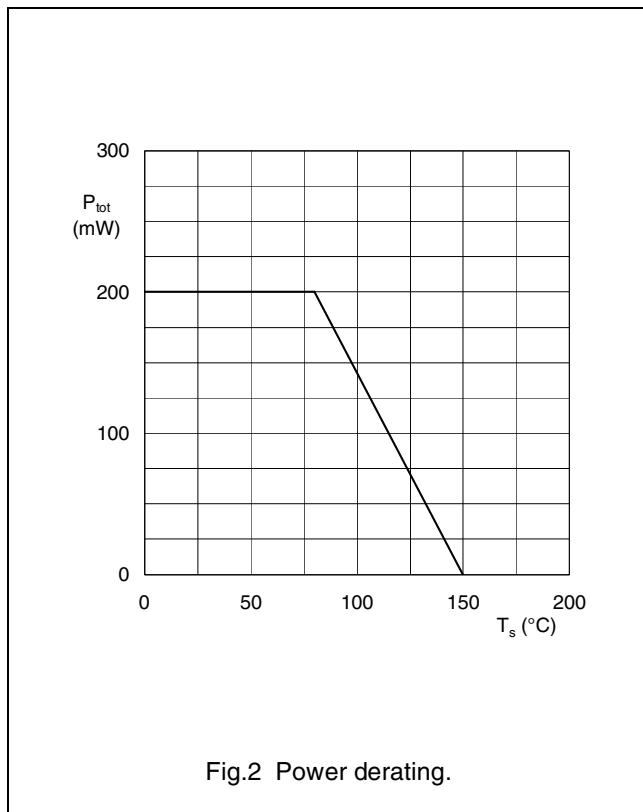
**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>S</sub>	DC supply voltage		–	3.3	V
V <sub>CTRL</sub>	control voltage		–	< V <sub>S</sub>	V
I <sub>CTRL</sub>	control current		–	1.2	mA
I <sub>S1</sub>	current into pin 3		–	27	mA
I <sub>S2</sub>	current into pin 4		–	50	mA
P <sub>D</sub>	drive power		–	tbf	dBm
P <sub>tot</sub>	total power dissipation	T <sub>s</sub> ≤ 80 °C	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	operating junction temperature		–	150	°C

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-s</sub>	thermal resistance from junction to solder point		350	K/W



## MMIC variable gain amplifier

BGA2031/1

## CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ ;  $Z_S = Z_L = 50\ \Omega$ ;  $V_S = 3\text{ V}$ ; unless otherwise specified.

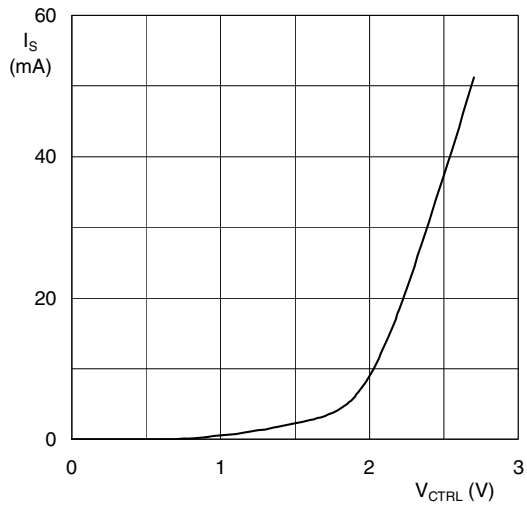
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f	frequency range		800	–	2500	MHz
$V_{S1}, V_{S2}$	supply voltages		2.7	3	3.3	V
$I_S$	supply current (in pin 3 + pin 4)	$V_{CTRL} = 0$ ; $P_D = 0\text{ mW}$	–	0	10	$\mu\text{A}$
		$V_{CTRL} = 2.7\text{ V}$ ; $V_S = 3\text{ V}$ ; $P_D = 0\text{ mW}$	37	51	63	mA
		$V_{CTRL} = 2.4\text{ V}$ ; $V_S = 3\text{ V}$ ; $P_D = 0\text{ mW}$	23	30	37	mA
$I_{CTRL}$	control current	$V_{CTRL} = 2.7\text{ V}$	0.7	0.92	1.1	mA
<b>f = 1900 MHz</b>						
f	frequency range		1850	–	1950	MHz
$G_P$	power gain	$V_{CTRL} = 2.7\text{ V}$ ; $P_L = 12\text{ dBm}$	–	23	–	dB
$\Delta G$	gain control range	$0 < V_{CTRL} < 2.7\text{ V}$	–	56	–	dB
$G_{CS}$	gain control slope	note 1	–	21	–	dB/V
ACPR	adjacent channel power rejection	$\pm 1.23\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 10\text{ dBm}$	–	49	–	dBc
		$\pm 1.98\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 10\text{ dBm}$	–	74	–	dBc
$P_L$	load power	at 1 dB gain compression point	–	13	–	dBm
$P_N$	noise power	in CDMA receive band (1895 – 1955 MHz)	–	tbf	–	dBm/Hz
$V_{SWR_{IN}}$	input VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:3.5	–	
$V_{SWR_{OUT}}$	output VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:1.3	–	
<b>f = 836 MHz</b>						
f	frequency range		824	–	849	MHz
$G_P$	power gain	$V_{CTRL} = 2.7\text{ V}$ ; $P_L = 8\text{ dBm}$	–	24	–	dB
$\Delta G$	gain control range	$0 < V_{CTRL} < 2.7\text{ V}$	–	62	–	dB
$G_{CS}$	gain control slope	note 1	–	22	–	dB/V
ACPR	adjacent channel power rejection	$\pm 885\text{ kHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 8\text{ dBm}$	–	49	–	dBc
		$\pm 1.98\text{ MHz}$ offset; $BW_{ACP} = 30\text{ kHz}$ ; $BW_{carrier} = 1.23\text{ MHz}$ ; $P_L = 8\text{ dBm}$	–	74	–	dBc
$P_L$	load power	at 1 dB gain compression point	–	11	–	dBm
$P_N$	noise power	in CDMA receive band (869 to 894 MHz)	–	tbf	–	dBm/Hz
$V_{SWR_{IN}}$	input VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:2	–	
$V_{SWR_{OUT}}$	output VSWR	$V_{CTRL} = 2.7\text{ V}$	–	1:1.4	–	

## Notes

$$1. G_{CS} = (G @ V_{ctrl} = 2.5\text{ V} - G @ V_{ctrl} = 1.5\text{ V}) / (V_{ctrl} = 2.5\text{ V} - V_{ctrl} = 1.5\text{ V})$$

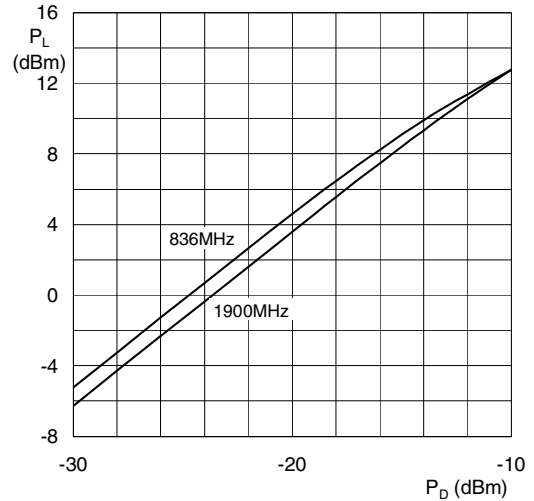
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BGA2031/1



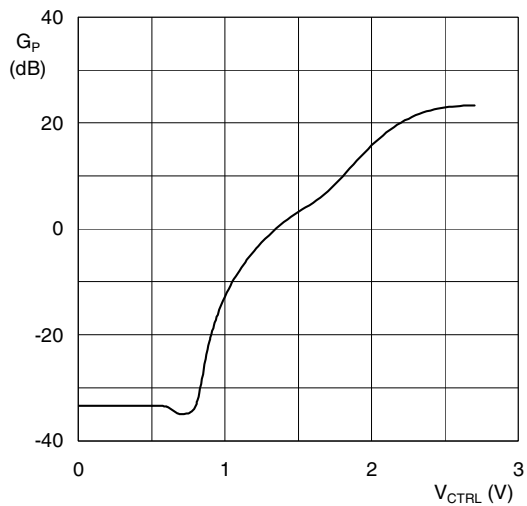
V<sub>S</sub> = 3 V.

Fig.2 Total supply current as a function of control voltage; typical values.



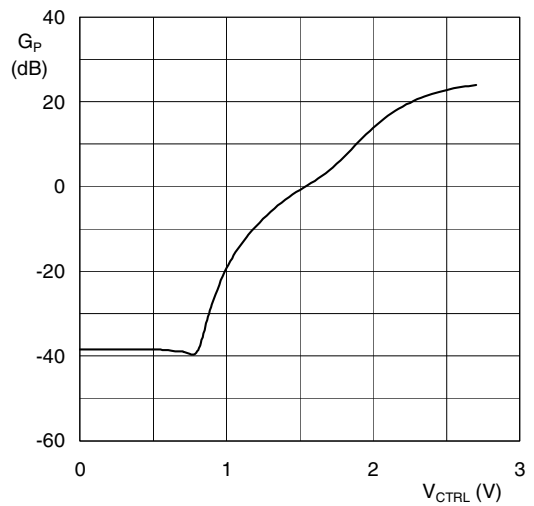
V<sub>S</sub> = 3 V; V<sub>CTRL</sub> = 2.7 V.

Fig.3 Load power as a function of the drive power; typical values.



V<sub>S</sub> = 3 V; P<sub>D</sub> = -14 dBm; f = 1.9 GHz.

Fig.4 Power gain as a function of control voltage; typical values.

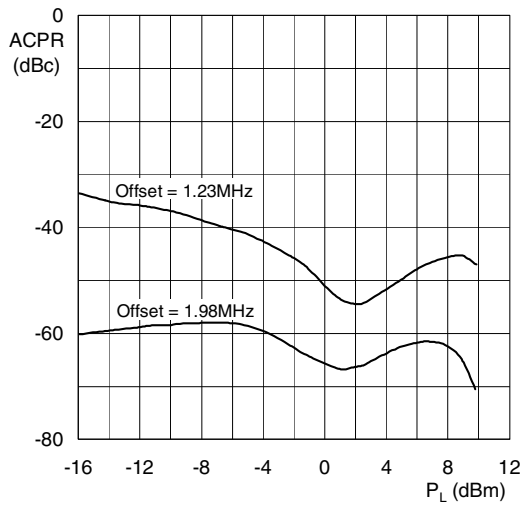


V<sub>S</sub> = 3 V; P<sub>D</sub> = -14 dBm; f = 836 MHz.

Fig.5 Power gain as a function of control voltage; typical values.

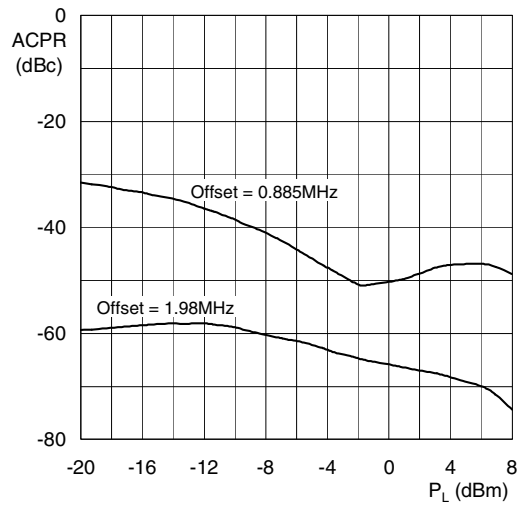
MMIC variable gain amplifier

BGA2031/1



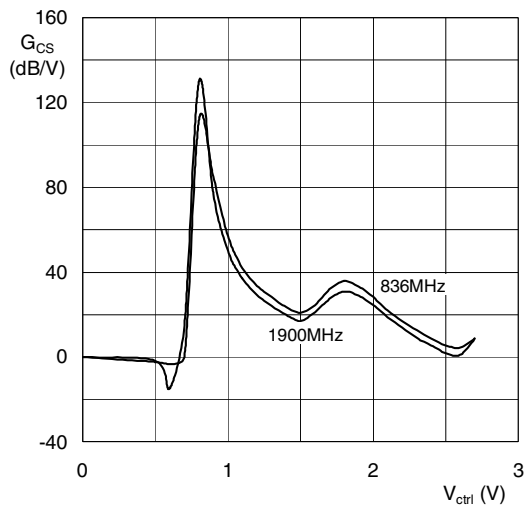
$V_S = 3\text{ V}$ ;  $f = 1.9\text{ GHz}$ ;  $P_D = -12.8\text{ dBm}$ .

Fig.6 Adjacent channel power rejection as a function of the load power; typical values.



$V_S = 3.6\text{ V}$ ;  $f = 836\text{ MHz}$ ;  $P_D = -16\text{ dBm}$ .

Fig.7 Adjacent channel power rejection as a function of the load power; typical values.



$V_S = 3\text{ V}$ ;  $P_D = -14\text{ dBm}$ .

Fig.8 Gain control slope as a function of the control voltage; typical values.

MMIC variable gain amplifier

BGA2031/1

ELECTRICAL BLOCK DIAGRAM

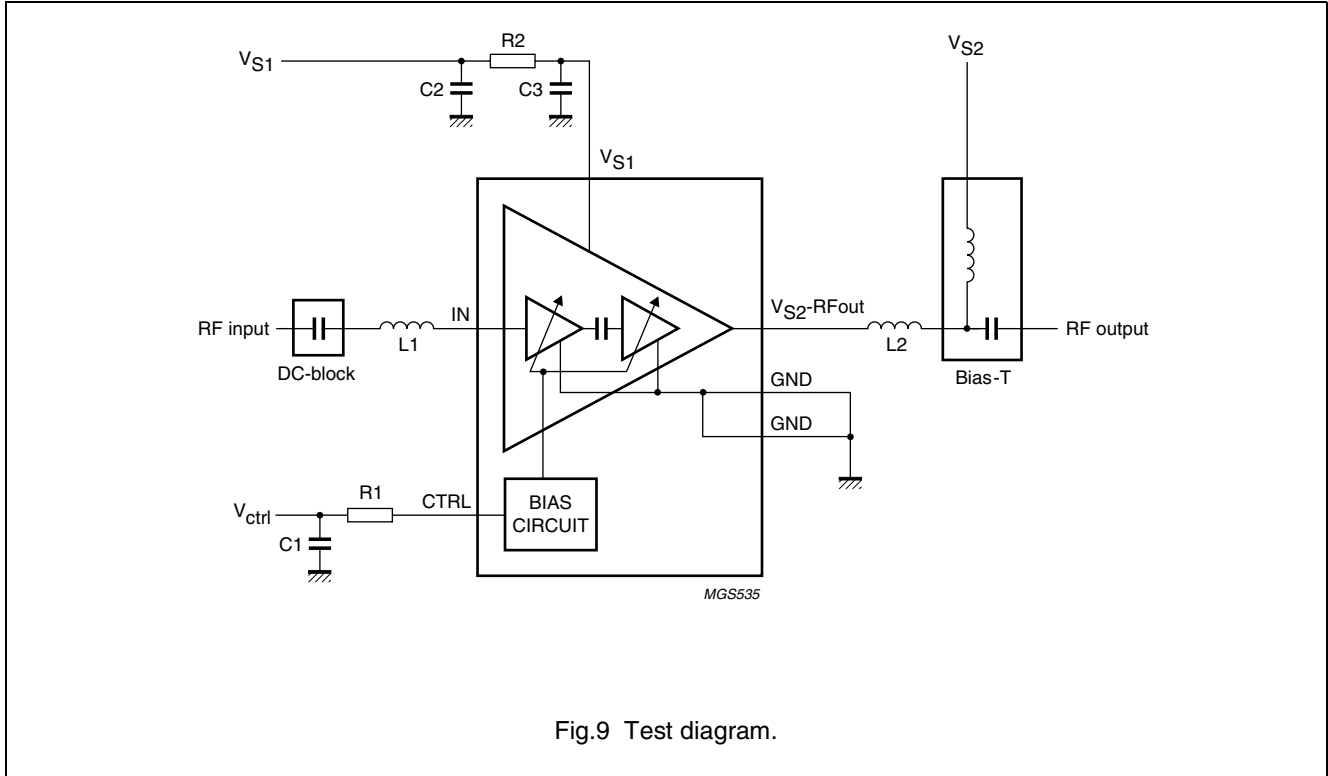


Fig.9 Test diagram.

List of components (see Fig.3)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	multilayer ceramic chip capacitor	10 nF	0603	tbf
C2	multilayer ceramic chip capacitor	22 nF	0603	tbf
C3	multilayer ceramic chip capacitor	1.5 nF	0603	tbf
L1, L2	stripline; note 1	50 Ω		tbf
R1	SMD resistor	22 Ω; 0.16 W	0603	tbf
R2	SMD resistor	2.4 Ω; 0.16 W	0603	tbf

Note

1. The striplines are on a gold plated double copper-clad printed-circuit board ( $\epsilon_r = 6.15$ ), board thickness = 0.64 mm, copper thickness = 35 μm, gold thickness = 5 μm.

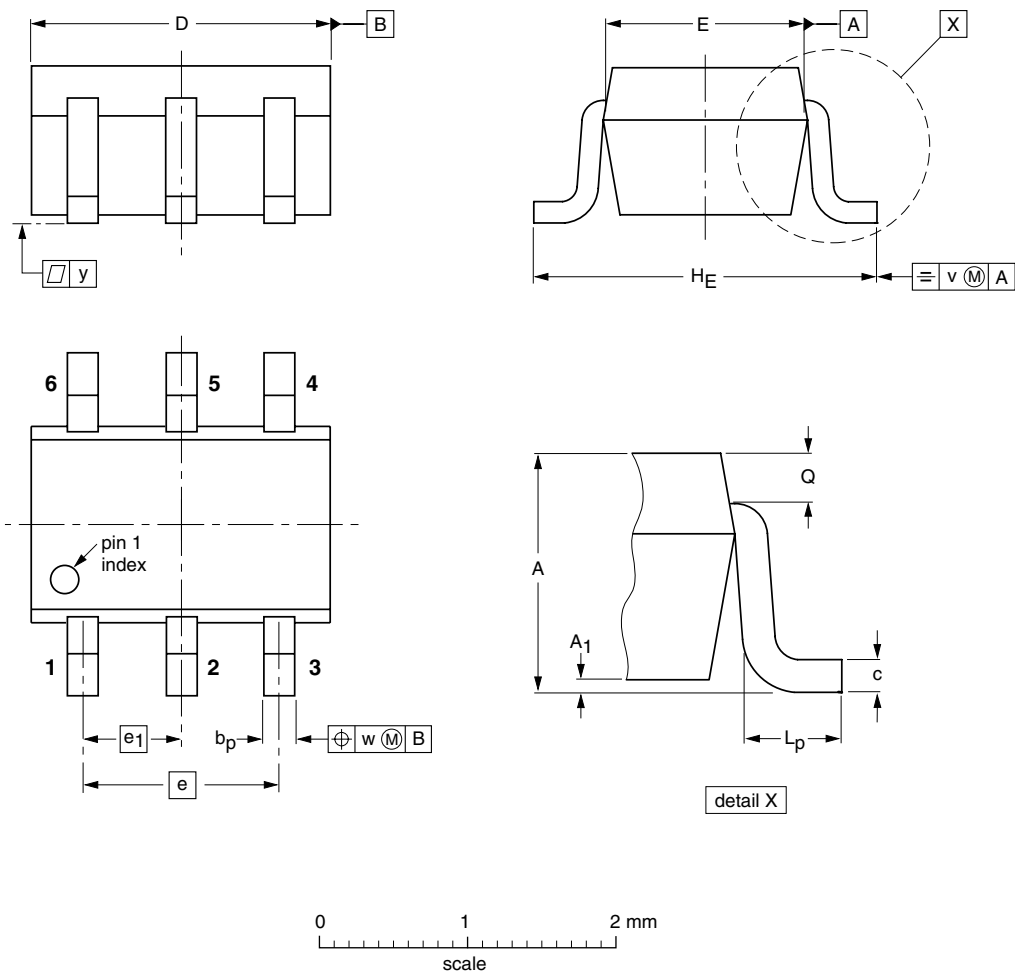
MMIC variable gain amplifier

BGA2031/1

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28



## MMIC variable gain amplifier

BGA2031/1

**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**Argentina:** see South America

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**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

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**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
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**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

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Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

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Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

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**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
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**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

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**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

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Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
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**Pakistan:** see Singapore

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Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Al.Jerozolimskie 195 B, 02-222 WARSAW,  
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Tel. +27 11 471 5401, Fax. +27 11 471 5398

**South America:** Al. Vicente Pinzon, 173, 6th floor,  
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Tel. +55 11 821 2333, Fax. +55 11 821 2382

**Spain:** Balmes 22, 08007 BARCELONA,  
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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

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