

# DATA SHEET

## **BSH301**

Dual N-channel enhancement  
mode MOS transistor

Objective specification

1999 Apr 06

# Dual N-channel enhancement mode MOS transistor

# BSH301

### FEATURES

- 40 mΩ on-state resistance at 2.5 V gate drive
- $R_{DSon}$  rating down to 1.8 V
- ESD gate protection.

### APPLICATIONS

- Li-Ion safety switch
- Power management.

### DESCRIPTION

Two N-channel enhancement mode MOS transistors in an 8-pin plastic TSSOP8 package.

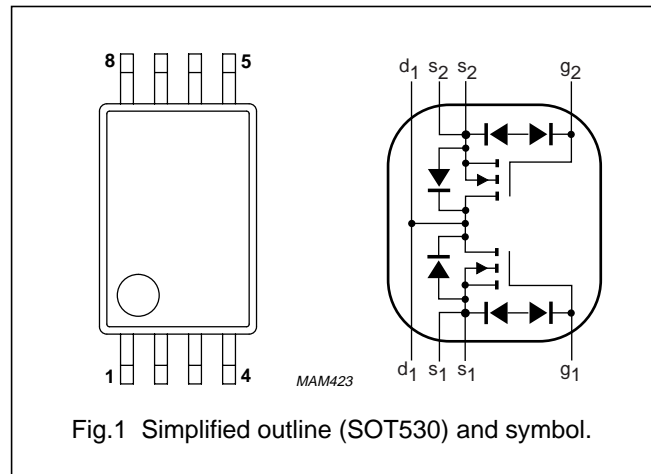


Fig.1 Simplified outline (SOT530) and symbol.

### PINNING SOT530 (TSSOP8)

PIN	SYMBOL	DESCRIPTION
1	d1	drain 1
2	s1	source 1
3	s1	source 1
4	g1	gate 1
5	g2	gate 2
6	s2	source 2
7	s2	source 2
8	d1	drain 1

### CAUTION

The device is supplied in an antistatic package. The gate inputs must be protected against static discharge during transport or handling.

### QUICK REFERENCE DATA

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	20	V
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = 1.25 \text{ A}$	–	1	V
$V_{GS}$	gate-source voltage (DC)		–	$\pm 8$	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	0.4	–	V
$I_D$	drain current (DC)	$T_S = 80 \text{ }^\circ\text{C}; \text{note 1}$	–	5	A
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}; I_D = 3.5 \text{ A}$	–	0.04	$\Omega$
$P_{tot}$	total power dissipation	$T_S = 80 \text{ }^\circ\text{C}$	–	1.75	W

### Note

1.  $T_S$  is the temperature at the soldering of the drain lead.

Full Data Sheet will appear: on WWW (Internet; details in front section/back of this HB/CD-ROM) or updated Loose leaf

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per FET</b>					
$V_{DS}$	drain-source voltage (DC)		–	20	V
$V_{GS}$	gate-source voltage (DC)		–	±8	V
$I_D$	drain current (DC)	$T_S = 80\text{ °C}$ ; note 1	–	5	A
$I_{DM}$	peak drain current	note 2	–	20	A
$P_{tot}$	total power dissipation	$T_S = 80\text{ °C}$ ; note 3	–	1.75	W
		$T_{amb} = 25\text{ °C}$ ; note 4	–	1.85	W
		$T_{amb} = 25\text{ °C}$ ; note 5	–	0.95	W
$T_{stg}$	storage temperature		–55	+150	°C
$T_j$	operating junction temperature		–55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_S = 80\text{ °C}$	–	1.75	A
$I_{SM}$	peak pulsed source current	note 2	–	7	A

**Notes**

- $T_S$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Maximum permissible dissipation per transistor. Both devices may be loaded up to 3.5 W at the same time.
- Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with  $R_{th\ a-tp}$  (ambient to tie-point) of 27.5 °C/W.
- Maximum permissible dissipation per transistor. Device mounted on a printed-circuit board with  $R_{th\ a-tp}$  (ambient to tie-point) of 90 °C/W.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

135002/00/01/pp5

Date of release: 1999 Apr 06

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