# DATA SHEET

# CGY2030M
## DECT 500 mW power amplifier

Product specification
Supersedes data of 1996 Jul 12
File under Integrated Circuits, IC17

1997 Jan 17

Philips
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# DECT 500 mW power amplifier CGY2030M

## FEATURES

- Power Amplifier (PA) overall efficiency 40%
- 27 dB gain
- 0 dBm input power
- Operation possible without negative supply
- Wide operating temperature range –30 to +85 °C
- SSOP16 package.

## GENERAL DESCRIPTION

The CGY2030M is a GaAs Monolithic Microwave Integrated Circuit (MMIC) power amplifier specifically designed to operate at 3.6 V battery supply. When power control is not required, it can be operated without negative supply voltage.

## APPLICATIONS

- 1.88 to 1.9 GHz transceivers for DECT applications
- 2 GHz transceivers (PHS, DCS).

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER (1) | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | positive supply voltage | – | 3.2 | – | V |
| $I_{DD}$ | positive peak supply current | – | 400 | – | mA |
| $P_o$ | output power | – | 27 | – | dBm |
| $T_{amb}$ | operating ambient temperature | –30 | – | +85 | °C |

**Note**

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| CGY2030M | SSOP16 | plastic shrink small outline package; 16 leads; body width 4.4 mm | SOT369-1 |

## BLOCK DIAGRAM

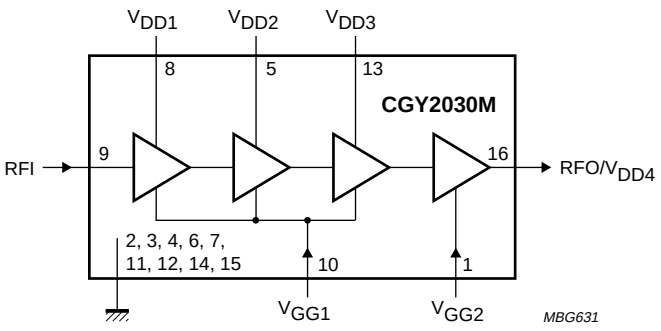



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{GG2}$ | 1 | fourth stage negative gate supply voltage |
| GND | 2 to 4 | ground |
| $V_{DD2}$ | 5 | second stage supply voltage |
| GND | 6 and 7 | ground |
| $V_{DD1}$ | 8 | first stage supply voltage |
| RFI | 9 | PA input |
| $V_{GG1}$ | 10 | first second and third stages negative gate supply voltage |
| GND | 11 and 12 | ground |
| $V_{DD3}$ | 13 | third stage supply voltage |
| GND | 14 and 15 | ground |
| RFO/$V_{DD4}$ | 16 | PA output and fourth stage supply voltage |

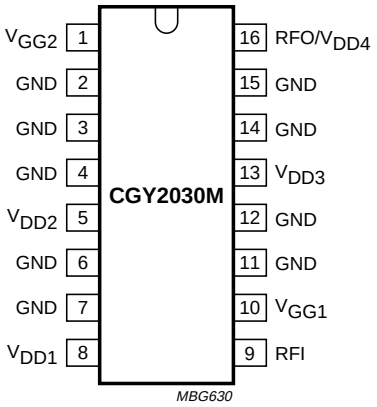



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

### Amplifier

The CGY2030M is a 4-stage GaAs MESFET power amplifier capable of delivering 500 mW (typ.) at 1.9 GHz into a 50 Ω load. Each amplifier stage has an open-drain configuration. The drains have to be loaded externally by adequate reactive circuits which must also provide a DC path to the supply.

The amplifier can be switched off by means of an external PNP series switch connected between the battery and the amplifier drains. This switch can also be used to vary the actual supply voltage applied to the amplifier and hence, control the output power.

This device is specifically designed to work with a maximum duty factor of 25%.

### Biasing

Two modes of operation are possible:

- Mode 1
- Mode 2.

MODE 1

In the first mode, the pins $V_{GG1}$ and $V_{GG2}$ are simply connected together to the ground via resistors (10 kΩ in the evaluation board; see Fig.4). The amplifier biases itself internally to a negative voltage by action of the incoming RF signal. In this mode, power control cannot be achieved by varying the amplifier supply voltage; therefore it is suitable only for applications where power control is not required such as DECT.

MODE 2

If a negative bias is available, a second mode of operation is possible, in which the amplifier is biased by providing adequate negative voltages at pins $V_{GG1}$ and $V_{GG2}$. In this mode, the amplifier internal bias does not depend on the incoming RF level, nor on the drain voltage, so that power control is possible by variation of the supply voltage.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | operating supply voltage | | – | – | 5.2 | V |
| $V_{DD} - V_{GG}$ | voltage difference between supply voltage and gate bias voltage | no input signal | – | – | 8 | V |
| $T_{j(max)}$ | maximum operating junction temperature | | – | – | 150 | °C |
| $P_{tot}$ | total power dissipation | | – | – | 400 | mW |
| $T_{stg}$ | IC storage temperature | | –55 | – | +125 | °C |

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th\ j\text{-}a}$ | thermal resistance from junction to ambient in free air | 145 | K/W |

## HANDLING

Do not operate or store near strong electrostatic fields. Meets class 1 ESD test requirements [Human Body Model (HBM)], in accordance with *"MIL STD 883C - method 3015"*.

## DC CHARACTERISTICS

$V_{DD}$ = 3.2 V; $T_{amb}$ = 25 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Pins RFO/$V_{DD4}$, $V_{DD3}$, $V_{DD2}$ and $V_{DD1}$** | | | | | | |
| $V_{DD}$ | positive supply voltage | | 2.6 | 3.2 | 4.2 | V |
| $I_{DD}$ | positive peak supply current | | – | 400 | 500 | mA |
| **Pins $V_{GG1}$ and $V_{GG2}$; in mode 2** | | | | | | |
| $V_{GG1}$ | bias voltage for input stages | note 1 | – | –1.2 | – | V |
| $V_{GG2}$ | bias voltage for output stage | note 1 | – | –2.0 | – | V |
| $I_{GG(tot)}$ | total gate peak current | note 2 | –1 | – | +1 | mA |

**Notes**

1. Negative voltages $V_{GG1}$ and $V_{GG2}$ must be applied before supply voltage $V_{DD}$.
2. Due to non linear effects at high power levels, the gate current can be either negative or positive.

## AC CHARACTERISTICS

$V_{DD}$ = 3.2 V; $f_{RF}$ = 1900 MHz; $P_i$ = 0 dBm; $T_{amb}$ = 25 °C; duty factor δ = 25%; 50 Ω impedance system; measured and guaranteed on CGY2030M evaluation board (see Fig.4).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $P_i$ | input power | note 1 | –3 | – | +5 | dBm |
| δ | duty factor | | – | – | 25 | % |
| $f_{RF}$ | operating frequency | | – | 1900 | – | MHz |
| **Measured in mode 1; without negative biasing; $V_{GG1}$ and $V_{GG2}$ connected to ground** | | | | | | |
| $P_o$ | output power | | 26 | 27 | 28.5 | dBm |
| η | efficiency | | – | 40 | – | % |
| $P_{leak}$ | RF leakage to output in power off state | $V_{DD}$ = 0 V | – | –40 | – | dBm |
| H2, H3 | second and third harmonics level | | – | –35 | – | dBc |
| Stab | stability (spurious levels) | note 2 | – | –60 | – | dBc |
| **Measured in mode 2; with negative biasing at pins $V_{GG1}$ and $V_{GG2}$** | | | | | | |
| $P_o$ | output power | | 25.5 | 26.5 | 28 | dBm |
| η | efficiency | | – | 35 | – | % |
| $P_{leak}$ | RF leakage to output in power off state | $V_{DD}$ = 0 V | – | –50 | – | dBm |

**Notes**

1. Self biasing guaranteed in mode 1 at minimum input power (–3 dBm) and minimum supply voltage $V_{DD}$ (2.6 V).
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 seconds test period.

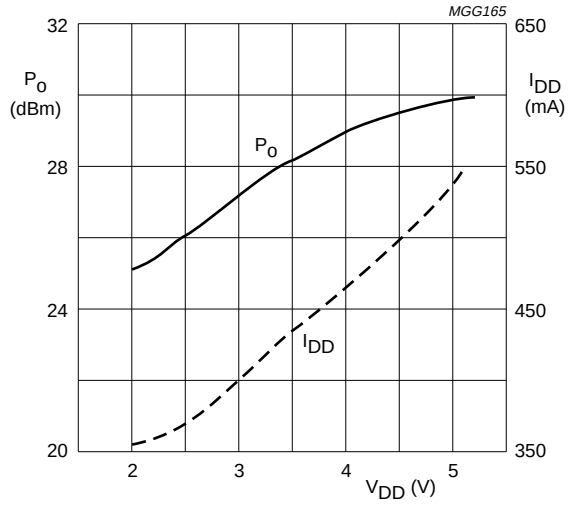
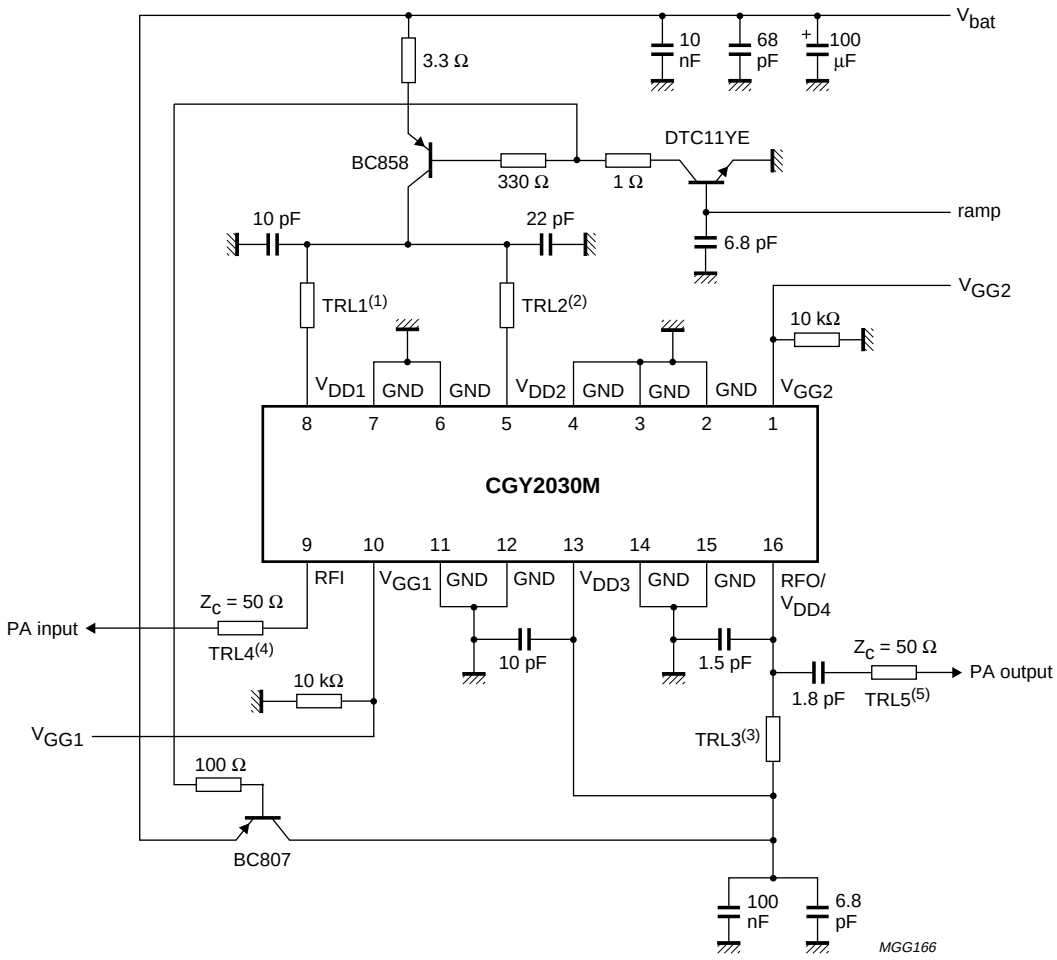



Fig.3 Typical power and current characteristics in mode 1.

## APPLICATION INFORMATION

The CGY2030M is operated and tested in accordance with the circuit diagram shown in Fig.4. Supply voltage switching is achieved by two bipolar PNP transistors. One transistor switches the first and second stages and the other switches the third and fourth stages.

By switching on the last amplifier stages with some delay compared to the first stages, it is possible to get the last stages already self-biased before their supply voltage has reached its steady state value. This enables smooth power up-ramping without any power overshoot. A simpler drain switching circuit can be used if the amplifier is operated with negative biasing of the pins $V_{GG1}$ and $V_{GG2}$.




Thickness: 0.8 mm; substrate: FR4; $\varepsilon_r$ = 4.7.

(1) TRL1: width = 500 µm; length = 11200 µm.

(2) TRL2: width = 500 µm; length = 7770 µm.

(3) TRL3: width = 300 µm; length = 15450 µm.

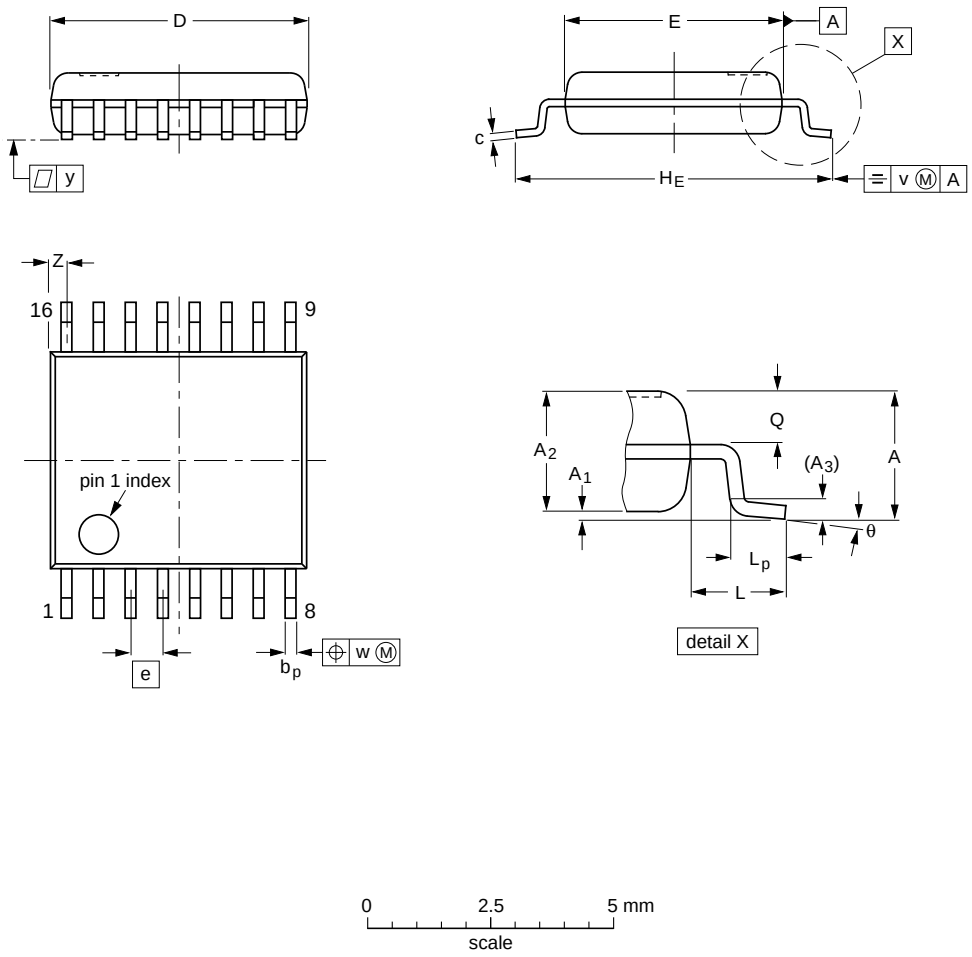
(4) TRL4: width = 1600 µm; length = 12000 µm.

(5) TRL5: width = 1600 µm; length = 11000 µm.

Fig.4 Evaluation board schematic.

## PACKAGE OUTLINE

**SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm** **SOT369-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.5 | 0.15<br>0.00 | 1.4<br>1.2 | 0.25 | 0.32<br>0.20 | 0.25<br>0.13 | 5.30<br>5.10 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.45 | 0.65<br>0.45 | 0.2 | 0.13 | 0.1 | 0.48<br>0.18 | $10^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT369-1 | | | | | | ~~94-04-20~~<br>95-02-04 |

## SOLDERING

### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1)**.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## DEFINITIONS

| | |
|---|---|
| **Data sheet status** | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
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**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

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Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,
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Tel. +7 095 755 6918, Fax. +7 095 755 6919

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

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**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,
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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2870, Fax. +886 2 2134 2874

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,
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Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
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**Ukraine**: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

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Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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Printed in The Netherlands 437027/1200/03/pp12 Date of release: 1997 Jan 17 Document order number: 9397 750 01565


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