# DATA SHEET

# CGY2105ATS
## High dynamic range dual LNA MMIC

Preliminary specification
File under Integrated Circuits, IC17

1999 Dec 23

Philips Semiconductors

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## FEATURES

- Dual Low Noise Amplifier (LNA) Monolithic Microwave Integrated Circuit (MMIC)
- Typical noise figure of 0.55 dB
- Typical gain of 16.3 dB at 1810 MHz
- Input IP3 of 13.5 dBm at 1810 MHz
- Low current of 58 mA at 2.5 V for each channel
- Low cost SSOP16 plastic package.

## APPLICATIONS

- DCS1800
- PCS1900.

## GENERAL DESCRIPTION

The CGY2105 is a dual Gallium Arsenide (GaAs) MMIC amplifier designed for use in very low noise figure applications, where high linearity is also required.

Excellent tracking between the two amplifiers is obtained. Gain and noise figure variations with temperature are very small.

The device is suitable for use in DCS1800 and PCS1900 base station applications.

It also provides high gain and very low noise performance at frequencies between 1.0 and 2.5 GHz, as used in Wireless Local Area Network (WLAN) applications.

A rematching of the application board might be necessary for optimum performance.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| CGY2105ATS | SSOP16 | plastic shrink small outline package; 16 leads; body width 4.4 mm | SOT369-1 |

## BLOCK DIAGRAM

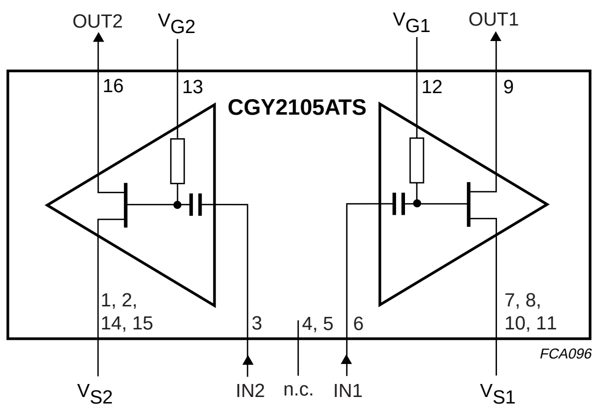



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{S2}$ | 1, 2, 14 and 15 | amplifier 2 source |
| IN2 | 3 | amplifier 2 input |
| n.c. | 4 | not connected |
| n.c. | 5 | not connected |
| IN1 | 6 | amplifier 1 input |
| $V_{S1}$ | 7, 8, 10 and 11 | amplifier 1 source |
| OUT1 | 9 | amplifier 1 drain output |
| $V_{G1}$ | 12 | amplifier 1 gate bias |
| $V_{G2}$ | 13 | amplifier 2 gate bias |
| OUT2 | 16 | amplifier 2 drain output |

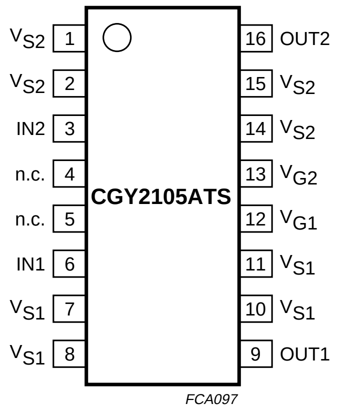



Fig.2 Pin configuration.

## LIMITING VALUES

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | – | – | 5 | V |
| $V_{GS}$ | gate-source voltage | | –3 | – | +1 | V |
| $V_{DG}$ | drain-gate voltage | | – | – | 7 | V |
| $V_{supply}$ | positive supply voltage | see Chapter “Application and test information” | – | – | 6 | V |
| $V_{neg}$ | negative supply voltage | see Chapter “Application and test information” | –6 | – | – | V |
| $T_{amb}$ | ambient temperature | | –40 | – | +85 | °C |
| $T_j$ | junction temperature | | – | – | 150 | °C |
| $T_{stg}$ | storage temperature | | – | – | 150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ < 85 °C | – | – | 430 | mW |

## THERMAL CHARACTERISTICS

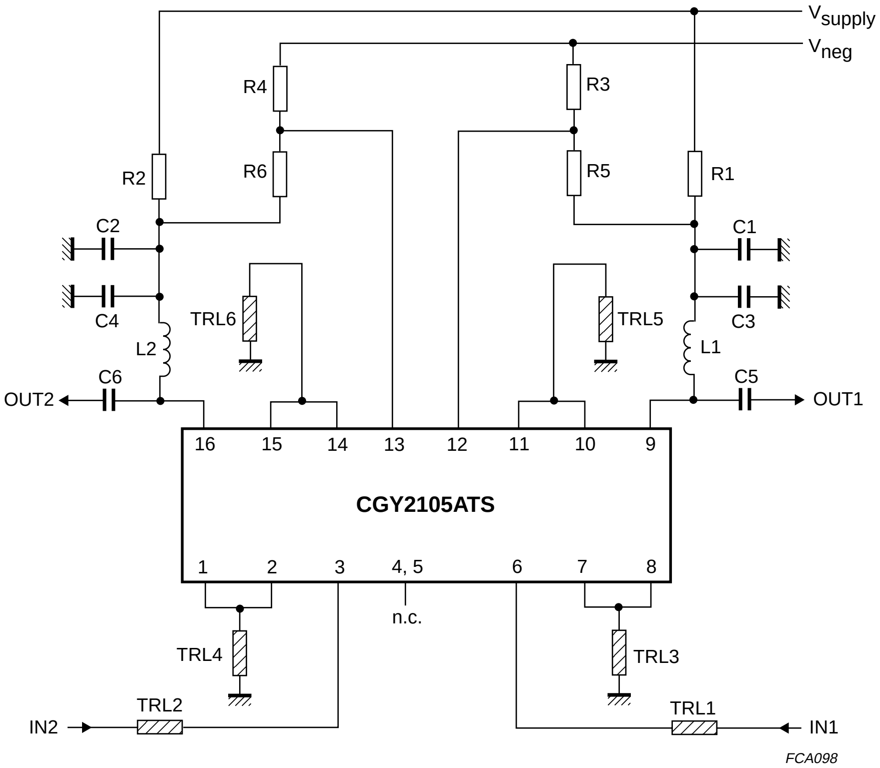
| SYMBOL | PARAMETER | VALUE | UNIT |
|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | 138 | K/W |

## CHARACTERISTICS

$T_{amb}$ = 25 °C; measured and guaranteed only for the application shown in Chapter “Application and test information”; unless otherwise specified.

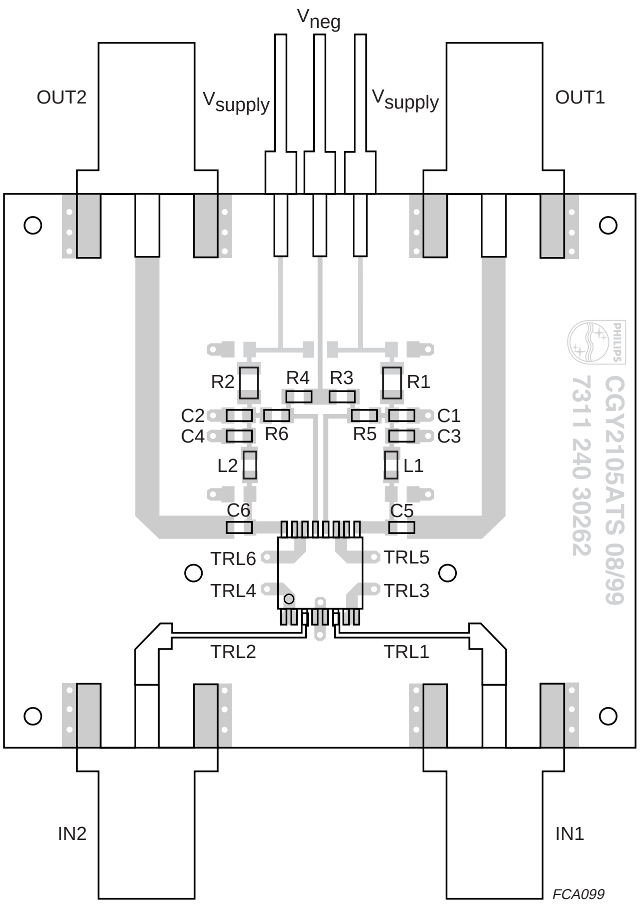
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $I_{supply}$ | positive supply current (for each LNA) | $V_{supply}$ = 5.0 V; $V_{neg}$ = –5.0 V | 42 | 58 | 72 | mA |
| $I_{neg}$ | negative supply current (for each LNA) | $V_{supply}$ = 5.0 V; $V_{neg}$ = –5.0 V | – | 0.3 | 0.4 | mA |
| **Amplifiers: $V_{supply}$ = 5.0 V; $V_{neg}$ = –5.0 V; $Z_0$ = 50 Ω; both LNAs biased; duty cycle 100%** | | | | | | |
| $f_i$ | input frequency | | 1710 | – | 1910 | MHz |
| G | gain | $f_i$ = 1710 MHz | 16 | 16.9 | 17.8 | dB |
| | | $f_i$ = 1710 to 1910 MHz | 14.8 | 16.3 | 17.8 | dB |
| $\Delta G_{(T)}$ | gain variation with temperature | –40 °C < $T_{amb}$ < +85 °C | – | ±0.45 | – | dB |
| NF | noise figure | | – | 0.55 | 0.8 | dB |
| $\Delta NF_{(T)}$ | noise figure variation with temperature | –40 °C < $T_{amb}$ < +85 °C | – | ±0.25 | – | dB |
| $IP3_i$ | input third-order intercept point | Δf = ±0.5 MHz | 11 | 13.5 | – | dBm |
| $\Delta IP3_{i(T)}$ | input third-order intercept point variation with temperature | –40 °C < $T_{amb}$ < +85 °C | – | ±0.45 | – | dB |
| $ISO_r$ | reverse isolation | | 18 | 20 | – | dB |
| $ISO_i$ | isolation between inputs | | 21 | 23 | – | dB |
| $s_{11}$ | input reflection coefficient | 50 Ω source | – | –8.5 | – | dB |
| $s_{22}$ | output reflection coefficient | 50 Ω load | – | –22 | – | dB |

## APPLICATION AND TEST INFORMATION




The demonstration board has been optimized for a centre frequency of 1.8 GHz.
The MMIC s-parameters (typical values) in a range from 0.1 to 6 GHz are available on request.

Fig.3 Application diagram.




Designed for a centre frequency of 1.8 GHz.

Fig.4 Application PCB layout.

**Table 1** List of components; see Figs 3 and 4

| COMPONENT | DESCRIPTION | VALUE | REFERENCE |
|---|---|---|---|
| C1, C2 | decoupling capacitor | 1 nF | Philips; NPO, 0603 |
| C3, C4 | decoupling capacitor | 47 pF | Philips; NPO, 0603 |
| C5, C6 | decoupling capacitor | 47 pF | Philips; NPO, 0603 |
| R1, R2 | drain biasing resistor | 39 Ω | Philips; XR7, 0805 |
| R3, R4 | gate biasing resistor | 15 kΩ | Philips; 0603 |
| R5, R6 | gate biasing resistor | 10 kΩ | Philips; 0603 |
| L1, L2 | drain biasing inductor | 18 nH | Coilcraft; 0603 |

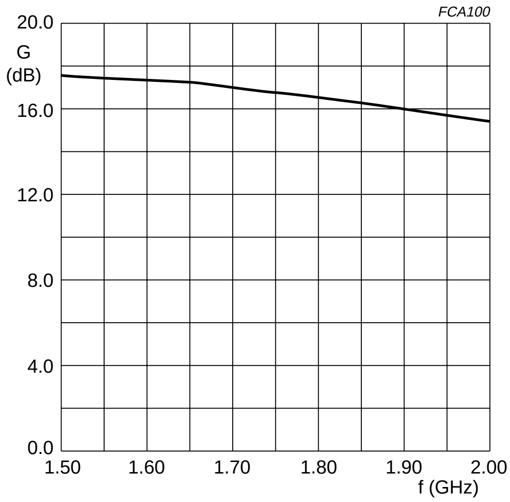
**Table 2** Transmission lines; see Figs 3 and 4

| COMPONENT | $Z_0$ | LENGTH IN λ | LENGTH IN mm(1) | WIDTH IN mm(1) |
|---|---|---|---|---|
| TRL1, TRL2 | 100 Ω | 0.08λ at 1800 MHz | 10 mm | 0.25 mm |
| TRL3, TRL4 | 100 Ω | 0.08λ at 1800 MHz | 4 mm | 0.80 mm |
| TRL5, TRL6 | 100 Ω | 0.08λ at 1800 MHz | 3.4 mm | 0.80 mm |

**Note**

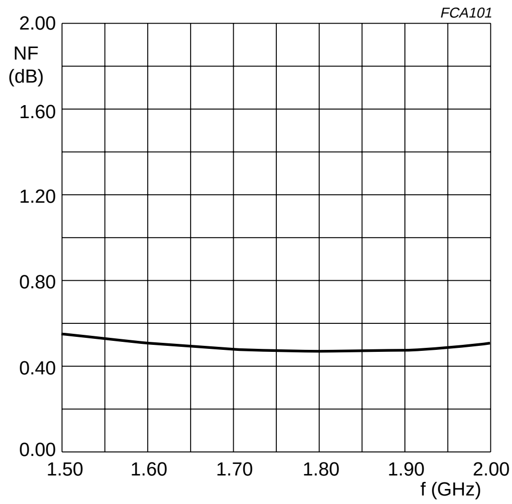
1. Transmission line lengths and widths in mm are valid for a double sided PCB; thickness of 0.8 mm in FR4 material (ε = 4.7).

## Measured performance



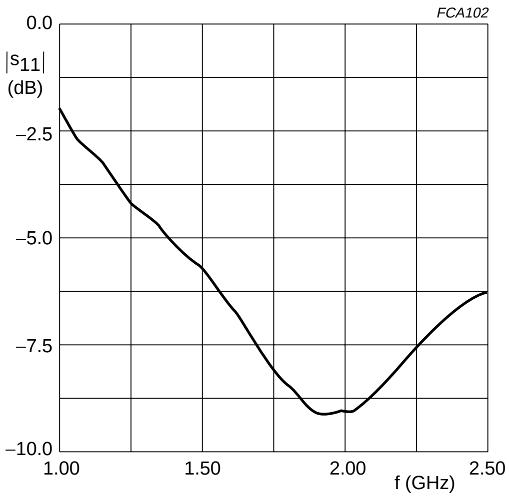

$V_{supply}$ = 5 V; $V_{neg}$ = –5 V.

Fig.5 Gain as a function of the frequency.



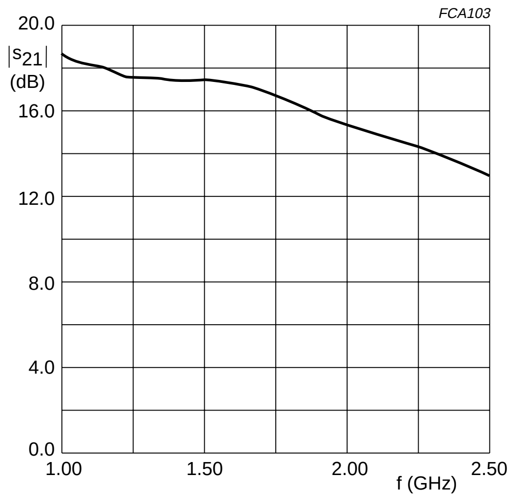

$V_{supply}$ = 5 V; $V_{neg}$ = –5 V.

Fig.6 Noise figure as a function of the frequency.



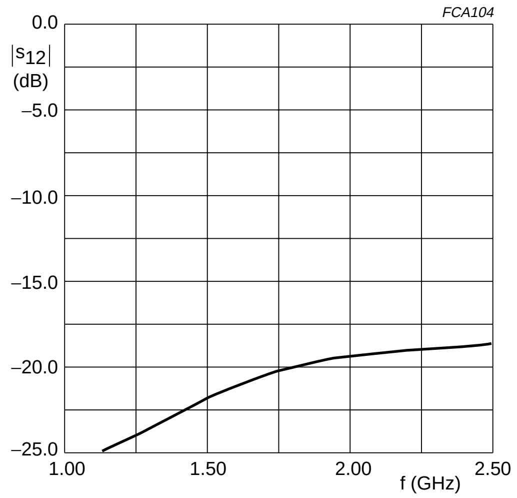

$V_{supply}$ = 5 V; $V_{neg}$ = –5 V.

Fig.7 Input reflection coefficient $|s_{11}|$ as a function of the frequency.



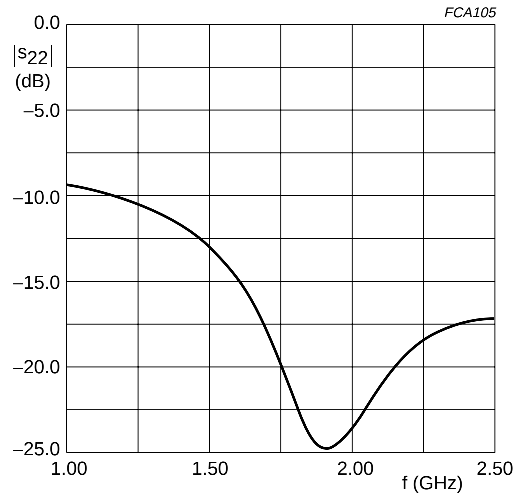

$V_{supply}$ = 5 V; $V_{neg}$ = –5 V.

Fig.8 Forward transmission coefficient $|s_{21}|$ as a function of the frequency.



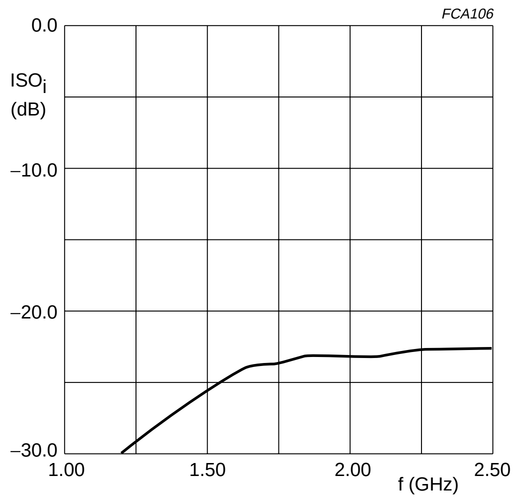

$V_{supply}$ = 5 V; $V_{neg}$ = −5 V.

Fig.9 Reverse transmission coefficient $|s_{12}|$ as a function of the frequency.



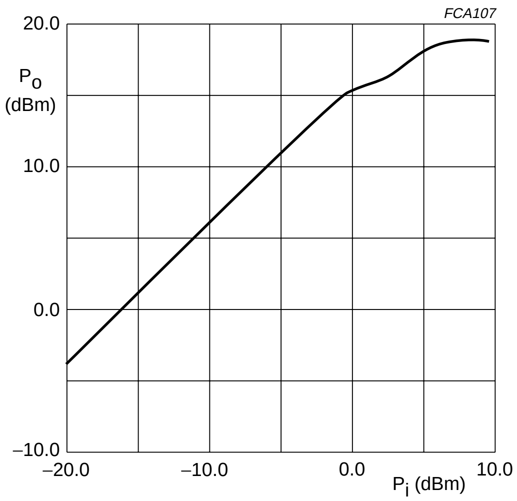

$V_{supply}$ = 5 V; $V_{neg}$ = −5 V.

Fig.10 Output reflection coefficient $|s_{22}|$ as a function of the frequency.




$V_{supply}$ = 5 V; $V_{neg}$ = −5 V.

Fig.11 Isolation between RF inputs as a function of the frequency.

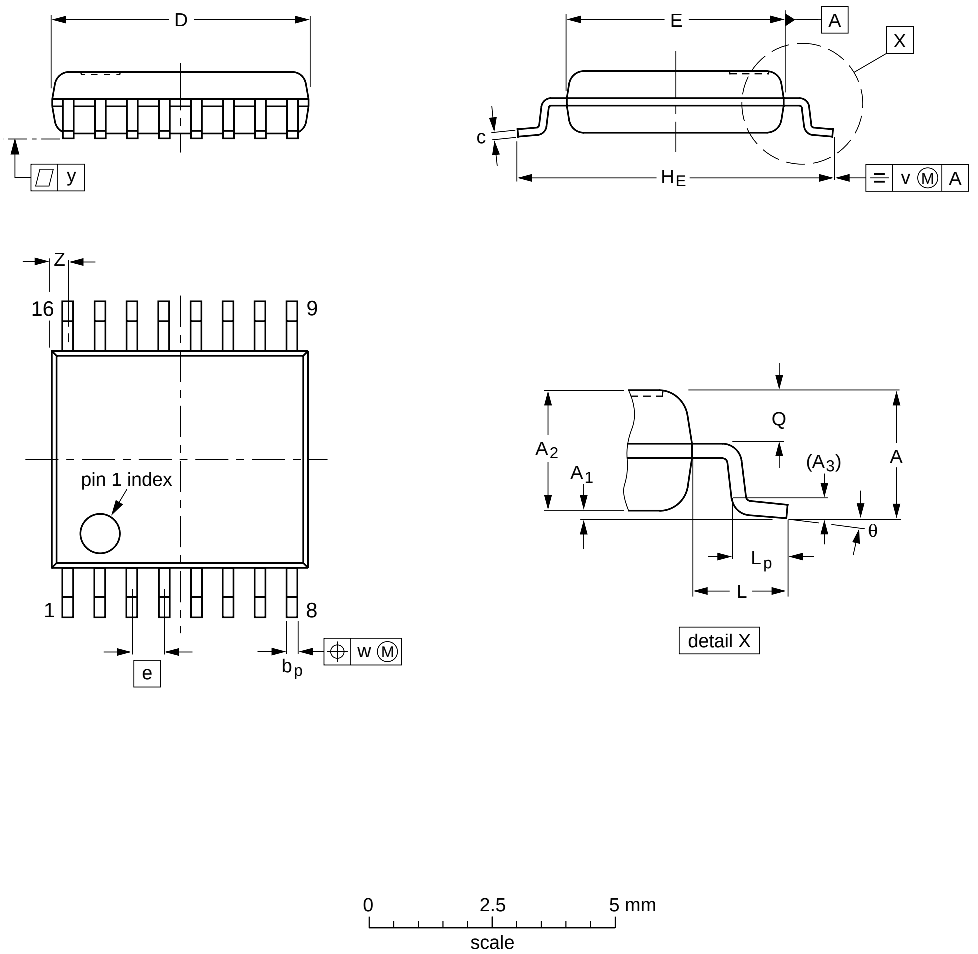



$V_{supply}$ = 5 V; $V_{neg}$ = −5 V.

Fig.12 RF output power as a function of the RF input power.

## PACKAGE OUTLINE

**SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm** **SOT369-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.5 | 0.15<br>0.00 | 1.4<br>1.2 | 0.25 | 0.32<br>0.20 | 0.25<br>0.13 | 5.30<br>5.10 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1.0 | 0.75<br>0.45 | 0.65<br>0.45 | 0.2 | 0.13 | 0.1 | 0.48<br>0.18 | $10^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT369-1 | | | | | | ~~94-04-20~~<br>95-02-04 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, LFBGA, SQFP, TFBGA | not suitable | suitable |
| HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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**NOTES**

## NOTES

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