

DATA SHEET

TEA1081

Supply circuit with power-down for
telephone set peripherals

Product specification
Supersedes data of February 1988
File under Integrated Circuits, IC03

September 1994

Philips Semiconductors



PHILIPS

Supply circuit with power-down for telephone set peripherals

TEA1081

FEATURES

- High input impedance for audio signals
- Low DC series resistance
- High output current
- Large audio signal handling capability
- Low distortion
- Two modes of operation:
 - output voltage that follows the DC line voltage
 - regulated output voltage
- Power-down input
- Low number of external components.

GENERAL DESCRIPTION

The TEA1081 is an integrated circuit for use in line-powered telephone sets to supply peripheral circuits for extended dialling and/or loudspeaker facilities.

The IC uses a part of the surplus line current normally drawn by the voltage regulator of the speech/transmission circuit. A power-down function isolates the IC from its load and reduces the input current.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_O	DC output voltage		2.0	–	10.0	V
ΔV_{LN-O}	voltage drop from line to output	$I_O = 0$ mA	–	0.5	–	V
R_S	internal series resistance		–	20	–	Ω
I_O	output current (pin 7) TEA1081 TEA1081T	$V_{LN} = 4$ V	–	–	30 20	mA mA
$V_{LN(rms)}$	AC line voltage (RMS value)	$V_{LN} = 4$ V; $I_O = 15$ mA; THD = 2%	–	1.5	–	V
I_{INT}	internal supply current	$V_{LN} = 4$ V; $I_O = 0$ mA; PD = LOW; $V_{SP} = V_O$	–	0.8	1.4	mA
T_{amb}	operating ambient temperature		–25	–	+70	$^{\circ}\text{C}$

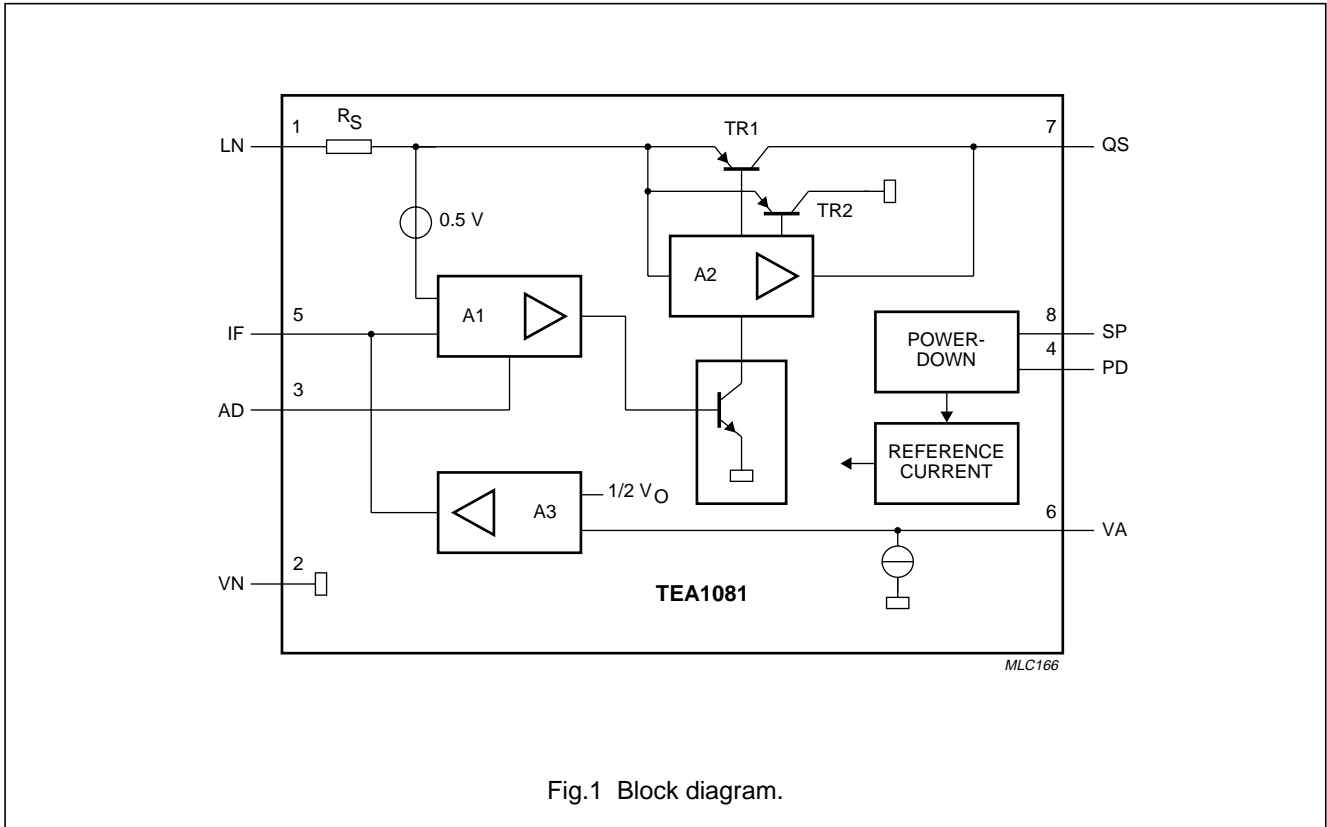
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA1081	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TEA1081T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

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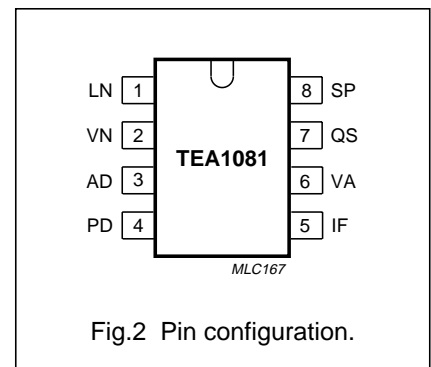
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BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
LN	1	positive line terminal
VN	2	negative line terminal
AD	3	amplifier decoupling
PD	4	power-down input
IF	5	low-pass filter input
VA	6	output voltage adjustment
QS	7	power supply output
SP	8	supply input; power-down circuit



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FUNCTIONAL DESCRIPTION

The TEA1081 is a supply interface between telephone line and peripheral devices in the telephone set. The high input impedance of the circuit allows direct connection to the telephone line (via a diode bridge). An inductor function is obtained by amplifier A1, resistor R_S (see Fig.1) and an external low-pass RC filter.

Under the control of amplifier A2, transistor TR1 supplies peripheral devices and transistor TR2 minimizes line signal distortion by momentarily diverting input current to ground whenever the instantaneous value of the line voltage drops below the output voltage.

Internal circuits are biased by a temperature and line voltage compensated reference current source.

The power-down circuit isolates the supply circuit from external circuitry.

Line terminals: LN and VN (pins 1 and 2)

The input terminals LN and VN can be connected directly to the line. The minimum DC line voltage required at the input is expressed by formula (1); see also Table 1.

$$V_{LN} = I_1 \times R_S + V_{LNmin} + V_{LN(P)} \quad (1)$$

Table 1 Explanation of formula (1).

SYMBOL	DESCRIPTION
I ₁	input current
R _S	internal series resistance
V _{LNmin}	minimum instantaneous line voltage (1.4 V at I _O = 5 mA)
V _{LN(P)}	required peak level of AC line voltage

The internal current (I_{INT}) at I_O = 0 mA is typically 0.8 mA at V_{LN} = 4 V and reaches a maximum of 1.4 mA at V_{LN} = 12 V.

Supply terminals: QS and VA (pins 7 and 6)

Peripheral devices are supplied from QS (pin 7). Two modes of output voltage regulation are available.

OUTPUT VOLTAGE FOLLOWS LINE VOLTAGE (SEE FIG.3)

The TEA1081 operates in this mode when there is no external resistor (R_V) between QS and VA (see Fig.6).

The output voltage follows the line voltage and is expressed by formula (2); see also Table 2.

$$V_O = V_{LN} - (I_1 \times R_S + 0.5) \quad (2)$$

Table 2 Explanation of formula (2).

SYMBOL	DESCRIPTION
V _{LN}	line voltage
I ₁	input current
R _S	internal series resistance

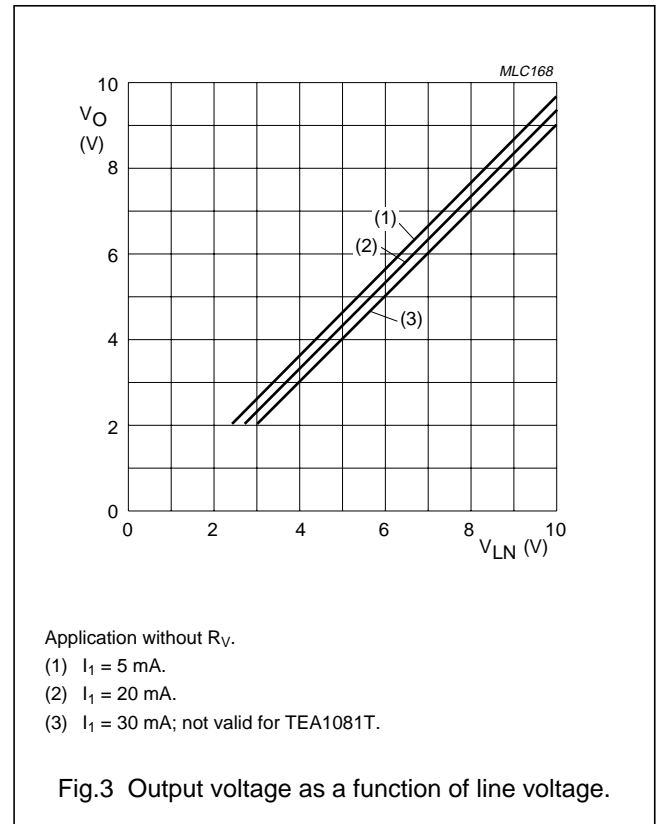
REGULATED OUTPUT VOLTAGE (SEE FIG.4)

The circuit operates in this mode when an external resistor (R_V) is connected between QS and VA (see Fig.6).

The output voltage is held constant at V_O = 2 × I₆ × R_V (V) as soon as the line voltage

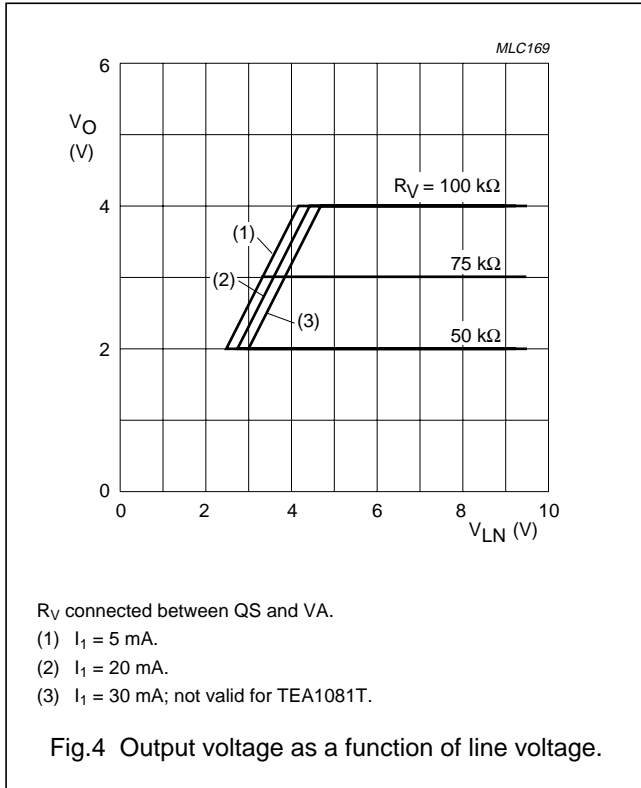
$$V_{LN} > (2 \times I_6 \times R_V + I_1 \times R_S + 0.5) \quad (V)$$

The control current I₆ is typically 20 μA.



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Input and output currents I₁ and I_O (pins 1 and 7)

The maximum available current into pin 1 (I₁) is determined by:

- The minimum line current (I_{LINEmin}) that is available for the telephone set
- The specified minimum input current (I_{LNmin}) for the speech/transmission circuit.

That is I_{1max} = I_{LINEmin} - I_{LNmin}.

At V_{LN(rms)} < 150 mV, the input current I₁ is approximately:

$$I_1 = I_{INT} + k \times I_O \text{ (mA)}$$

Where:

- I_{INT} = internal supply current (0.8 mA at V_{LN} = 4 V);
- k = correction factor (k < 1.1 for the specified output current range).

With large line signals the instantaneous line voltage may drop below V_O + 0.4 V. Normally (when V_{LN} > V_O + 0.4 V), instantaneous current flows from LN to QS (pin 1 to pin 7) to the output load.

When V_{LN} < V_O + 0.4 V, the instantaneous current is diverted to pin 2 to prevent distortion of the line signal.

Input current at V_{LN(rms)} = 1 V and without R_V approximates to:

$$I_1 = I_{INT} + 2 \times I_O \text{ (mA)}$$

The maximum supply current (within the specified output current limits) available for peripheral devices is shown by:

$$I_{Omax} = \frac{I_{LINEmin} - I_{LNmin} - I_{INT}}{2}$$

Where:

- I_{LINEmin} is the minimum line current of the telephone set;
- I_{LNmin} is the specified minimum input current of the speech/transmission circuit.

Input low-pass filter: IF (pin 5)

The input impedance between LN and VN at audio frequencies is determined by the filter elements C_L (between pins 1 and 5), R_L (between pins 5 and 7) and the internal resistor R_S (typical value 20 Ω).

At audio frequencies the TEA1081 behaves as an inductor of the value L₁ = C_L × R_L × R_S (H). The typical value of L₁ at C_L = 2.2 μF and R_L = 100 kΩ is 4.4 H.

Amplifier decoupling: AD (pin 3)

To ensure stability, a 68 pF decoupling capacitor is required between AD (pin 3) and LN (pin 1).

If I_{Omin} < 1.5 mA, a 47 pF capacitor has to be added between AD (pin 3) and VA (pin 6).

Power-down inputs: PD and SP (pins 4 and 8)

During pulse dialling or register recall, or if the input current to pin 1 is insufficient to maintain the output current, the supply to peripheral devices can be switched off by activating the PD input at pin 4. With PD = HIGH, the input current is reduced to 40 μA (typ.) at V_{LN} = 4 V and the internal circuits are isolated from the load at QS (pin 7).

The power-down circuit is supplied via the SP input (pin 8). SP can be wired to QS in conditions where V_O > V_{SPmin} during line interruptions. When V_O < V_{SPmin}, SP should be wired to an external supply point (e.g. to V_{CC} of the TEA1060 family circuit).

When power-down is not required, the PD and SP inputs can be left open-circuit.

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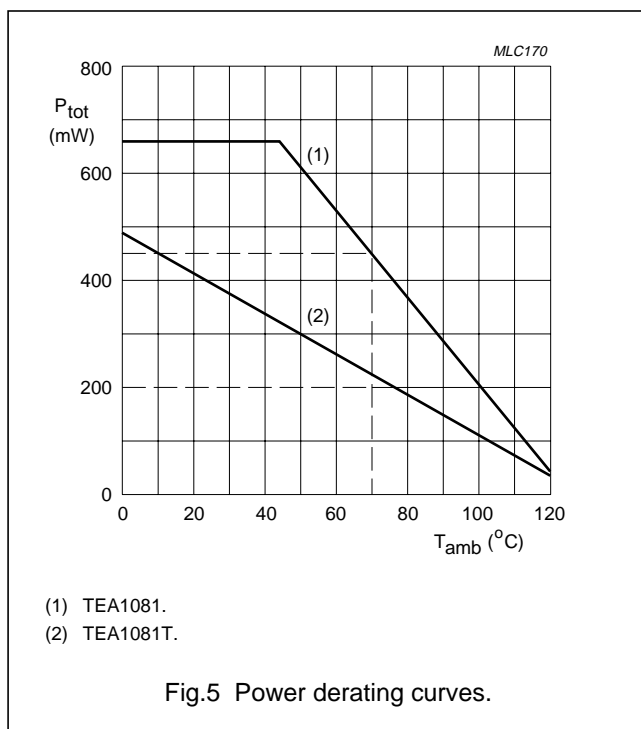
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{LN}	positive line voltage	continuous	–	12	V
		during switch-on or line interruptions	–	12.5	V
V _{LN(RM)}	repetitive peak line voltage for a 1 ms pulse per 5 s	12 Ω resistor in series with pin 1	–	28	V
V _I	input voltage (all other terminals)		V _{VN} – 0.5	V _{LN} + 0.5	V
I _I	DC input current TEA1081 TEA1081T		–	120	mA
			–	80	mA
I _I	input current (all other terminals)		–1	+1	mA
P _{tot}	total power dissipation		see Fig.5		
T _{amb}	operating ambient temperature		–25	+70	°C
T _{stg}	storage temperature		–40	+125	°C
T _j	junction temperature		–	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient in free air		
	TEA1081	120	K/W
	TEA1081T (mounted on a printed-circuit board of 50 × 50 × 1.5 mm)	260	K/W



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CHARACTERISTICS

$V_{LN} = 4\text{ V}$; $V_{LN(rms)} = 100\text{ mV}$; $I_O = 5\text{ mA}$; $f = 300\text{ to }3400\text{ Hz}$; $R_L = 100\text{ k}\Omega$; $C_L = 2.2\text{ }\mu\text{F}$; $R_V = 75\text{ k}\Omega$; $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified; see Fig.6.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{LN}	operating DC line voltage		2.5	–	12.0	V
V_{LNmin}	minimum instantaneous line voltage		–	–	1.4	V
V_{LNmax}	maximum instantaneous line voltage		12.0	–	–	V
Characteristics with $R_V = 75\text{ k}\Omega$ connected between pins 6 and 7 and $C_L = 10\text{ }\mu\text{F}$						
I_1	input current (pin 1)	$V_{LN(rms)} = 0\text{ V}$	–	5.8	–	mA
		$V_{LN(rms)} = 1.5\text{ V}$; $I_O = 15\text{ mA}$	–	30	–	mA
V_O	output voltage (pin 7)		–	3.0	–	V
ΔV_O	variation of output voltage over the ranges of: line voltage temperature temperature output current	$V_{LN} = 4\text{ to }6\text{ V}$	–	100	–	mV
		$T_{amb} = +25\text{ to }-25\text{ }^\circ\text{C}$	–	–100	–	mV
		$T_{amb} = +25\text{ to }+75\text{ }^\circ\text{C}$	–	–100	–	mV
		$I_O = 5\text{ to }20\text{ mA}$	–	–100	–	mV
I_6	control current (pin 6)		–	20	–	μA
Characteristics without R_V						
I_1	input current (pin 1)	$V_{LN(rms)} = 0\text{ V}$	–	6.0	–	mA
		$V_{LN(rms)} = 1.5\text{ V}$; $I_O = 15\text{ mA}$	–	31	–	mA
ΔV_{LN-O}	voltage drop from line to output	$I_O = 0\text{ mA}$	–	0.5	–	V
		$I_O = 15\text{ mA}$; $V_{LN(rms)} = 1.5\text{ V}$	–	1.1	–	V
I_O	output current (pin 7) TEA1081 TEA1081T		–	–	30	mA
			–	–	20	mA
R_S	internal series resistance		–	20	–	Ω
I_{INT}	internal supply current	$I_O = 0\text{ mA}$; PD = LOW; $V_{SP} = V_O$	–	0.8	1.4	mA
		$I_O = 0\text{ mA}$; PD = HIGH (note 1); $V_{SP} > 2\text{ V}$	–	40	60	μA
THD	total harmonic distortion	$V_{LN(rms)} = 1.5\text{ V}$	–	–	2	%
BRL	balance return loss	600 Ω reference	25	–	–	dB
$V_{LN(2H)}$	second harmonic level of line voltage	$f = 500\text{ Hz}$; $V_{LN} = 0\text{ dBm}$; $Z_{line} = 600\text{ }\Omega$	–	–58	–	dBm
$V_{LN(3H)}$	third harmonic level of line voltage	$f = 500\text{ Hz}$; $V_{LN} = 0\text{ dBm}$; $Z_{line} = 600\text{ }\Omega$	–	–60	–	dBm
$V_{ni(rms)}$	noise voltage on input terminal (RMS value)	$V_{LN(rms)} = 0\text{ V}$; $R_L = 600\text{ }\Omega$; P53 curve	–	–83	–	dBmp
Power-down input (pin 4)						
V_{IL}	LOW level input voltage		–	–	0.3	V
V_{IH}	HIGH level input voltage		1.5	–	V_{SP}	V
I_4	input current		–	–	10	μA

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-down input (pin 8)						
V_8	supply voltage for power-down		2	–	V_{LN}	V
I_8	supply current to power-down circuit	$V_8 = 3\text{ V}$	–	–	70	μA

Note

1. Power-down circuit supplied via external source.

APPLICATION INFORMATION

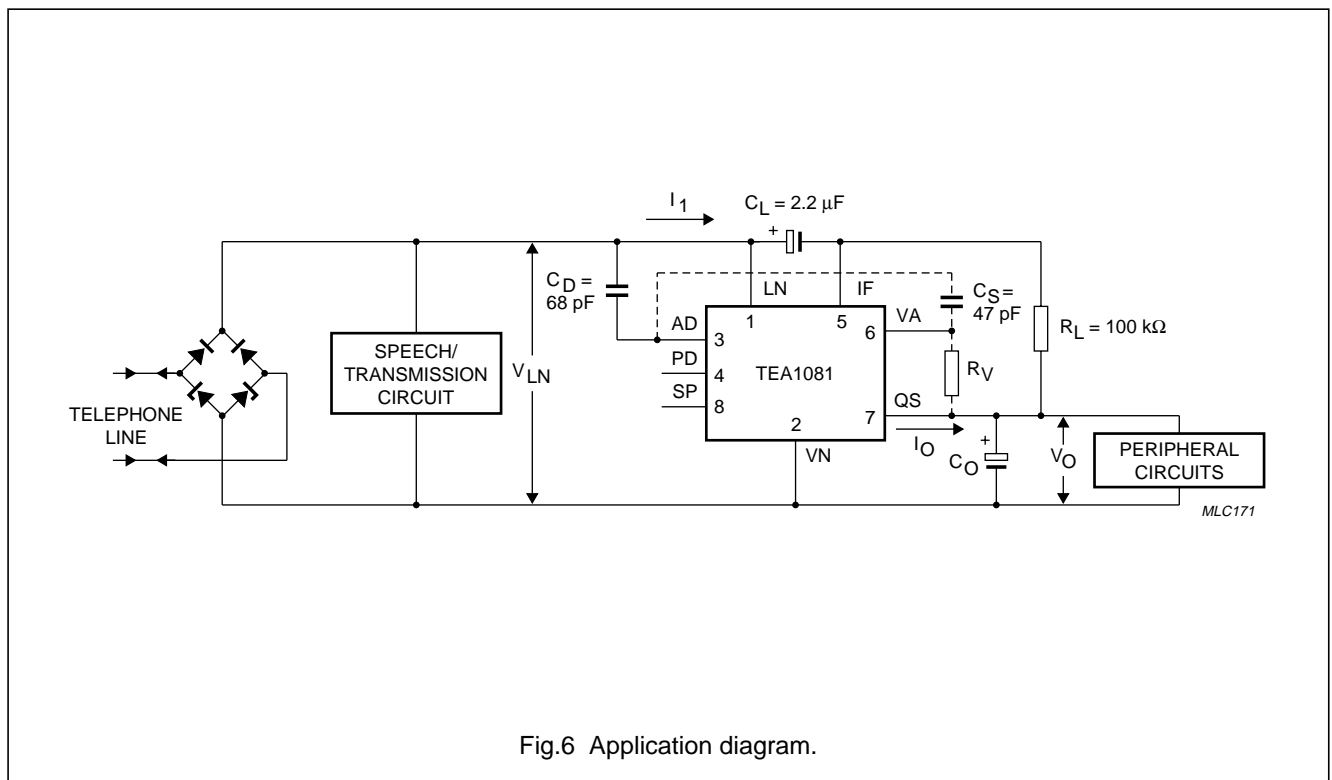
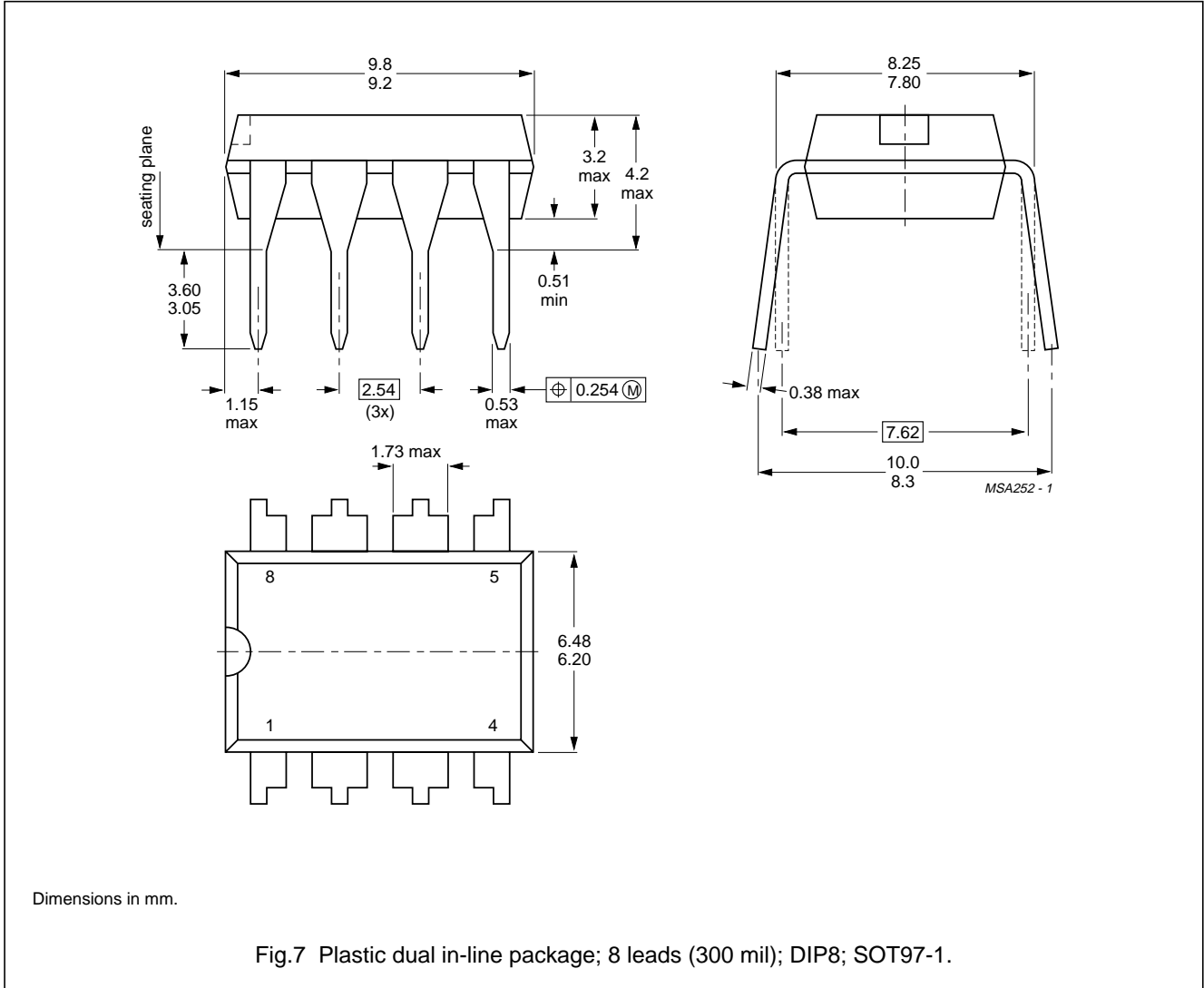


Fig.6 Application diagram.

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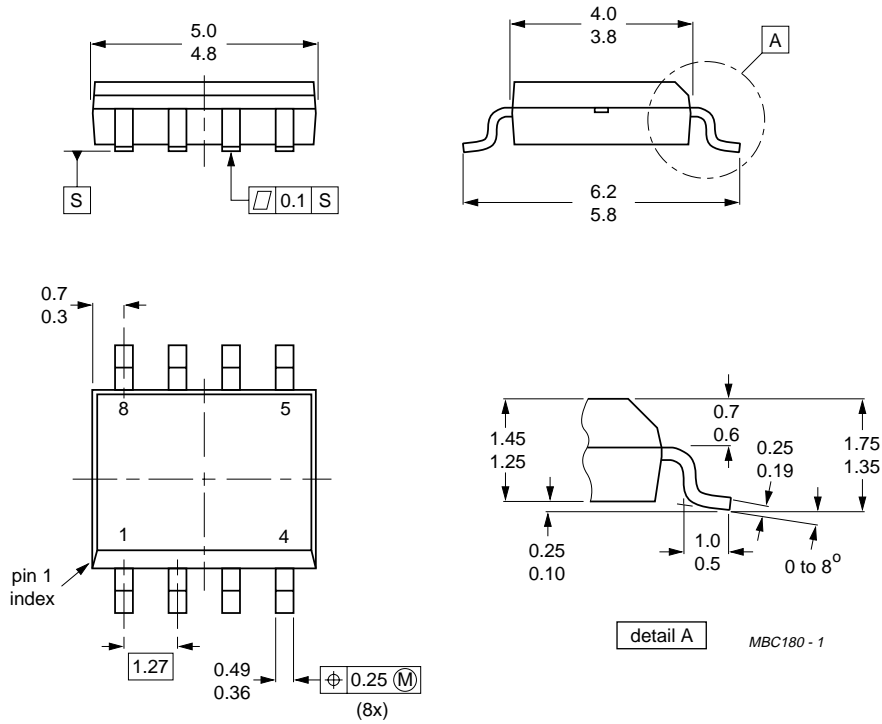
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PACKAGE OUTLINES



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Dimensions in mm.

Fig.8 Plastic small outline package; 8 leads; body width 3.9 mm (SO8; SOT96-1).

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SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low-voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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