INTEGRATED CIRCUITS



Preliminary specification File under Integrated Circuits, IC03A March 1992



### TEA1085; TEA1085A

### FEATURES

- Internal supply
  - optimum current split-up
  - low constant current (adjustable) in transmission IC
    nearly all line current available for listening-in
  - adjustable supply voltage
- Loudspeaker amplifier

dynamic limiter providing low distortion and the highest possible output power SE or BTL drive for loudspeaker volume control by potentiometer and/or logic inputs (e.g. microcontroller drive) fixed gain of 35 dB

Larsen level limiter

low sensitivity for own speech due to 3rd-order filter and attack delay adjustable voltage thresholds

- Power down input
- MUTE input
  - TEA1085/TEA1085A
  - clickfree switching between listening-in mode and standby mode

#### TEA1085

- toggle function
- start-up in standby condition
- TEA1085A
- logic level input

### **ORDERING INFORMATION**

#### PACKAGE EXTENDED TYPE NUMBER PINS **PIN POSITION** MATERIAL CODE TEA1085/TEA1085A 24 DIL SOT101B<sup>(1)</sup> plastic TEA1085T/TEA1085AT SO24 SOT137A<sup>(2)</sup> 24 plastic

#### Notes

- 1. SOT101-1; 1998 Jun 18.
- 2. SOT137-1; 1998 Jun 18.

### **GENERAL DESCRIPTION**

The TEA1085 and TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The circuits incorporate a supply circuit, loudspeaker amplifier dynamic limiter, MUTE circuit, power-down facility and logic inputs for gain setting. The devices also incorporate a Larsen Level Limiter to reduce howling effects.

The ICs are intended for use in conjunction with a transmission circuit of the TEA1060 family.

## TEA1085; TEA1085A

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>SUP</sub>	input current range		4	-	120	mA
V <sub>BB</sub>	stabilized supply voltage		-	3.6	-	V
I <sub>SUP</sub>	current consumption	PD = HIGH	-	55	-	μA
Gv	voltage gain loudspeaker amplifier					
		SE	-	35	-	dB
		BTL	-	41	-	dB
$\Delta G_v$	maximum gain reduction with logic inputs (3 steps)		-	18	-	dB
I <sub>SUP</sub>	minimum input current					
		$P_{OUT} = 20 \text{ mW typ.}$ into 50 Ω SE	-	15	17	mA
		$P_{OUT}$ = 40 mW typ. into 50 Ω BTL	-	-	32	mA
t <sub>ad(RMS)</sub>	Larsen limiter attack delay time $V_{DTI}$ jumps from 0 to $\geq$ 100 mV (RMS value)		100	-	200	ms
V <sub>DTI(RMS)</sub>	Larsen limiter threshold level	Larsen mode	-	7	-	mV
Gv	Larsen limiter preamplifier gain setting range		30	_	52	dB
T <sub>amb</sub>	operating ambient temperature range		-25	-	+75	°C



### Preliminary specification

# Listening-in circuit for line-powered telephone sets

### TEA1085; TEA1085A

### **PIN CONFIGURATION**

SYMBOL	PIN	DESCRIPTION				
V <sub>SS</sub>	1	negative supply	1			
SUP	2	positive supply	1			
SDC	3	supply amplifier decoupling	1			
SREF	4	supply reference input	]			
LSI1	5	loudspeaker amplifier input 1	]			-
LSI2	6	loudspeaker amplifier input 2	]	V <sub>SS</sub> 1	U	24
GSC2	7	logic input 2 for gain select	]	SUP 2		23
GSC1	8	logic input 1 for gain select	]			22
LAI–	9	Larsen limiter preamplifier inverting input		SREF 4		21
LAI+	10	Larsen limiter preamplifier non-inverting input		LSI1 5 LSI2 6	TEA1085	20 19
QLA	11	Larsen limiter preamplifier output	]		TEA1085A	18
LLC	12	Larsen limiter capacitor	]			10
THL2	13	Larsen limiter residual threshold level				
THL1	14	Larsen limiter attack delay threshold level		LAI- 9 LAI+ 10		16 15
DTI	15	Larsen limiter detector input	1	QLA 11		14
DCA	16	Larsen limiter detector current adjustment		LLC 12		13
SIC	17	Larsen limiter current stabilizer	1		MLA41	5
VA	18	V <sub>BB</sub> voltage adjustment	]			
PD	19	power-down input	]			
MUTE	20	MUTE input				
QLS1	21	loudspeaker amplifier output 1				
QLS2	22	loudspeaker amplifier output 2				
DLC	23	dynamic limiter capacitor		Fig.2	Pin configu	ratio
V <sub>BB</sub>	24	stabilized supply decoupling				

### FUNCTIONAL DESCRIPTION

Figure 1 illustrates a block diagram of the TEA1085/TEA1085A with external components and connections to the transmission IC.

The TEA1085/TEA1085A are bipolar ICs which have been designed for use in line-powered telephone sets and provide a listening-in facility for the received line signal via a loudspeaker. Nearly all the line current can be used for powering the loudspeaker.

The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and, a double push-pull output stage to drive the loudspeaker in the BTL (bridge tied load) or SE (single ended) configuration. The gain of the preamplifier is controlled by a dynamic limiter which prevents high distortion of the loudspeaker signal. This is achieved by preventing clipping of the loudspeaker signal, with respect to the supply voltage, and at too low supply current. Two logic inputs can be used to reduce the gain in 3 steps. Because of acoustic feedback from the loudspeaker to the microphone, howling signals (Larsen effect) can occur on the telephone line and in the loudspeaker. When the Larsen signal exceeds a voltage and time duration threshold the Larsen level limiter (LLL) will reduce the

### TEA1085; TEA1085A

Larsen signal to a low level within a short period of time by reducing the gain of the receiving preamplifier. This is achieved by using the microphone signal as an input signal which is processed in the LLL via a preamplifier and 3rd-order filter.

The MUTE input can be used to enable or disable the loudspeaker amplifier.

The MUTE function of the TEA1085 has a toggle input to permit the use of a simple push-button switch.

The MUTE function of the TEA1085A has a logic input to operate with a microcontroller.

By activating the power-down input the current consumption of the circuit will be reduced, this enables pulse dialling or flash (register recall).

An internal start circuit ensures normal start-up of the transmission IC and start-up of the listening-in IC in the standby mode.

The TEA1085/TEA1085A are intended for use in conjunction with a member of the TEA1060 family and should be connected between LINE and SLPE of the transmission IC. The transmission characteristics (impedance, gain settings, for example) are not affected. The interconnection between the two ICs is illustrated in Fig.3.



### TEA1085; TEA1085A

### Supply; SUP, SREF, V<sub>BB</sub>, V<sub>SS</sub> and VA

The line current is divided into  $I_{TR}$  for the TEA1060 and  $I_{SUP}$  for the TEA1085/TEA1085A. The supply arrangement is illustrated in Fig.4.



#### Where:

V <sub>int</sub>	is an internal temperature compensated
	reference voltage with a typical value of
	315 mV between SUP and SREF

- R20 is a resistor between SUP and SREF
- $I_{CC}$  is the internal current consumption of the TEA106X ( $\approx$  1 mA)

A practical value for R20 is 150  $\Omega$ . This value of resistance produces a value for I<sub>TR</sub> = 2 mA and I<sub>SUP</sub> = I<sub>line</sub> – 3 mA.

The TEA1085/TEA1085A stabilizes its own supply voltage at V<sub>BB</sub>. Transistor TR1 provides the supplies for the internal circuits. TR2 is used to minimize the signal distortion on the line by momentarily diverting the input current to V<sub>SS</sub> whenever the instantaneous value of the voltage V<sub>SUP</sub> drops below the supply voltage V<sub>BB</sub>. V<sub>BB</sub> is fixed to a typical value of 3.6 V but can be increased by means of an external resistor (R38) connected between

VA and V<sub>SS</sub> or decreased by connecting this resistor between VA and V<sub>BB</sub>. The minimum level on V<sub>BB</sub> is restricted to 3.0 V; the level of the V<sub>BB</sub> limiter is also affected (see application report for further information). The supply at V<sub>BB</sub> is decoupled by a 470  $\mu$ F capacitor.

The DC voltage ( $V_{SUP} - V_{SS}$ ) is determined by the transmission IC ( $V_{LN-SLPE}$ ); thus:  $V_{SUP} - V_{SS} = V_{LN-SLPE} + V_{int}$ . The minimum DC voltage that can be applied to this input is  $V_{BB(max)} + 0.4$  V.

Where:  $V_{BB(max)}$  is the worst case supply voltage (this depends on the setting of R38, which is connected between VA and  $V_{SS}$ ).

The internal current consumption of the TEA1085/TEA1085A (I<sub>SUP0</sub>) is typically 4.2 mA (where V<sub>SUP</sub> - V<sub>SS</sub> = 4.5 V, MUTE off). Thus the current available for powering the loudspeaker is I<sub>SUP</sub> - I<sub>SUP0</sub>. The current I<sub>SUP0</sub> consists of a bias current of  $\approx$  0.4 mA for the circuitry connected to SUP and current I<sub>BB0</sub> of  $\approx$  3.8 mA which is used for the circuitry connected to V<sub>BB</sub> (see Fig.4).



#### Supply amplifier stability (SDC) pin 3

To ensure stability of the TEA1085/TEA1085A, in combination with a transmission IC of the TEA1060 family, a 47 pF capacitor connected between SDC and SUP and a 150  $\mu$ H coil connected between SUP and the positive line terminal (Fig.16) is required.

## Loudspeaker amplifier (LSI1/LSI2 and QLS1/QLS2) pins 5/6, 21/22

The TEA1085/TEA1085A have symmetrical inputs at LSI1 and LSI2. The input signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (see Fig.3). The amount of attenuation must be chosen in accordance with the receive gain of the transmission IC (which depends on the sensitivity of the earpiece transducer). The maximum input signal level is 450 mV(RMS) at  $T_{amb} = +25$  °C.

The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimized for use with a 50  $\Omega$  loudspeaker (e.g. Philips type AD2071).

The gain of the amplifier is fixed to  $\approx$  35 dB for the SE drive and  $\approx$  41 dB for the BTL drive (when the inputs for logic control are left open-circuit or are connected to V<sub>SS</sub>). The volume control can be obtained by using a potentiometer at the input and/or by the logic control function.

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### Logic gain control (GSC1 and GSC2) pins 7 and 8

The logic inputs GSC1 and GSC2 can be used to reduce the gain of the loudspeaker amplifier by means of the logic gain control function in 3 steps of 6 dB.

GSC2	GSC1	gain (dB)	gain reduction (dB)
0	0	35	0
0	1	28.7	6.3
1	0	22.2	12.2
1	1	17	18

### Where:

 $\begin{array}{l} 0 = \text{connection to } V_{SS} \text{ or left open-circuit} \\ 1 = \text{applying a voltage} \geq V_{SS} + 1.5 \text{ V} \end{array}$ 

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### Dynamic limiter (DLC) pin 23

To prevent distortion of the signal at the loudspeaker outputs the gain of the amplifier is reduced rapidly when:

- the peaks of the signal at the loudspeaker outputs exceed an internally determined threshold (voltage limiter)
- the DC current into SUP is insufficient (current limiter)
- the voltage at V<sub>BB</sub> decreases below an internally determined threshold, typically 2.9 V (V<sub>BB</sub> limiter)

The time in which the gain reduction is effected is the 'attack time'; this is very short in the first and third instance and relatively long in the second instance. The circuit will remain in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain will then return to a nominal level after a time determined by the capacitor connected to DLC (release time).

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#### MUTE input (MUTE) pin 20; TEA1085A

This MUTE is provided with a logic input to operate with a microcontroller for instance.

The loudspeaker amplifier is disabled when the MUTE input is LOW (connected to  $V_{SS}$  or open input). A HIGH level at the MUTE input enables the amplifier in the listening-in mode.

### MUTE input (MUTE) pin 20; TEA1085

The MUTE function is provided with a toggle input and is designed to switch between the standby condition and the listening-in condition on the rising edge of the input MUTE signal (see Fig.6).

In the basic application the MUTE input must be LOW (connected to V<sub>SS</sub>). A simple push-button can be used to operate the MUTE toggle (see Fig.7). Debouncing can be realized by means of a small capacitor connected between MUTE and V<sub>SS</sub>.

An internal start circuit ensures that the circuit always starts up in the standby condition.





#### Power down input (PD) pin 19

During pulse dialling or register recall (timed loop break) the telephone line is interrupted, thereby breaking the supply to the transmission and listening-in circuits. The capacitor connected to V<sub>BB</sub> provides the supply for the listening-in circuit during the supply breaks. By making the PD input HIGH during the loop break the requirement on the capacitor is eased and, consequently, the internal (standby) current consumption I<sub>BBO</sub> (Fig.4) at V<sub>BB</sub> is reduced from 3.8 mA to 400  $\mu$ A typical. So that the transmission circuit is not affected transistors TR1 and TR2 are inhibited and the bias current is reduced from  $\approx 0.4$  mA to  $\approx 55 \,\mu$ A with V<sub>SUP</sub> = 4.5 V in the following equation:

 $I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2V_d) / Ra$ 

(where  $4.2 \text{ V} < \text{V}_{\text{SUP}} < \text{V}_{\text{BB}} + 3 \text{ V}$ )

 $2V_d$  = the voltage drop across 2 internal diodes ( $\approx$  1.3 V) Ra = an internal resistor of typical 60 k $\Omega$ 

### Larsen limiter current stabilizer (SIC) pin 17

A current reference is set by resistor R36 between SIC and  $V_{SS}$ . The preferred value is 120 k $\Omega$ . The internal reference current is given by the following equation:

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 $I_{SIC}$  = 1.25 / R36; when R36 = 120 k\Omega,  $I_{SIC}$  = 10.5  $\mu A$ 

Changing the value of R36 will affect the timing of the Larsen level limiter system.

## Larsen limiter preamplifier (LAI1/LAI2 and QLA) pins 9/10 and 11

This circuit amplifies the microphone signal to a level suitable for the Larsen limiter detector. The gain is set by external components (see Fig.8).

Normally the gain is set to the same level as the microphone amplifier of the transmission circuit, this ensures that the output signal level at output QLA is equal to the line signal level.

The gain between QLA and the microphone input is given by the following equation (the high-pass filter is not taken into account):

 $A_{pre}$  =  $V_{QLA}$  /  $V_{M}$  = R29 / R26; in the basic application R25 = R26 = 10  $k\Omega$ 

The gain can be adjusted between 30 dB (R29 = 316 k $\Omega$ ) and 52 dB (R29 = 4 M $\Omega$ ). The impedance result of R28 and R27 in parallel must be equal to R29 (e.g. R27 = R28 = 2 × R29).



#### Larsen limiter detector (DTI and DCA) pins 15 and 16

The QLA output signal is AC coupled to the detector input DTI. DTI is biased by potential divider R30 and R31. The voltage applied to DTI of the Larsen level limiter is converted into a current for further processing in this circuit. Current adjustment is achieved using the network connected between DCA and  $V_{BB}$  (see Fig.8).

The equation for DC current is:

$$I_{DCA} = \frac{R30}{R30 + R31} \times V_{BB} \times \frac{1}{R32 + R33}$$

The equation for AC current is:

$$i_{DCA} = \frac{V_{DTI}}{R33}$$
 for f >  $\frac{1}{2}\pi$  R33 C25

In the basic application:

R30 = 100 kΩ, R31 = 220 kΩ, R33 = 500 Ω, R32 = 100 kΩ and C25 = 330 nF

This results in  $I_{DCA} = 11 \ \mu A$  and the equation:

$$\frac{I_{DCA}}{V_{DTI}} = 2 (mA/V)$$

#### **High-pass filter**

A third order high-pass filter is created between the microphone input voltage and the current flowing into DCA. The cut-off frequencies (see Fig.9) of the three sections are:

f1 = 
$$\frac{1}{2\pi R_{eg}C24}$$
 where  $R_{eq} = \frac{R30 \times R31}{R30 + R31}$   
f2 =  $\frac{1}{2\pi R33C24}$ 

$$f3 = \frac{1}{2\pi R^2 6 C^2 3} = 1/(2\pi R^2 5 C^2 2)$$

Where: R25 = R26 and C22 = C23

The filter reduces the sensitivity of the system to own speech.

Normal speech is in the frequency range 300 Hz to 3400 Hz, however, the Larsen signal normally occurs at a frequency > 3 kHz.

With the component values as used in the basic application (see Fig.16); f1 = 500 Hz, f2 = 1 kHz and f3 = 3 kHz



Where: 
$$g = \frac{i_{DCA}}{V_m}$$
  $g_o = \frac{A_{pre}}{R33}$ 

#### Larsen limiter capacitor (LLC) pin 12

A 1  $\mu$ F capacitor (C26) is connected externally between V<sub>SS</sub> and LLC to determine the attack and release timing of the Larsen level limiter in the listen-in and Larsen mode. The timing is also dependent on the value of the resistor connected between SIC and V<sub>SS</sub>.

## Larsen level limiter threshold (THL1 and THL2) pins 13 and 14

When the signal at DTI exceeds the first threshold level the capacitor connected to LLC will start to discharge. The first threshold level is determined by the value of the resistor, R35, connected to THL1 and  $V_{SS}$ . The amount of discharge of C26 depends on how much the level of the signal at DTI exceeds the first threshold level (for normal speech the discharge is small).

The Larsen effect is generally defined as a signal level of  $\geq 100 \text{ mV}(\text{RMS})$ , on line, for a period of more than 100 ms. The Larsen signal must be reduced to a low level within 200 ms. For Larsen signal levels (f > f3 in Fig.9) of  $\geq 100 \text{ mV}(\text{RMS})$  at DTI and, with the component values of Fig.16, the system will switch from the listen-in mode to the Larsen mode in a time period of 100 ms to 200 ms; consequently, the initial Larsen effect will last only for a short period of time.

This reaction time is the 'attack delay time' and ensures minimum sensitivity of the system for own speech.

The first threshold level at DTI is determined by the equation:

$$V_{DTI1} = \left(\frac{1.25}{R25} - \frac{I_{DCA}}{2}\right) \times 2 \times R33$$
 (if f > f3 in Fig.9)

Where: I<sub>DCA</sub> = the DC current into DCA

With the component values given in Fig.16,  $I_{DCA} = 11 \ \mu A$  thus  $V_{DTI1} = 18.8 \ mV$ .

#### Listen-in mode

During normal speech the discharge of the capacitor connected to LLC is not sufficient to reach the threshold level whereby the system switches to the Larsen mode. This is because normal speech is not continuous, the discharge of C26 is slow (attack delay) and the charge is fast.

The slope of  $V_{LLC}$  during charge is given in the equation:

$$S_{1i} = \frac{\Delta V_{LLC}}{\Delta_{\tau}} = \frac{1.25}{C26 \times R36} \quad (V/s)$$

With C26 = 1  $\mu$ F and R36 = 120 k $\Omega$  this results in S<sub>1i</sub> = 10 V/s.

Discharge of the capacitor at LLC occurs when the signal at DTI exceeds  $V_{DTI1}$ , thus for a continuous signal at DTI the attack delay time  $t_{ad}$  (see Fig.10) is determined by the equation:

 $t_{ad} = \frac{C26 \times R36}{2 \times (3 \times k - 1)}$ 

Where  $k = t_1 / T$ 

The duty cycle is determined by the time in which the first threshold level ( $V_{DTI1}$ ) is exceeded by the signal level at DTI (see Fig.11) thus for large signals; k  $\leq$  0.5.

With the component values given in Fig.16;  $k \ge 0.457$  for signals  $\ge 100 \text{ mV}(\text{RMS})$ .

$$\label{eq:consequently 120 ms} \begin{split} & \text{Consequently 120 ms} \leq t_{ad} \leq 160 \text{ ms, for} \\ & \text{V}_{\text{DTI}} \geq 100 \text{ mV}(\text{RMS}) \end{split}$$

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#### Larsen mode

After the 'attack delay time' the circuit switches from the listen-in mode to the Larsen mode. The gain of the loudspeaker amplifier is reduced quickly to a value ( $t_{LAa}$  = Larsen attack time, see Fig.10) whereby the residual Larsen signal is determined by a second threshold level. This level can be set by resistor R34 connected between THL2 and V<sub>SS</sub>. The second threshold level must always be selected at a lower level than the first threshold level thus R34 > R35.

The time taken to effect gain reduction is very short. In the Larsen mode the circuit acts as a dynamic limiter with peak detector and regulates the gain so that the signal level at DTI is determined by the second threshold level  $V_{\text{DTI2}}$ . The second threshold level at DTI is determined by the equation:

$$V_{DTI2} = \left(\frac{1.25}{R34} - \frac{I_{DCA}}{2}\right) \times 2 \times R33$$
 (if f > f3 in Fig.9)

Where:  $I_{DCA}$  = the DC current into DCA

With the component values given in Fig.16,  $V_{DTI2} = 6.9$  mV.

The charge current in the Larsen mode is reduced to half the charge current in the listen-in mode.

The slope of  $V_{LLC}$  during charge (see Fig.10) is given in the equation:

$$S_{la} = \frac{\Delta V_{LLC}}{\Delta_{\tau}} = \frac{1.25}{2 \times C26 \times R34} (V/s)$$

Where: C26 = 1  $\mu$ F and R36 = 100 k $\Omega$ , S<sub>la</sub> = 5 V/s

When the Larsen effect stops (total open-loop gain < 1) the gain of the loudspeaker amplifier will return to its normal value in a time period known as the 'Larsen release time' ( $t_{LAr}$ ). This time period is determined by capacitor C26 connected to LLC and resistor R36 connected to SIC.

Where: C26 = 1  $\mu$ F and R36 = 120 k $\Omega$ , t<sub>LAr</sub> = 250 ms

In practice the choice of the threshold levels (determined by R35 and R34) depends on the sensitivity of the microphone and loudspeaker, the send and receive gains, sidetone suppression and the acoustical properties which are determined by the cabinet of the telephone set.





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### LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>SUP</sub>	positive supply voltage				
	continuous		_	12	V
	during switch-on or line interruption		-	13.2	V
	repetitive supply voltage from 1 ms to 5 s	with 12 $\Omega$ current	-	28	V
		limiting resistor in series with supply			
V <sub>SREF</sub>	supply reference voltage		V <sub>SS</sub> – 0.5	V <sub>SUP</sub> + 0.5	V
Vn	voltage on all other pins		$V_{SS} - 0.5$	V <sub>BB</sub> + 0.5	V
I <sub>SUP</sub>	supply current				
	TEA1085/TEA1085A	see Fig.12	-	120	mA
	TEA1085T/TEA1085AT	see Fig.13	-	120	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 75 °C; T <sub>j</sub> = 125 °C			
	TEA1085/TEA1085A		_	1	w
	TEA1085T/TEA1085AT		_	666	mW
T <sub>amb</sub>	operating ambient temperature range		-25	+75	°C
T <sub>stg</sub>	storage temperature range		-40	+125	°C
Tj	junction temperature		_	+125	°C

### THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
R <sub>th j-a</sub>	from junction to ambient in free air		
	TEA1085/TEA1085A		50 K/W
	TEA1085T/TEA1085AT	note 1	75 K/W

### Note

1. Device mounted on a glass epoxy board  $40.1 \times 19.1 \times 1.5$  mm.





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### CHARACTERISTICS

 $V_{SREF} = 4.2 \text{ V}; V_{SS} = 0 \text{ V}; I_{SUP} = 15 \text{ mA}; V_{SUP} = 0 \text{ V}(RMS); f = 800 \text{ Hz}; T_{amb} = 25 \text{ °C}; PD = LOW; MUTE (TEA1085) = OFF (listening-in mode); MUTE (TEA1085A) = HIGH (listening-in mode); GSC1 = GSC2 = LOW; 50 \Omega loudspeaker; no R38; test circuit Fig.14; unless otherwise specified$ 

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies			•		•	
V <sub>SUP</sub>	minimum DC input voltage		-	V <sub>BB</sub> + 0.7	-	V
V <sub>SUP-SREF</sub>	internal reference voltage		275	315	355	mV
V <sub>BB</sub>	stabilized supply voltage	no R38; I <sub>SUP</sub> = 15 mA	3.4	3.6	3.8	V
$\Delta V_{BB}$	variation from I <sub>SUP</sub> = 15 to 120 mA		_	10	-	mV
		$\label{eq:result} \begin{array}{l} \text{R38} = 39.2 \text{ k}\Omega \text{ between} \\ \text{pins } \text{V}_{\text{SS}} \text{ and } \text{VA}; \\ \text{V}_{\text{SREF}} = 5.2 \text{ V}; \\ \text{I}_{\text{SUP}} = 15 \text{ mA} \end{array}$	4.2	4.45	4.7	V
$\Delta V_{BB} / \Delta T$	variation with temperature	no R38; I <sub>SUP</sub> = 15 mA	tbf	-0.2	tbf	V
I <sub>SUP</sub>	minimum operating current		_	4.2	5.5	mA
THD	distortion of AC signal on SUP	V <sub>SUP(RMS)</sub> = 1 V	_	0.3	_	%
V <sub>no(RMS)</sub>	noise between SUP and $V_{EE}$		_	-72	_	dBmp
	current consumption in power-down condition	PD = HIGH				
I <sub>SUP</sub>		V <sub>SUP</sub> = 4.5 V	-	55	75	μA
I <sub>BB</sub>		V <sub>BB</sub> = 3.6 V	-	400	550	μA
Loudspea	ker amplifier inputs LSI1 and L	-SI2				
Z <sub>i</sub>	input impedance					
		single ended	7.5	9.5	11.5	kΩ
		differential	15	19	23	kΩ
Gv	voltage gain with 50 $\Omega$ load	I <sub>SUP</sub> = 15 mA; V <sub>i</sub> = 1.8 mV(RMS)				
		single ended	34	35	36	dB
		BTL output	39.9	40.9	41.9	dB
$\Delta G_v$	variation with signal level	$\label{eq:supersolution} \begin{split} I_{SUP} &= 50 \text{ mA};\\ V_i &= 1.8 \text{ mV}(\text{RMS}) \text{ and}\\ 14 \text{ mV}(\text{RMS}) \end{split}$				
		single ended	-	+0.1	0.4	dB
		BTL output	-	+0.2	0.6	dB
$\Delta G_v$	variation with frequency referred to 1 kHz	f = 300 Hz and 3400 Hz; V <sub>i</sub> = 1.8 mV(RMS)				
		single ended	-	± 0.1	-	dB
		BTL output	-	± 0.1	-	dB
$\Delta G_v$	variation with temperature referred to 25 °C	$T_{amb} = -25 \text{ to } +75 ^{\circ}\text{C}$				
		single ended	-	± 0.4	-	dB
		BTL output	-	± 0.5	-	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Loudspea	ker outputs QLS1 and QLS2					
V <sub>o(p-p)</sub>	output voltage (peak-to-peak value)	V <sub>i</sub> = 22 mV(RMS)				
	single ended	I <sub>SUP</sub> = 9 mA; note 1	1.2	1.45	_	V
		I <sub>SUP</sub> = 17 mA; note 2	2.5	2.9	_	V
	bridge tied load	I <sub>SUP</sub> = 23.5 mA; note 2	2.5	2.9	_	V
		I <sub>SUP</sub> = 32 mA; note 3	3.5	4.0	_	V
THD	total harmonic distortion	V <sub>i</sub> = 22 mV(RMS)				
	single ended	I <sub>SUP</sub> = 9 mA	_	0.4	2	%
		I <sub>SUP</sub> = 17 mA	_	0.7	2	%
	bridge tied load	I <sub>SUP</sub> = 23.5 mA	_	0.4	2	%
V <sub>o(p-p)</sub>	output voltage (peak-to-peak value)	V <sub>i</sub> = 22 mV(RMS)				
	single ended	I <sub>SUP</sub> = 17 mA; V <sub>SUP</sub> – V <sub>EE</sub> = 1 V(RMS)	1.75	2.15	_	V
Dynamic I	imiter					
THD	total harmonic distortion	V <sub>i</sub> = 22 mV(RMS) +10 dB				
	single ended	I <sub>SUP</sub> = 9 mA	_	0.5	10	%
		I <sub>SUP</sub> = 17 mA	_	1.2	10	%
	bridge tied load	I <sub>SUP</sub> = 23.5 mA	-	0.6	10	%
t <sub>att</sub>	dynamic behaviour of limiter attack time; V <sub>i</sub> jumps from 10 mV(RMS) to 65 mV(RMS)	single ended load				
	voltage limiter	I <sub>SUP</sub> = 17 mA	_	2	5	ms
	current limiter	I <sub>SUP</sub> = 12 mA	_	500	tbf	ms
	V <sub>BB</sub> limiter	I <sub>SUP</sub> = 9 mA	-	10	-	ms
t <sub>rel</sub>	release time; V <sub>i</sub> jumps from 65 mV(RMS) to 10 mV(RMS)	I <sub>SUP</sub> = 17 mA	tbf	75	tbf	ms
V <sub>BBO</sub>	threshold V <sub>BB</sub> limiter below which gain reduction starts	I <sub>SUP</sub> = 9 mA	tbf	2.95	tbf	V
V <sub>no(RMS)</sub>	noise output voltage	1 kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)				
	single ended		-	170	-	μV
	bridge tied load		-	350	-	μV
Logic gain	control					
$\Delta G_v$	reduction of voltage gain	V <sub>i</sub> = 1.8 mV(RMS)				
	GSC2 = 0, GSC1 = 1		5.8	6.3	6.8	dB
	GSC2 = 1, GSC1 = 0		11.7	12.2	12.7	dB
	GSC2 = 1, GSC1 = 1		17	18	19	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Larsen lim	iter preamplifier		•			
	operational amplifier					
G <sub>v0</sub>	open-loop gain		_	92	_	dB
f <sub>p1</sub>	1st pole		-	120	-	Hz
f <sub>p2</sub>	2nd pole		-	3.3	-	MHz
G <sub>B</sub>	unity gain bandwidth		-	4	_	MHz
Gv	voltage gain	f = 3 kHz; R26 = 10 kΩ; R29 = 4 MΩ	51	52	53	dB
Gv	gain adjustment range		30	-	52	dB
Larsen lim	iter detector					
	voltage to current convertor					
V <sub>DCA</sub> -V <sub>DTI</sub>	DC offset voltage	$V_{BB} - V_{DTI} = 1 V$	-25	1	+25	mV
Gv	voltage gain from DTI to DCA	V <sub>DTI</sub> = 100 mV(RMS); f = 3 kHz	tbf	-0.8	tbf	dB
V <sub>THL1</sub>	DC voltage at THL1	R35 = 51 kΩ	1.8	1.25	1.33	V
V <sub>THL2</sub>	DC voltage at THL2	R34 = 100 kΩ	1.8	1.25	1.33	V
	dynamic behaviour with a burst at DTI	f = 3 kHz; see Fig.15				
t <sub>LIr</sub>	listen-in release time	see Fig.15(a)	tbf	40	tbf	ms
t <sub>ad</sub>	attack delay time	see Fig.15(b)				
	V <sub>DTI</sub> jumps from 0 to 100 mV (RMS value)		-	160	200	ms
	V <sub>DTI</sub> jumps from 0 to 1 V (RMS value)		100	120	-	ms
t <sub>LAa</sub>	Larsen attack time	see Fig.15(b); V <sub>DTI</sub> = 100 mV(RMS)	-	20	tbf	ms
t <sub>LAr</sub>	Larsen release time	see Fig.15(b)				
	V <sub>DTI</sub> jumps from 100 mV to 0 mV (RMS value)		tbf	250	tbf	ms
V <sub>LLC</sub>	DC voltage at LLC	V <sub>DTI</sub> = 0 V	1.75	1.9	2.0	V
$-\Delta V_{LLC}$	reduction of V <sub>LLC</sub> to attack Larsen mode		0.59	0.63	0.68	V
$\Delta G_v$	gain reduction	$V_{LLC} = 0.7 V$	60	tbf	tbf	dB

### TEA1085; TEA1085A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT	
MUTE inp	MUTE input; TEA1085						
	(toggle function, positive edge triggered set-reset flip-flop)						
V <sub>IL</sub>	LOW level input voltage		0	-	0.3	V	
V <sub>IH</sub>	HIGH level input voltage		1.5	-	$V_{BB} + 0.4$	V	
I <sub>MUTE</sub>	input current	MUTE = LOW	-	-22	-28	μA	
t <sub>W</sub>	minimum input pulse width		—	50	_	μs	
P <sub>R</sub>	minimum pulse repetition time		_	2	_	ms	
V <sub>BB(MUTE)</sub>	supply voltage below which MUTE toggle is reset		tbf	2	tbf	V	
$\Delta G_v$	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = ON	60	100	-	dB	
MUTE inp	ut; TEA1085A		·	·			
V <sub>IL</sub>	LOW level input voltage		0	-	0.3	V	
VIH	HIGH level input voltage		1.5	-	V <sub>BB</sub> + 0.4	V	
I <sub>MUTE</sub>	input current	MUTE = HIGH	_	10	20	μA	
$\Delta G_v$	reduction of gain from LSI1, LSI2 to QLS1, QLS2	MUTE = HIGH	60	100	-	dB	
Power dov	vn input			•		•	
V <sub>IL</sub>	LOW level input voltage		0	-	0.3	V	
V <sub>IH</sub>	HIGH level input voltage		1.5	-	V <sub>BB</sub> + 0.4	V	
I <sub>PD</sub>	input current	PD = HIGH	-	2.3	2.8	μA	
Logic inpu	its GSC1 and GSC2			·			
V <sub>IL</sub>	LOW level input voltage		0	-	0.3	V	
VIH	HIGH level input voltage		1.5	-	V <sub>BB</sub> + 0.4	V	
I <sub>GSC</sub>	input current	GSC = HIGH	-	6	8	μA	

Notes

1. Typical output power is 5 mW into 50  $\Omega$ 

2. Typical output power is 20 mW into 50  $\Omega$ 

3. Typical output power is 40 mW into 50  $\Omega$ 



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COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R1		620	Ω
R5		3.6	kΩ
R9		20	Ω
R20		150	Ω
R25		10	kΩ
R26		10	kΩ
R27		8	MΩ
R28		8	MΩ
R29		4	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
Capacitor			
C1		100	μF
C3		4.7	μF
C20		470	μF
C21		68	pF
C22		2.2	μF
C23		2.2	μF
C24		100	nF
C25		330	nF
C26		1	μF
C27		220	μF
C28		330	nF
C31	TEA1085 only	10	nF

 Table 2
 Component values in test circuit Fig.14





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Preliminary specification

### TEA1085; TEA1085A

The basic application circuit of the TEA1085/TEA1085A is illustrated in Fig.16. Only the most important components of the TEA1060 part are shown, other components and their values are given in the TEA1060 Data sheet. The supply pin (V<sub>BB</sub>) of the TEA1085/TEA1085A can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc.). Further information will be published in the TEA1085 application report.

COMPONENT	CONDITION	VALUE	UNIT
Resistor			
R20		150	Ω
R24	note 1	1	kΩ
R25		10	kΩ
R26		10	kΩ
R27	note 1	3.3	MΩ
R28	note 1	3.3	MΩ
R29	note 1	1.65	MΩ
R30		100	kΩ
R31		220	kΩ
R32		100	kΩ
R33		500	Ω
R34		100	kΩ
R35		51	kΩ
R36		120	kΩ
RV20	note 1	1	kΩ
Capacitor	•	•	•
C11		4.7	nF
C20		470	μF
C21		47	pF
C22		4.7	nF
C23		4.7	nF
C24		4.7	nF
C25		330	nF
C26		1	μF
C27		47	μF
C28		330	nF
C29		220	nF
C30		220	nF
C31	TEA1085 only	10	nF
Coil		-	
L1		150	μH

Table 3	Component	values in	application	circuit	Fia.16
	oomponom	value o m	appnoation	onoun	1 19.10

#### Note

1. Value depends on the gain setting of the transmission circuit.

### PACKAGE OUTLINES

### DIP24: plastic dual in-line package; 24 leads (600 mil)



#### Note

inches

0.20

0.020

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

0.051

0.015

0.009

0.16

OUTLINE	REFERENCES		EUROPEAN			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT101-1	051G02	MO-015AD				<del>-92-11-17</del> 95-01-23

0.54

1.24

0.10

0.60

0.13

0.60

0.63

0.01

0.087

### TEA1085; TEA1085A

SOT101-1



### TEA1085; TEA1085A

#### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

### DIP

#### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45  $^{\circ}$ C.

#### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonallyopposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

### TEA1085; TEA1085A

### DEFINITIONS

Data sheet status			
Objective specification	This data sheet contains target or goal specifications for product development.		
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.		
Product specification	This data sheet contains final product specifications.		
Limiting values			
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.			
Application information			

Where application information is given, it is advisory and does not form part of the specification.

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

### TEA1085; TEA1085A

NOTES

### TEA1085; TEA1085A

NOTES

### TEA1085; TEA1085A

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Printed in The Netherlands

415102/00/02/pp32

Date of release: March 1992

Document order number: 9397 750 nnnnn

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