8-bit latched/registered/pass-thru Futurebus+ universal interface transceiver

FB2033

FEATURES

- 8-bit transceivers
- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL Open Collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce
- Glitch-free power up/power down operation
- Low I_{CC} current
- Tight output skew
- Supports live insertion

QUICK REFERENCE DATA

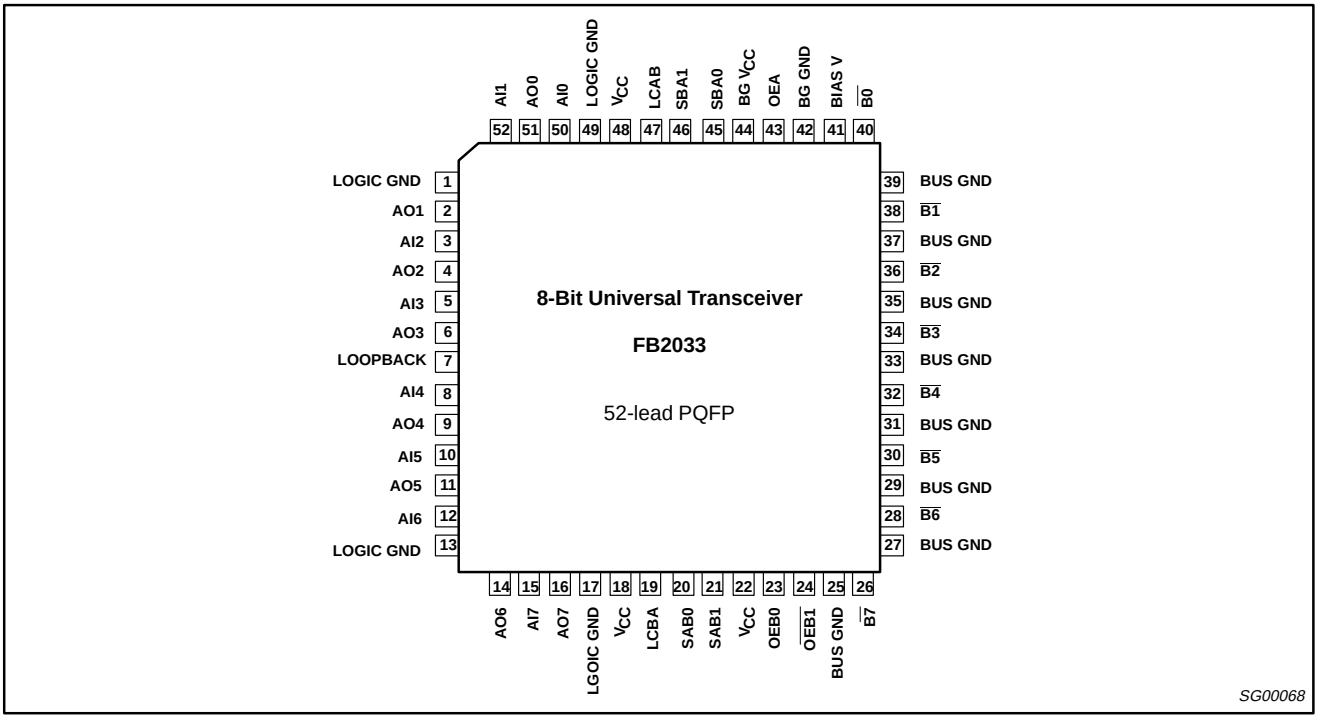
SYMBOL	PARAMETER		TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay AIn to $\overline{Bn}$		3.0 3.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{Bn}$ to AOn		4.3 4.1	ns
C_{OB}	Output capacitance ($\overline{B0}$ – $\overline{Bn}$ only)		6	pF
I_{OL}	Output current ($\overline{B0}$ – $\overline{Bn}$ only)		100	mA
I_{CC}	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	24	mA
		$\overline{Bn}$ to AOn (outputs Low)	45	
		$\overline{Bn}$ to AOn (outputs High)	22	

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_{amb} = 0°C to +70°C	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (QFP)	FB2033BB	SOT379-1

NOTE: Thermal mounting or forced air is recommended

PIN CONFIGURATION



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DESCRIPTION

The FB2033 is an 8-bit transceiver featuring a split input (AI) and output (AO) bus on the TTL-level side.

The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two pairs of mode select inputs (SBA0 and SBA1 for B-to-A, SAB0 and SAB1 for A-to-B). It can be configured as a buffer, a register, or a D-type latch.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the flip-flop mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-High latch enables. Regardless of the mode, data is inverted from input to output.

Data flow in the B-to-A direction, regardless of the logic element selected, is further controlled by the Loopback input. When the Loopback input is High the output of the selected A-to-B logic element (not inverted) becomes the B-to-A input.

The 3-State AO port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and $\overline{\text{OEB1}}$. Only when OEB0 is High and $\overline{\text{OEB1}}$ is Low is the output enabled. When either OEB0 is Low or $\overline{\text{OEB1}}$ is High, the B-port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the flip-flop and latched modes or can be retained while the associated outputs are in 3-State (AO port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port ensure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to “Backplane Transceiver Logic” (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The “V_{OH}” clamp reduces inductive ringing effects during a Low-to-High transition. The “V_{OH}” clamp is always active. The other clamp, the “trapped reflection” clamp, clamps out ringing below the BTL 0.5V V_{OL} level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to ensure glitch- free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while V_{CC} is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a V_{CC} pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a “hard” signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble- shoot.

As with any high power device thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
AI0 – AI7	50, 52, 3, 5, 8, 10, 12, 15	Input	Data inputs (TTL)
AO0 – AO7	51, 2, 4, 6, 9, 11, 14, 16	Output	3-State outputs (TTL)
$\overline{\text{B0}}$ – $\overline{\text{B7}}$	40, 38, 36, 34, 32, 30, 28, 26	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	23	Input	Enables the B outputs when High
$\overline{\text{OEB1}}$	24	Input	Enables the B outputs when Low
OEA	43	Input	Enables the AO outputs when High
BUS GND	39, 37, 35, 33, 31, 29, 27, 25	GND	Bus ground (0V)
LOGIC GND	1, 13, 17, 49	GND	Logic ground (0V)
V_{CC}	18, 22, 48	Power	Positive supply voltage
BIAS V	41	Power	Live insertion pre-bias pin
BG V_{CC}	44	Power	Band Gap threshold voltage reference
BG GND	42	GND	Band Gap threshold voltage reference ground
SABn	20, 21	Input	Mode select from AI to $\overline{\text{B}}$
SBAn	45, 46	Input	Mode select from $\overline{\text{B}}$ to AO
LCAB	47	Input	A-to-B clock/latch enable (transparent latch when High)
LCBA	19	Input	B-to-A clock/latch enable (transparent latch when High)
Loopback	7	Input	Enables loopback function when High (from AIn to AOn)

FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	AIn	$\overline{Bn}$*	OEB0	$\overline{OEB1}$	OEA	LCAB	LCBA	$SAB_{1\ 0}$	$SBA_{1\ 0}$	AOn	$\overline{Bn}$
AIn to $\overline{Bn}$ thru mode	L	—	H	L	L	X	X	LL	XX	Z	H**
	H	—	H	L	L	X	X	LL	XX	Z	L
AIn to $\overline{Bn}$ transparent latch	L	—	H	L	L	H	X	HX	XX	Z	H**
	H	—	H	L	L	H	X	HX	XX	Z	L
AIn to $\overline{Bn}$ latch and read	l	—	H	L	L	↓	X	HX	XX	Z	H**
	h	—	H	L	L	↓	X	HX	XX	Z	L
AIn to $\overline{Bn}$ register	L	—	H	L	L	↑	X	LH	XX	Z	H**
	H	—	H	L	L	↑	X	LH	XX	Z	L
$\overline{Bn}$ outputs latched and read (preconditioned latch)	X	—	H	L	L	L	X	HX	XX	Z	latched data
$\overline{Bn}$ to AOn thru mode	X	L	L	H	H	X	X	XX	LL	H	input
	X	H	L	H	H	X	X	XX	LL	L	input
$\overline{Bn}$ to AOn transparent latch	X	L	L	H	H	X	H	XX	HX	H	input
	X	H	L	H	H	X	H	XX	HX	L	input
$\overline{Bn}$ to AOn latch and read	X	l	L	H	H	X	↓	XX	HX	H	input
	X	h	L	H	H	X	↓	XX	HX	L	input
$\overline{Bn}$ to AOn register	X	L	L	H	H	X	↑	XX	LH	H	input
	X	H	L	H	H	X	↑	XX	LH	L	input
AOn outputs latched and read (preconditioned latch)	X	X	L	H	H	X	L	XX	HX	latched data	X
Disable $\overline{Bn}$ outputs	X	X	L	X	X	X	X	XX	XX	X	H**
	X	X	X	H	X	X	X	XX	XX	X	H**
Disable AOn outputs	X	X	X	X	L	X	X	XX	XX	Z	X

FUNCTION SELECT TABLE

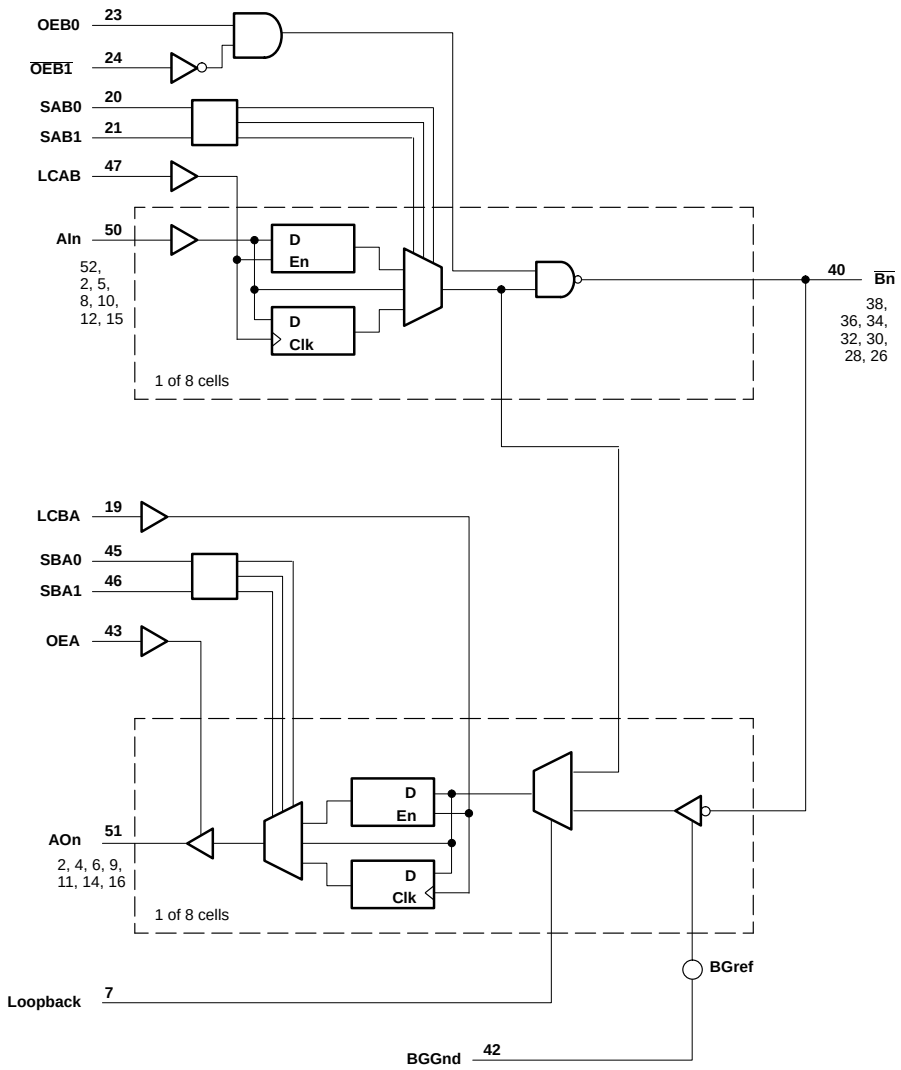
MODE SELECTED	SXX1	SXX0
Thru mode	L	L
Register mode	L	H
Latch mode	H	X

NOTES:

H = High voltage level
L = Low voltage level
h = High voltage level one set-up time prior to the High-to-Low LCXX transition
l = Low voltage level one set-up time prior to the High-to-Low LCXX transition
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
↑ = Low-to-High transition
↓ = High-to-Low transition
H** = Goes to level of pull-up voltage
$\overline{Bn}$* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

NOTE: In Loopback mode (Loopback = High), AIn inputs are routed to the AOn outputs. The $\overline{Bn}$ inputs are blocked out.

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage	All inputs except $\overline{B0}$ – $\overline{Bn}$	-1.2 to +7.0	V
		$\overline{B0}$ – $\overline{Bn}$	-1.2 to +3.5	
I_{IN}	Input current		-40 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	AO0 – AOn	48	mA
		$\overline{B0}$ – $\overline{Bn}$	200	
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except $\overline{B0}$ – $\overline{Bn}$	2.0			V
		$\overline{B0}$ – $\overline{Bn}$	1.62	1.55		
V_{IL}	Low-level input voltage	Except $\overline{B0}$ – $\overline{Bn}$			0.8	V
		$\overline{B0}$ – $\overline{Bn}$			1.47	
I_{IK}	Input clamp current	Except $\overline{B0}$ – $\overline{Bn}$			-40	mA
		$\overline{B0}$ – $\overline{Bn}$			-50	
I_{OH}	High-level output current	AO0 – AOn			-3	mA
I_{OL}	Low-level output current	AO0 – AOn			24	mA
		$\overline{B0}$ – $\overline{Bn}$			100	
I_{IA}	Off device input current	Except $\overline{B0}$ – $\overline{Bn}$, V_I = 0 to 5.5V, V_{CC} = 0V			100	µA
C_{OB}	Output capacitance of B port			6	7	pF
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				MIN	TYP[2]	MAX	
I_{OH}	High level output current	$\overline{B0}$ – $\overline{Bn}$	V_{CC} = MAX, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
I_{OFF}	Power-off output current	$\overline{B0}$ – $\overline{Bn}$	V_{CC} = 0.0V, V_{IL} = MAX, V_{IH} = MIN, V_{OH} = 1.9V			100	µA
V_{OH}	High-level output voltage	AO0 – AOn [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = -3mA	2.5	2.85		V
V_{OL}	Low-level output voltage	AO0 – AOn [4]	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 24mA			0.5	V
		$\overline{B0}$ – $\overline{Bn}$	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 100mA	.75	1.0	1.15	
			V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OL} = 4mA	0.5			
V_{IK}	Input clamp voltage	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MIN, I_I = I_{IK}			-0.5	V
		$\overline{B0}$ – $\overline{Bn}$	V_{CC} = MIN, I_I = I_{IK} [6]	0.3			
			V_{CC} = MIN, I_I = -18mA			-1.2	
I_I	Input current at maximum input voltage	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 0.0V or 5.5V			±50	µA
I_{IH}	High-level input current	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 2.7V, $\overline{Bn}$ = AIn = 0V			20	µA
		$\overline{B0}$ – $\overline{Bn}$	V_{CC} = MAX, V_I = 1.9V			100	
			V_{CC} = MAX, V_I = 3.5V [5]	100			mA
I_{IL}	Low-level input current	Except $\overline{B0}$–$\overline{Bn}$	V_{CC} = MAX, V_I = 0.5V			-20	µA
		$\overline{B0}$ – $\overline{Bn}$	V_{CC} = MAX, V_I = 0.75V			-100	
I_{OZH}	Off-state output current	AO0 – AOn	V_{CC} = MAX, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current	AO0 – AOn	V_{CC} = MAX, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current [3]	AO0 – AOn only	V_{CC} = MAX, V_O = 0.0V	-45		-150	mA
I_{CC}	Supply current (total)	AIn to $\overline{Bn}$	V_{CC} = MAX, outputs Low or High		24	50	mA
		$\overline{Bn}$ to AOn	V_{CC} = MAX, outputs Low		45	75	
		$\overline{Bn}$ to AOn	V_{CC} = MAX, outputs High		22	44	

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are V_{IH} = 1.8V and V_{IL} = 1.3V for the B side.
5. For B port input voltage between 3 and 5 volts I_{IH} will be greater than 100µA, but the parts will continue to function normally.
6. $\overline{B0}$ – $\overline{B7}$ clamps remain active for a minimum of 80ns following a High-to-Low transition.

LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{BIASV}	Bias pin voltage	V_{CC} = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V	4.5		5.5	V
I_{BIASV}	Bias pin DC current	V_{CC} = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			1	mA
		V_{CC} = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V			10	µA
$V_{\overline{Bn}}$	Bus voltage during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V	1.62		2.1	V
I_{LM}	Fall current during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V	1			µA
I_{HM}	Rise current during pre-bias	$\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V	-1			µA
$I_{\overline{Bn}PEAK}$	Peak bus current during insertion	V_{CC} = 0 to 5.25V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, t_r = 2ns			10	mA
$I_{OL}OFF$	Power up current	V_{CC} = 0 to 5.25V, OEB0 = 0.8V			100	µA
		V_{CC} = 0 to 2.2V, OEB0 = 0 to 5V			100	
t_{GR}	Input glitch rejection	V_{CC} = 5.0V	1.0	1.35		ns

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 4	100	150		100		MHz
t_{PLH} t_{PHL}	Propagation delay (thru mode) $\overline{Bn}$ to AOn	Waveform 1, 2	2.2 2.0	4.3 4.1	6.0 6.0	2.0 1.8	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) $\overline{Bn}$ to AOn	Waveform 1, 2	1.5 2.4	4.5 4.4	6.5 6.5	1.0 2.0	7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay LCBA to AOn	Waveform 1, 2	2.0 2.2	3.8 4.3	5.5 6.0	1.8 1.7	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay SBAn to AOn	Waveform 1, 2	1.4 1.4	2.9 3.1	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) AIn to AOn	Waveform 1, 2	2.0 2.0	3.8 3.9	6.0 6.0	2.8 2.3	7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay (Loopback mode) Loopback to AOn	Waveform 1, 2	1.2 1.2	3.4 3.2	5.0 5.5	1.0 1.0	6.0 6.5	ns
t_{PZH} t_{PZL}	Output enable time from High or Low OEA to AOn	Waveform 5, 6	1.0 2.6	3.1 4.0	5.1 5.5	1.0 2.4	5.5 5.8	ns
t_{PHZ} t_{PLZ}	Output disable time to High or Low OEA to AOn	Waveform 5, 6	1.0 1.0	3.5 3.3	5.0 4.6	1.7 1.7	5.6 5.2	ns
t_{TLH} t_{THL}	Output transition time, AOn Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				2.0 2.0	5.0 5.0	ns
$t_{SK}(o)$	Output to output skew, A port [1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew 2 $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:
1. $\overline{Bn}$ to AOn propagation delays are extended for 5 nanoseconds following B port excursions above 3.1 volts.
2. $\lvert t_{PN}actual - t_{PM}actual \rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
3. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

AC ELECTRICAL CHARACTERISTICS (Continued)

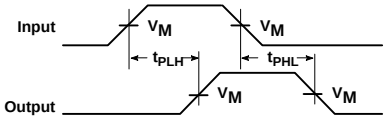
SYMBOL	PARAMETER	TEST CONDITION	B PORT LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%, C_D = 30pF, R_U = 9Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	2.9 2.9	4.3 4.4	1.0 1.0	4.8 4.6	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.3	4.5 4.8	1.0 1.0	5.1 5.1	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.4 5.1	5.7 6.6	2.4 2.0	6.4 7.1	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.6 3.3	5.0 4.9	1.4 1.0	5.7 5.2	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.0 3.1	4.5 5.0	1.0 1.0	5.0 5.6	ns
ΔV/Δt	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.4	1.2	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.8	1.5		2.0	ns
$t_{SK}(p)$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.5			ns
SYMBOL	**PARAMETER**	**TEST CONDITION**	**R_U = 16.5Ω**			**R_U = 16.5Ω**		**UNIT**
t_{PLH} t_{PHL}	Propagation delay (thru mode) AIn to $\overline{Bn}$	Waveform 1, 2	1.2 1.0	3.0 3.0	4.4 4.5	1.0 1.0	4.9 4.7	ns
t_{PLH} t_{PHL}	Propagation delay (transparent latch) AIn to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.2 3.4	4.6 4.9	1.0 1.0	5.2 5.2	ns
t_{PLH} t_{PHL}	Propagation delay LCAB to $\overline{Bn}$	Waveform 1, 2	2.7 2.2	4.5 5.2	5.8 6.7	2.4 2.0	6.5 7.2	ns
t_{PLH} t_{PHL}	Propagation delay SABn to $\overline{Bn}$	Waveform 1, 2	1.8 1.0	3.7 3.4	5.1 5.0	1.4 1.0	5.8 5.3	ns
t_{PZH} t_{PZL}	Enable/disable time OEB0 or $\overline{OEB1}$ to $\overline{Bn}$	Waveform 1, 2	1.4 1.0	3.1 3.2	4.6 5.1	1.0 1.0	5.1 5.7	ns
ΔV/Δt	Output transition rate, $\overline{Bn}$ Port 20% to 80%, 80% to 20%	Test Circuit and Waveforms				0.2	0.6	V/ns
$t_{SK}(o)$	Output to output skew, B port [1]	Waveform 3		0.5	1.0		1.5	ns
$t_{SK}(p)$	Pulse skew [2] $\lvert t_{PHL} - t_{PLH} \rvert_{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:
1. $\lvert t_{PN}$actual – t_{PM}actual $\rvert$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.).
2. $t_{SK}(p)$ is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

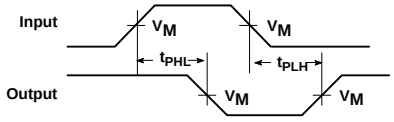
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = 5V			T_{amb} = 0 to 70°C, V_{CC} = 5V±10%		
			C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 9Ω (B side)					
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
t_w(H) t_w(L)	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
SYMBOL	PARAMETER	TEST CONDITION	C_L = 50pF (A side) / C_D = 30pF (B side) R_L = 500Ω (A side) / R_U = 16.5Ω (B side)					UNIT
t_s(H) t_s(L)	Setup time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns
t_h(H) t_h(L)	Hold time AIn to LCAB or $\overline{Bn}$ to LCBA	Waveform 4	1.0 1.0			1.3 1.3		ns
t_w(H) t_w(L)	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0			4.0 4.0		ns

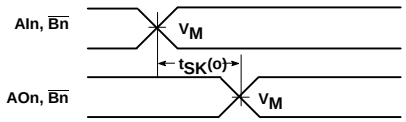
AC WAVEFORMS



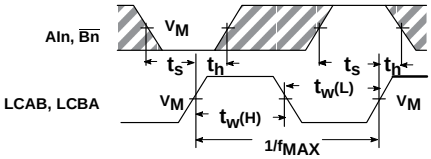
Waveform 1. Propagation Delay for Data or Output Enable to Output



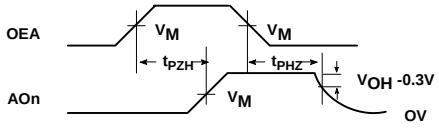
Waveform 2. Propagation Delay for Data or Output Enable to Output



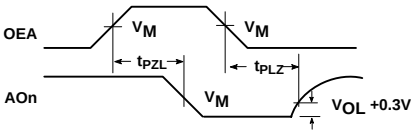
Waveform 3. Output to Output Skew



Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

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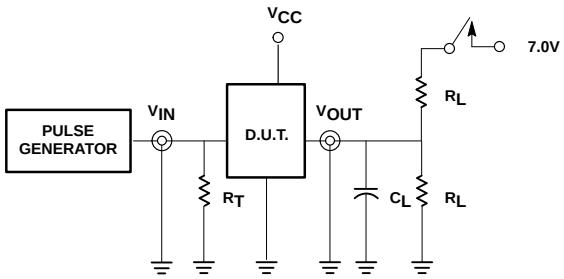
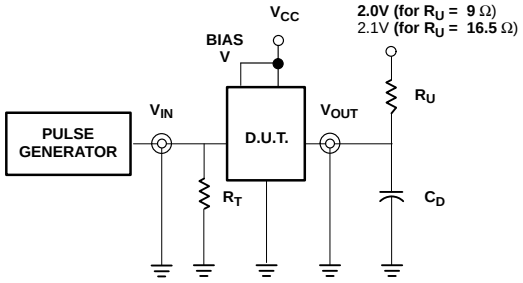
TEST CIRCUIT AND WAVEFORMS



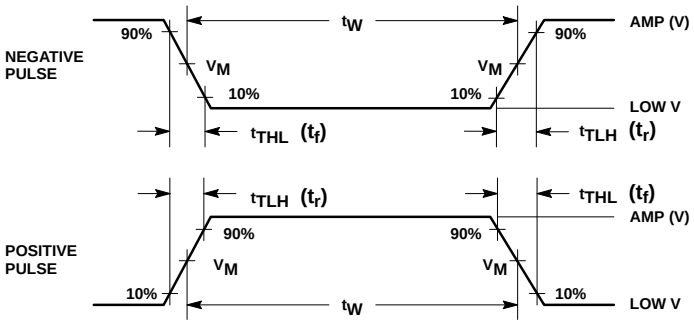
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open



Test Circuit for Outputs on B Port



V_M = 1.55V for $\overline{Bn}$, V_M = 1.5V for all others.

Input Pulse Definitions

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

DEFINITIONS:

R_L = Load Resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_U = Pull up resistor; see AC CHARACTERISTICS for value.

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