DECODER FOR COMPACT DISC DIGITAL AUDIO SYSTEM

GENERAL DESCRIPTION

The SAA7210 incorporates the functions of demodulator, subcoding processor, error corrector and concealment in one chip. The device accepts data from the disc and outputs serial data directly to a dual 16-bit digital-to-analogue converter TDA1541 (DAC) via the Inter IC signal bus (I^2S). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering. For descriptive purposes, the SAA7210 is referred to as the A-chip and the SAA7220 as the B-chip.

Features

- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Cross-Interleaved Reed-Solomon Code (CIRC) used for error correction system
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange between A-chip, B-chip and DAC
- Bidirectional data bus to external RAM (16 K x 4 bits)

purple binder, tab 6

QUICK REFERENCE DATA

Supply voltage (pin 40)	V_{DD}	typ.	5 V
Supply current (pin 40)	I_{DD}	typ.	200 mA
Data slicer input voltage range	$V_{I(p-p)}$		0,25 to 2,5 V
Oscillator operating frequency			
XTAL	f_{XTAL}	typ.	11,2896 MHz
VCO	f_{VCO}	typ.	8,6436 MHz
Maximum output current (each output)	I_O	max.	10 mA
Operating ambient temperature range	T_{amb}		−20 to +70 °C

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PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

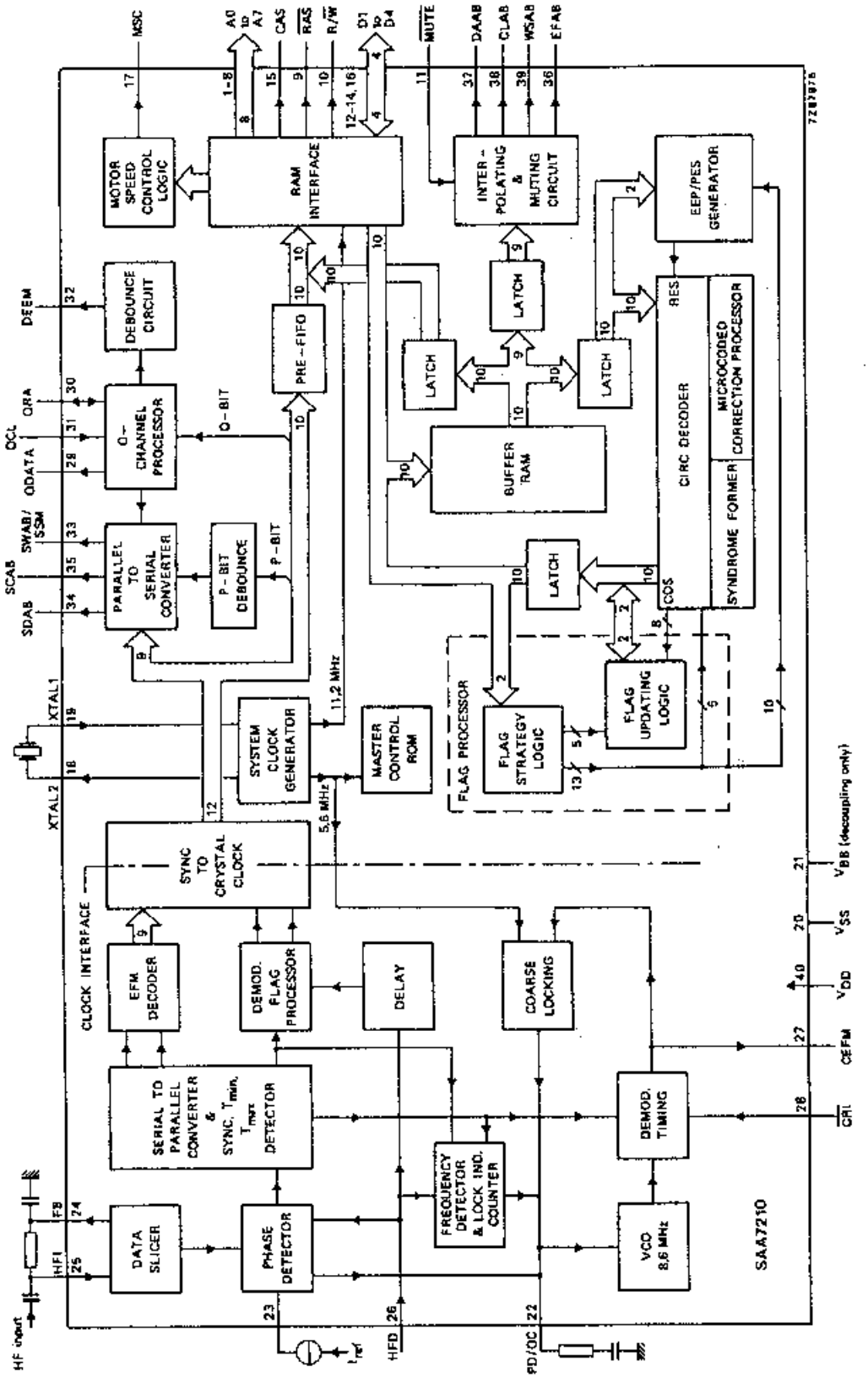


Fig. 1 Block diagram.

PHILIPS

DEVELOPMENT DATA

PINNING

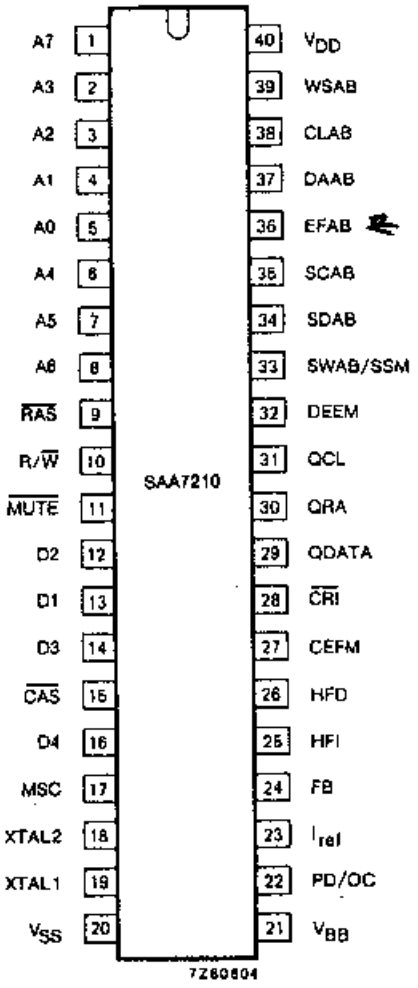


Fig. 2 Pinning diagram; for pin functions see next page.

Pin functions

pin no.	mnemonic	description
1-8	A0-A7	**Address:** address outputs to external RAM.
9	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB (pin 37) is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first "good" value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12-14	D1-D3	**Data:** data inputs/outputs to external RAM.
15	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	D4	**Data:** data input/output to external RAM.
17	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continous 50% duty factor.
18	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	V_{SS}	**Ground:** circuit earth potential.
21	V_{BB}	**Back Bias supply voltage:** back bias output voltage (−2,5 V ±20%). The internal back bias generator can be decoupled at this pin.
22	PD/OC	**Phase Detector output/Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	I_{ref}	**Current reference:** external reference input to the phase detector. This input is required to minimize the spread in the charge pump output of the phase detector. An internal clamp prevents the voltage on this pin rising above 3,5 V.
24	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input at pin 25 (HFI) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD (pin 26) is LOW, this output goes to high impedance state.
25	HFI	**High-Frequency Input:** level detector input to the data slicer. A differential signal of between 0,25 and 2,5 V (peak-to-peak value) is required to drive the data slicer correctly. When a T_{max} violation is detected or when HFD is LOW, this input is biased directly to its threshold voltage.
26	HFD	**High-Frequency Detector:** when HIGH this input signal enables the frequency and phase detector inputs, also the feedback output (FB) from the data slicer. An internal voltage clamp of 3 V (typ.) requires the HFD input to be fed via a high impedance. This input has an internal pull-up of 50 kΩ (typ.).

pin no.	mnemonic	description
27	CEFM	**Clock Eight-to-Fourteen Modulation:** demodulator clock output 4,3218 MHz (typ.).
28	$\overline{CRI}$	**Counter Reset Inhibit:** when LOW this input signal allows the divide-by-588 master counter in the DEMOD timing to run-free. This input has an internal pull-up of 50 kΩ (typ.).
29	QDATA	**Q-channel Data:** this subcoding output is parity checked and changes in response to the Q-channel clock input (see subcoding microprocessor handshaking protocol).
30	QRA	**Q-channel Request input/Acknowledge output:** the output has an internal pull-up of nominally 10 kΩ. (see subcoding microprocessor handshaking protocol).
31	QCL	**Q-channel Clock:** clock input generated by the micro-processor when it detects a QRA LOW signal.
32	DEEM	**De-emphasis:** signal derived from one bit of the parity-checked Q-channel and fed out via the debounce circuit.
33	SWAB/SSM	**Subcoding Word clock output & Start/Stop Motor input:** open drain output which is sensed during each HIGH period and if externally forced LOW a motor-stop condition will be decoded and fed to the motor control logic circuit.
34	SDAB	**Subcoding Data:** a 10-bit burst of data, including flags and sync bits, is output serially to the B-chip once per frame clocked by burst clock output SCAB (see Fig. 4).
35	SCAB	**Subcoding Clock:** a 10-bit burst clock 2,8224 MHz (typ.) output which is used to synchronize the subcoding data.
36	EFAB	**Error Flag:** output from interpolation and mute circuit to B-chip indicating unreliable data.
37	DAAB	**Data:** this output which is fed to the B-chip or DAC, together with its clock (CLAB) and word select (WSAB) outputs, conforms to the I^2S bus format (see Fig. 5).
38	CLAB	**Clock:** output to B-chip or DAC.
39	WSAB	**Word Select:** output to B-chip or DAC.
40	V_{DD}	**Power Supply:** positive supply voltage(+ 5 V).

DEVELOPMENT DATA

Note to the pin functions

The pin sequence of the address outputs (A0-A7) and the data outputs (D1-D4) has been selected to be compatible with various dynamic 16 K x 4-bit RAMs including the 4416.

FUNCTIONAL DESCRIPTION

Demodulation

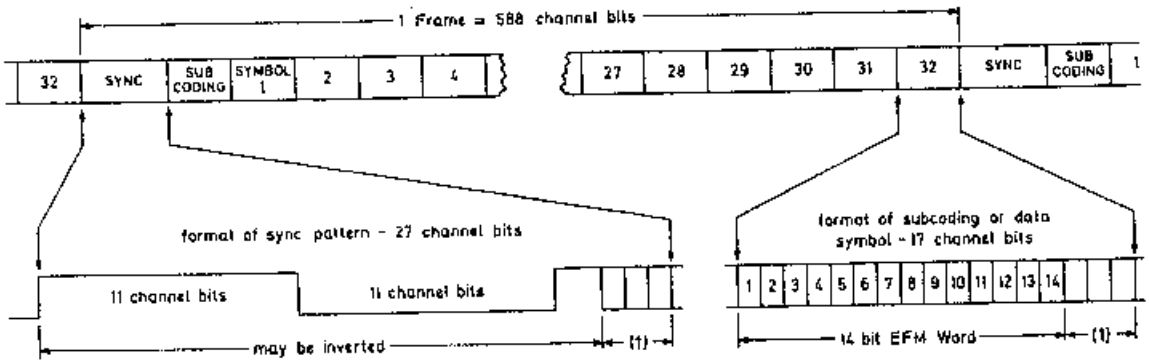
Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at twice the input data rate (typically at 8,6436 MHz), its frequency being dependent on the voltage at pin 22 (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output is divided by two to provide the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (PD/OC), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source connected to pin 23 (I_{ref}).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input (pin 28) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.



(1) = merging and low frequency suppression bits.

Fig. 3 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output to B-chip

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC-checked Q-channel. The DEEM output (pin 32) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34. The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output to the B-chip consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q-channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally on the rising edge of SWAB at pin 33 (see Fig. 4).

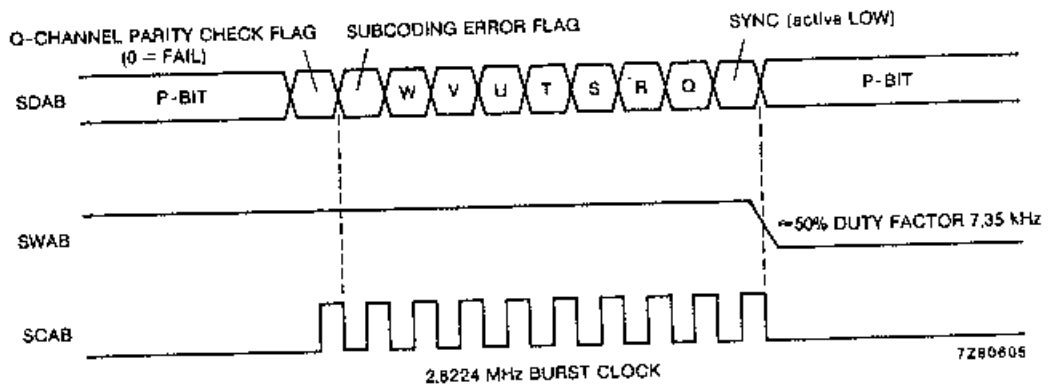


Fig. 4 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4 symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency (e.g. pitch control).

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 6) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address ($\overline{RAS}$ pin 9) is set up first and then three 4-bit nibbles are accessed using sequential column addresses ($\overline{CAS}$ pin 15). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good ' data (flags = 00) and three levels of error can be indicated.
The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

DEVELOPMENT DATA

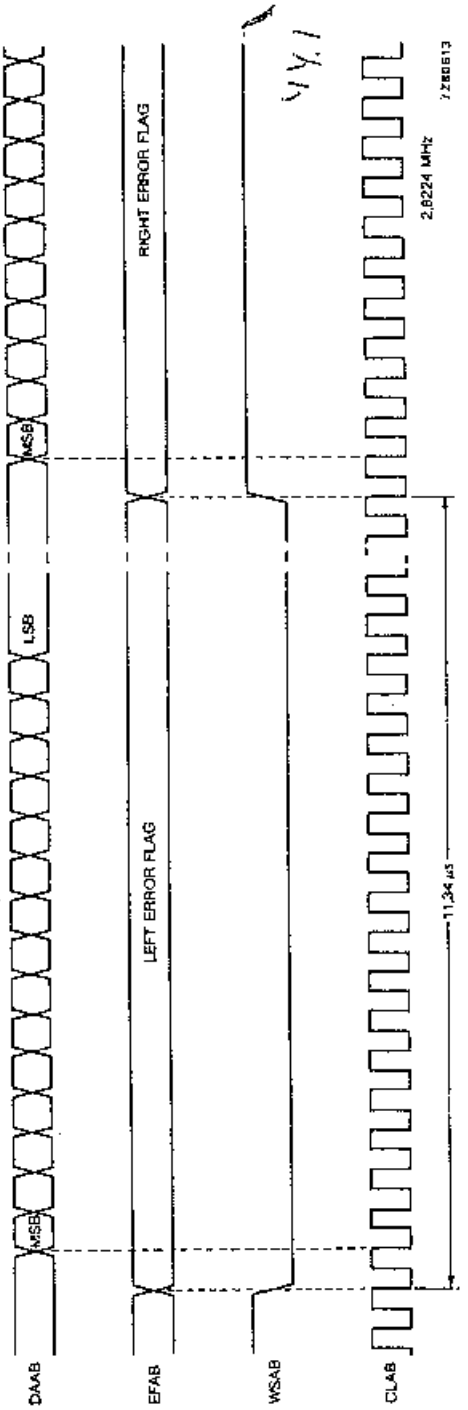


Fig. 5 Typical waveform outputs to B-chip or DAC.

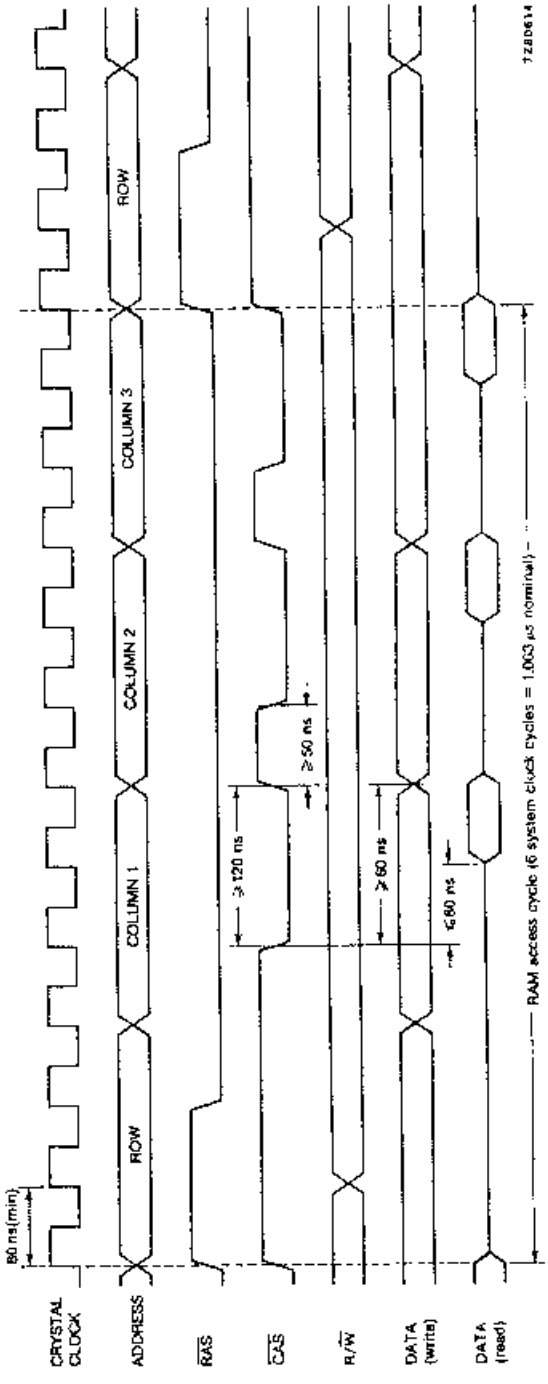


Fig. 6 RAM timing waveforms: timings based on RAM TMS4416; $\overline{G}$ input to RAM held LOW.

FUNCTIONAL DESCRIPTION (continued)

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the B-chip where it receives additional and more efficient concealment.

Motor speed control (see Fig. 7)

The motor speed control (MSC) output from pin 17 is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

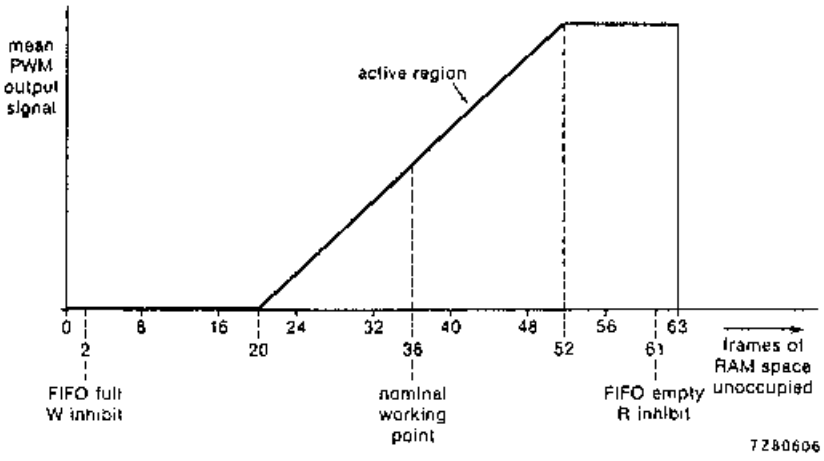


Fig. 7 Motor speed control.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 40)	V_{DD}		−0,5 to +7,0	V
Maximum input voltage range	V_I		−0,5 to V_{DD} +0,5	V
Input current (pin 23)	I_I	max.	5	mA
Maximum output voltage range (pin 17, 33)	V_O		−0,5 to +7,0	V
Output current (each output)	I_O	max.	10	mA
Storage temperature range	T_{stg}		−55 to +125	°C
Operating ambient temperature range	T_{amb}		−20 to +70	°C
Electrostatic handling *	V_{es}		−1000 to +1000	V

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −2- to +70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 40)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 40)	I_{DD}	–	200	tbf	mA
Inputs					
D1-D4, QCL					
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	$\pm I_{LI}$	–	–	10	µA
Input capacitance	C_I	–	–	7	pF
$\overline{MUTE}$, $\overline{CRI}$					
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance at V_I = 0 V	$\lvert Z_I \rvert$	tbf	50	tbf	kΩ
Input capacitance	C_I	–	–	7	pF
QRA, SWAB					
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance	C_I	–	–	7	pF
Internal pull-up impedance at V_I = 0 V	$\lvert Z_I \rvert$	5	10	–	kΩ
HFD					
Input voltage LOW	V_{IL}	−0,3	–	+0,8	V
Input voltage HIGH	V_{IH}	2,0	–	clamped	V
Input clamping voltage at I_I = 100 µA	V_{CL}	–	3	–	V
Input source current	$\pm I_S$	–	–	100	µA
Input capacitance	C_I	–	–	7	pF
Internal pull-up impedance at V_I = 0 V	$\lvert Z_I \rvert$	–	50	–	kΩ

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Outputs					
A1-A8, R/$\overline{W}$, D1-D4, $\overline{CAS}$, $\overline{RAS}$, CEFM, QDATA, DEEM, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	2,4	–	V_{DD}	V
Load capacitance	C_L	–	–	50	pF
MSC (open drain)					
Output voltage LOW at $-I_{OL}$ = 1 mA	V_{OL}	0	–	0,2	V
Load capacitance	C_L	–	–	50	pF
SWAB, QRA (open drain)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	50	pF
Internal load resistance	R_L	5	–	–	kΩ
ANALOGUE CIRCUITS					
Data slicer					
Input HFI					
A.C. input voltage range (peak-to-peak value)	$V_{I(p-p)}$	0,25	–	2,5	V
Input impedance normal (HFD HIGH)	$\lvert Z_I \rvert$	tbf	–	tbf	kΩ
disabled (HFD LOW)	$\lvert Z_I \rvert$	tbf	–	tbf	kΩ
Input capacitance	C_I	–	–	7	pF
Output FB					
Output current at V_{FB} = 2 V	I_O	tbf	100	tbf	μA
Phase detector					
Output PD/OC					
Output impedance	$\lvert Z_O \rvert$	–	tbf	–	kΩ
Control range (note 1)	α	±2,1	–	–	rad
Gain factor	G	–	tbf	–	mA/rad
Input I_{ref}					
Input reference current	I_{ref}	–	500	tbf	μA

CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Fine frequency detector					
Output PD/OC Output impedance	$\|Z_O\|$	–	2	–	kΩ
Coarse frequency detector					
Output PD/OC (note 2) Output impedance	$\|Z_O\|$	–	1	–	kΩ
Voltage controlled oscillator					
Input PD/OC Oscillator constant	K_{osc}	–	tbf	–	MHz/V
Crystal oscillator					
Input XTAL1					
Output XTAL2					
Mutual conductance at 100 kHz	G_m	1,5	–	–	mS
Small signal voltage gain ($G_V = G_m \times R_O$)	G_V	3,5	–	–	V/V
Input capacitance	C_I	–	–	10	pF
Feedback capacitance	C_{FB}	–	–	5	pF
Output capacitance	C_O	–	–	10	pF
Input leakage current	$\pm I_{LI}$	–	–	10	μA
Slave clock mode					
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	1,6	–	V_{DD} + 0,5	V
Input voltage LOW	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	V_{IH}	2,4	–	V_{DD} + 0,5	V
Input rise time (note 3)	t_r	–	–	20	ns
Input fall time (note 3)	t_f	–	–	20	ns
Input HIGH time at 1,2 V (relative to clock period)	t_{HIGH}	35	–	65	%

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TIMING					
Operating frequency (XTAL)	f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)					
coarse frequency detector inactive	f_{VCO1}	$f_{XTAL}/2$	8,6436	f_{XTAL}	MHz
no input pin 25 (HFI)	f_{VCO2}	4	–	15	MHz
Outputs (see Figs. 8 and 9)					
CEFM (note 4)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
Output HIGH time	t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (note 4) (data to B-chip; I^2S format)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB					
Data set-up time	$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB					
Data hold time	$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (note 4) (subcoding outputs)					
Output rise time	t_r	–	–	20	ns
Output fall time	t_f	–	–	20	ns
SDAB to SCAB					
Subcoding data set-up time	$t_{SU;SDAT}$	100	–	–	ns
SCAB to SDAB					
Subcoding data hold time	$t_{HD;SDAT}$	100	–	–	ns
SWAB (note 4)					
Output rise time	t_r	–	–	1	μs
Output fall time	t_f	–	–	100	ns
Output duty factor		–	50	–	%

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Q-channel I/O (see Figs. 12 and 13)					
QRA, QCL, QDATA					
Access time (note 5)					
normal mode	$t_{ACC;N}$	0	–	13,3 + n x 13,3	ms
refresh mode	$t_{ACC;F}$	13,3	–	n x 13,3	ms
QCL to QRA acknowledge delay	t_{DACK}	–	–	500	ns
QCL to QRA request hold time	$t_{HD;R}$	500	–	–	ns
QCL clock input LOW time	$t_{CK;LOW}$	500	–	–	ns
QCL clock input HIGH time	$t_{CK;HIGH}$	500	–	–	ns
QCL to QDATA delay time	t_{DD}	–	–	500	ns
Data hold time before new frame is accessed	$t_{HD;ACC}$	2,3	–	–	ms
Acknowledge time	t_{ACK}	–	–	10,8	ms

Notes to the characteristics

1. 1 rad = $\frac{180^{o}}{(3,14)}$.
2. Coarse frequency detector output PD/OC active for VCO frequencies > f_{XTAL} and < $\frac{f_{XTAL}}{2}$.
3. Reference levels = 1 V and 2,4 V.
4. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
5. Q-channel access times dependent on cyclic redundancy check (CRC).

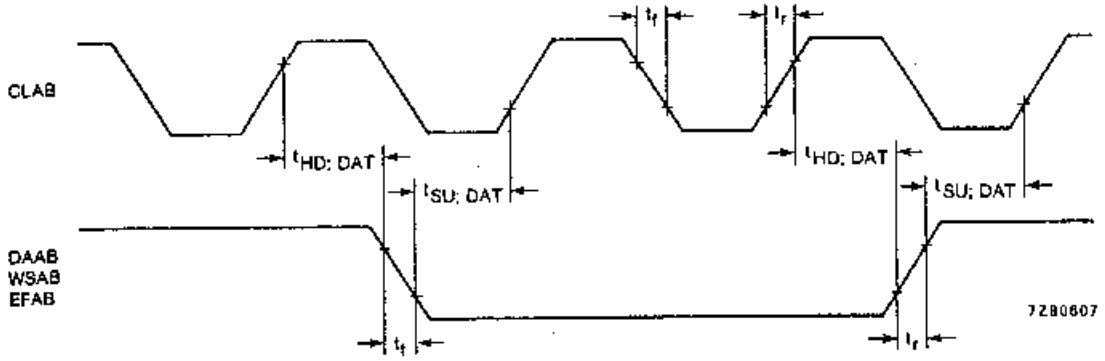


Fig. 8 Typical data output waveforms to B-chip or DAC: reference levels = 0,8 V and 2,0 V.

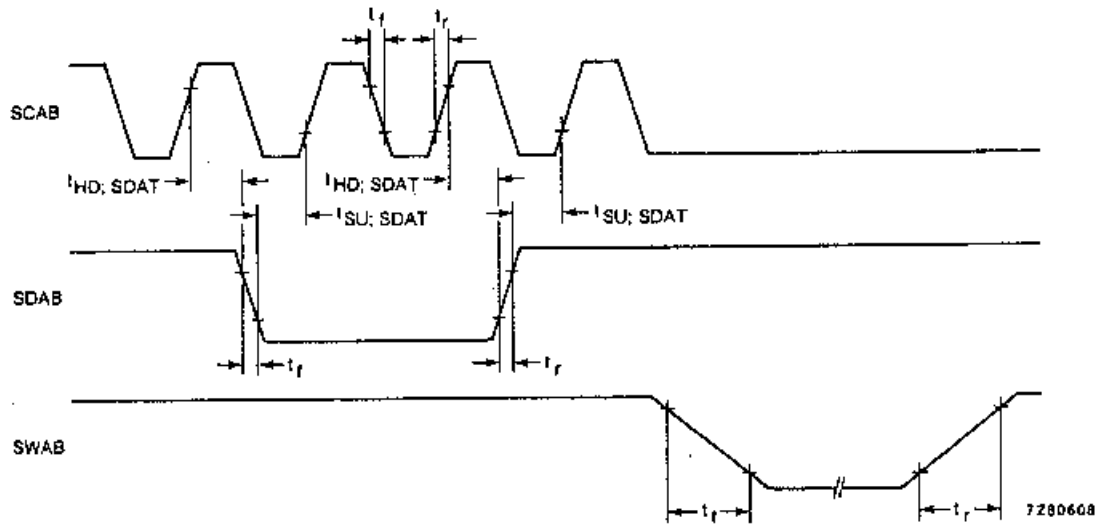


Fig. 9 Typical subcoding data output waveforms: reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a d.c. free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the d.c. content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 10).

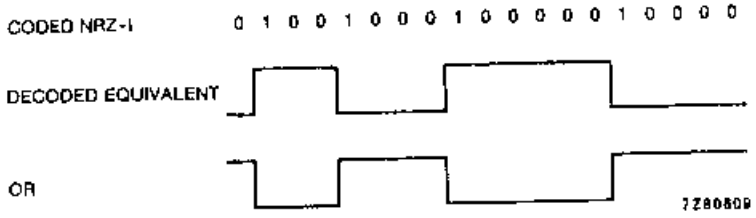


Fig. 10 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word												
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
X	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
X	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

Table 2 EFM code conversion

No.	DNZ data symbol D1 D8	equivalent code word C1 C14	No.	DNZ data symbol D1 D8	equivalent code word C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11			139		
to			to		
119			247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 0 1 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 0 1 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 0 1 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 0 1 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 0 1 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 0 1 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

APPLICATION INFORMATION (continued)

Subcoding microprocessor handshaking protocol (see Figs. 11, 12 and 13)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7210.

The SAA7210 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7210 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7210 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowledge signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7210 now disables the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7210 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7210 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

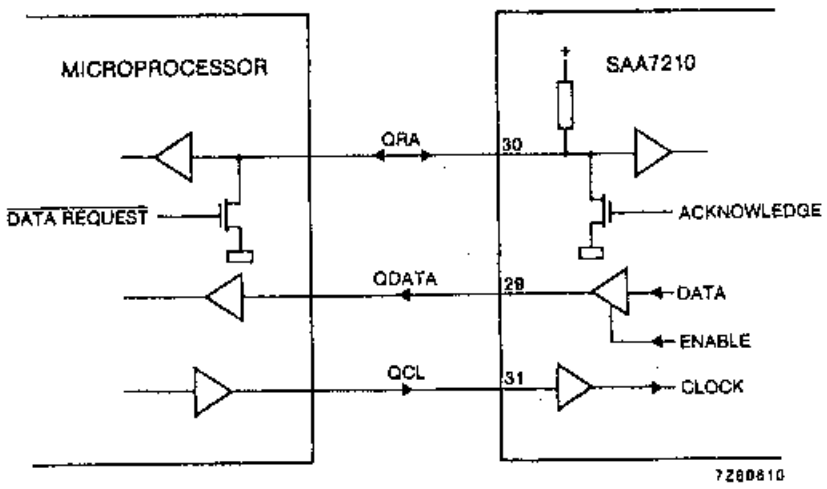


Fig. 11 Microprocessor handshaking protocol.

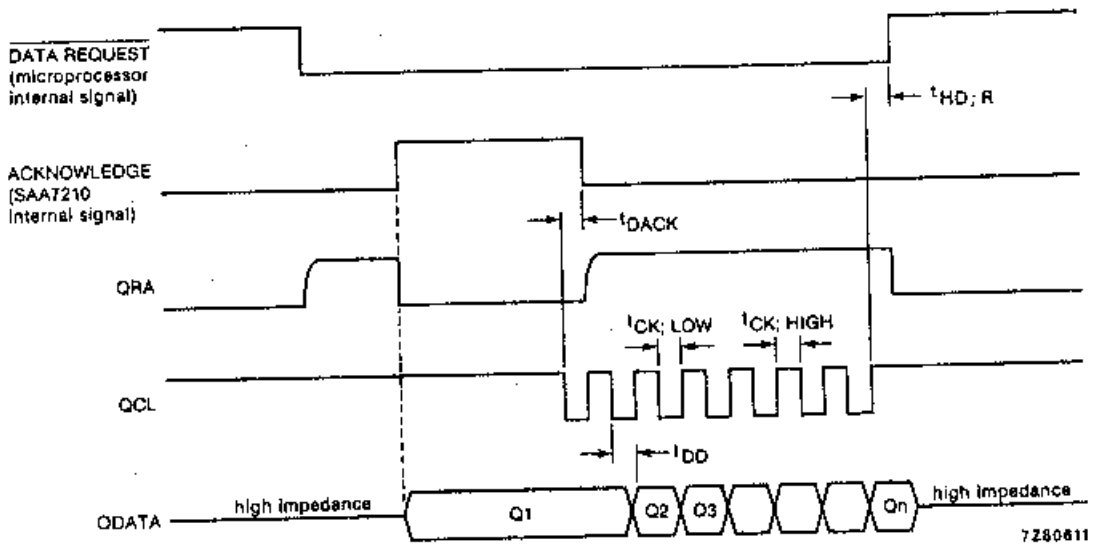


Fig. 12 Q-channel timing waveforms (normal mode).

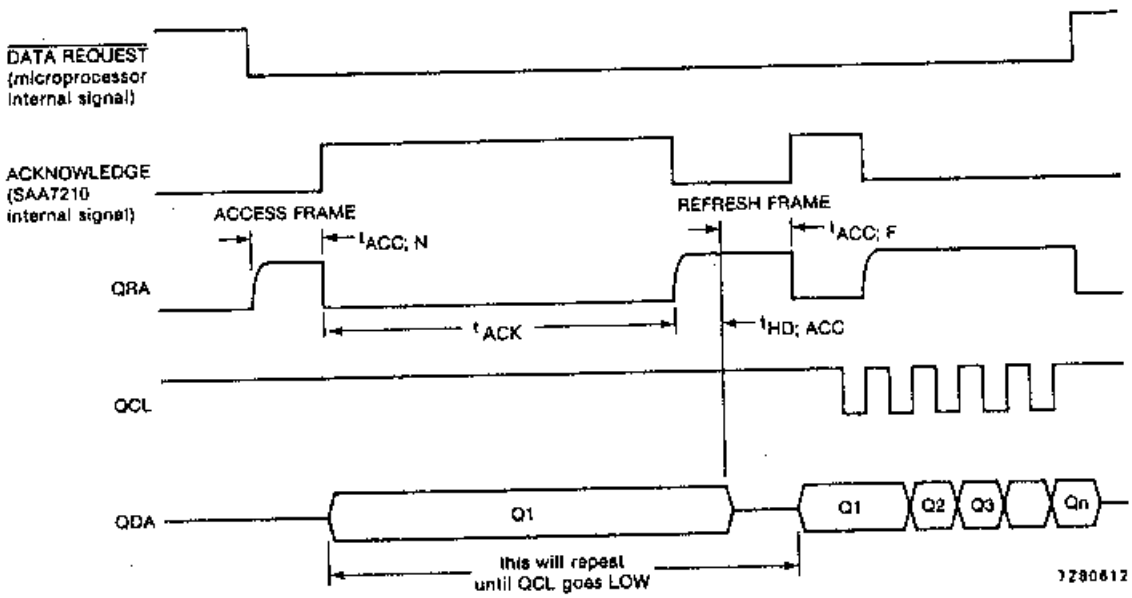
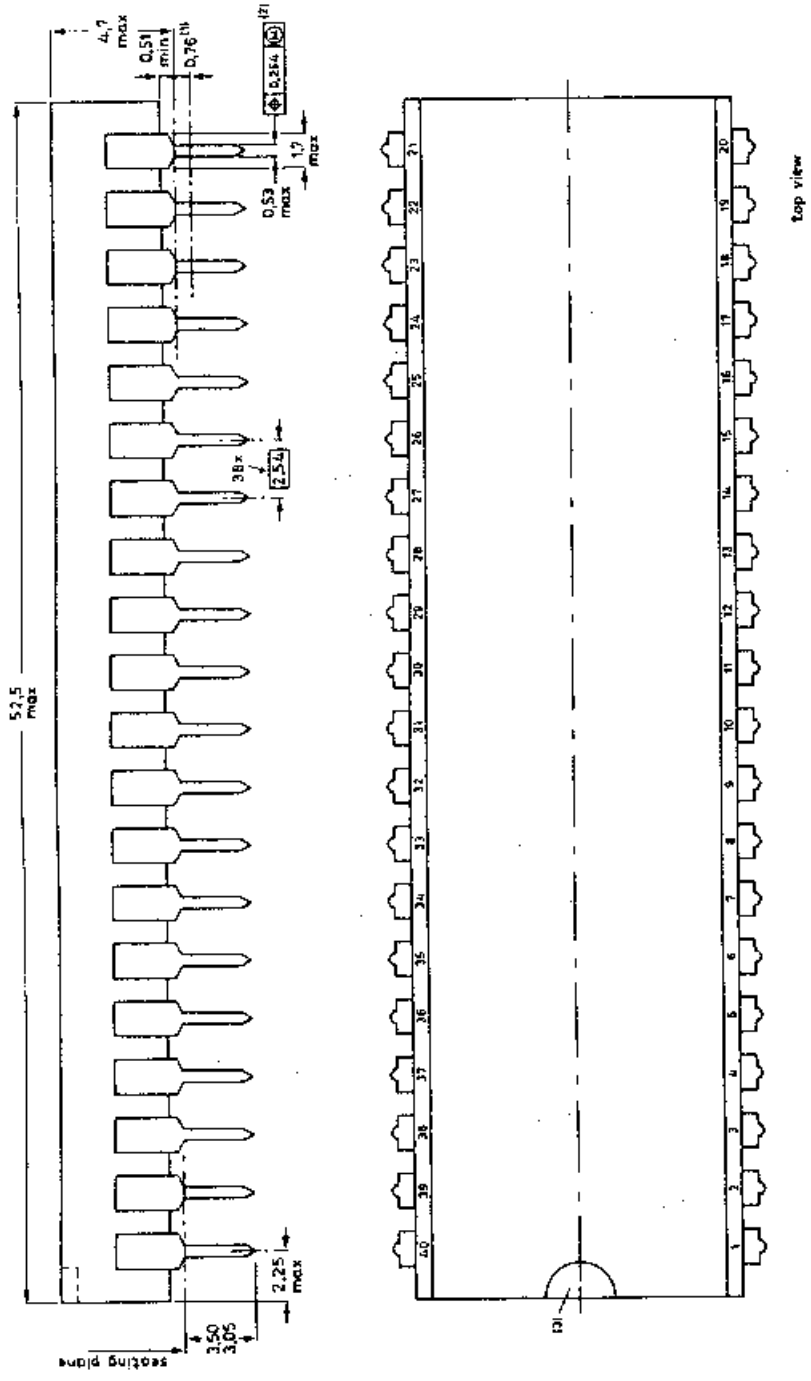
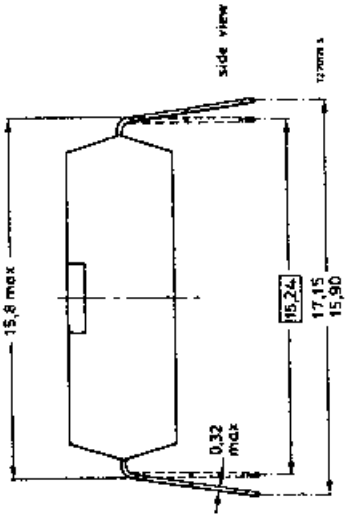


Fig. 13 Q-channel timing waveforms (refresh mode).

40-LEAD DUAL IN-LINE; PLASTIC (SOT-129)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm