# DATA SHEET

## FB2041
## 7-bit Futurebus+ transceiver

Product specification

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Philips
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PHILIPS

# 7-bit Futurebus+ transceiver FB2041

## DESCRIPTION

The FB2041 is a 7-bit bidirectional BTL transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. The FB2041 is an inverting transceiver.

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

## FEATURES

- 7-bit BTL transceiver
- Separate I/O on TTL A-port
- Inverting
- Three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Controlled output ramp and multiple GND pins minimize ground bounce
- Each BTL driver has a dedicated Bus GND for a signal return
- Glitch-free power up/power down operation
- Low $I_{CC}$ current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack

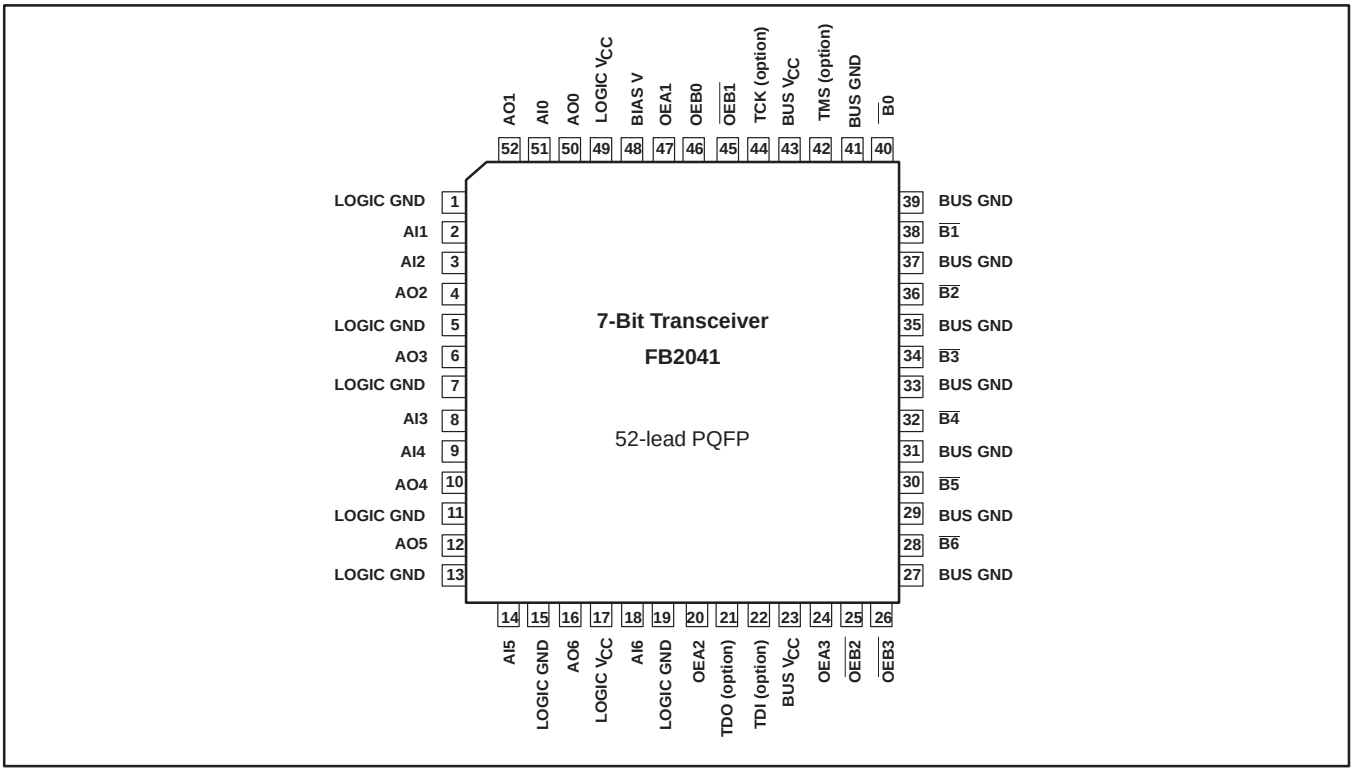
## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>AIn to $\overline{Bn}$ | | 3.7<br>2.7 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay<br>$\overline{Bn}$ to AOn | | 3.4<br>3.2 | ns |
| $C_{OB}$ | Output capacitance ($\overline{B0}$ - $\overline{B6}$ only) | | 6 | pF |
| $I_{OL}$ | Output current ($\overline{B0}$ - $\overline{B6}$ only) | | 100 | mA |
| $I_{CC}$ | Supply Current | Standby | 19 | mA |
| | | AIn to $\overline{Bn}$ (outputs Low or High) | 40 | |
| | | $\overline{Bn}$ to AOn (outputs Low) | 22 | |
| | | $\overline{Bn}$ to AOn (outputs High) | 19 | |

## ORDERING INFORMATION

| PACKAGE | COMMERCIAL RANGE<br>$V_{CC}$ = 5V±10%; $T_{amb}$ = 0 to +70°C | INDUSTRIAL RANGE<br>$V_{CC}$ = 5V±10%; $T_{amb}$ = -40 to +85°C | DWG No. |
|---|---|---|---|
| 52-pin Plastic Quad Flatpack | FB2041BB | CD3207BB | SOT379-1 |

## PIN CONFIGURATION




The B-port interfaces to “Backplane Transceiver Logic” (See the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1Vp-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

There are three separate pairs of driver enables in a 1 bit, 3 bit, 3 bit arrangement. The TTL/BTL output drivers for bit 0 are enabled with OEA1/$\overline{\text{OEB1}}$, output drivers for bits 1–2–3 are enabled with OEA2/$\overline{\text{OEB2}}$ and output drivers for bits 4–5–6 are enabled with OEA3/$\overline{\text{OEB3}}$.

The A-port operates at TTL levels with separate I/O. The 3-state A-port drivers are enabled when OEAn goes High after an extra 6ns delay which is built in to provide a break-before-make function. When OEAn goes Low, A-port drivers become High impedance without any extra delay. During power on/off cycles, the A-port drivers are held in a High impedance state when $V_{CC}$ is below 2.5V.

The B-port has an output enable, $\overline{\text{OEB0}}$, which affects all seven drivers. When OEB0 is High and $\overline{\text{OEBn}}$ is Low the output driver will be enabled. When OEB0 is Low or if $\overline{\text{OEBn}}$ is High, the B-port drivers will be inactive and at the level of the backplane signal.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 5V level while $V_{CC}$ is Low. If live insertion is not a requirement, the BIAS V pin should be tied to a $V_{CC}$ pin.

The LOGIC GND and BUS GND pins are isolated in the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a “hard” signal failure occurs instead of a pattern dependent error that may be very infrequent and impossible to trouble-shoot.

The LOGIC $V_{CC}$ and BUS $V_{CC}$ pins are also isolated internally to minimize noise and may be externally decoupled separately or simply tied together.

JTAG boundary scan functionality is provided as an option with signals TMS, TCK, TDI and TDO. When this option is not present, TMS and TCK are no-connects (no bond wires) and TDI and TDO are shorted together internally.

## PIN DESCRIPTION

| SYMBOL | PIN NUMBER | TYPE | NAME AND FUNCTION |
|---|---|---|---|
| AI0 – AI6 | 51, 2, 3, 8, 9, 14, 18 | Input | Data inputs (TTL) |
| AO0 – AO6 | 50, 52, 4, 6, 10, 12, 16 | Output | 3-state outputs (TTL) |
| $\overline{B0}$ – $\overline{B6}$ | 40, 38, 36, 34, 32, 30, 28 | I/O | Data inputs/Open Collector outputs, High current drive (BTL) |
| OEB0 | 46 | Input | Enables the Bn outputs when High |
| $\overline{OEB1}$ | 45 | Input | Enables the B0 output when Low |
| $\overline{OEB2}$ | 25 | Input | Enables the B1 – B3 outputs when Low |
| $\overline{OEB3}$ | 26 | Input | Enables the B4 – B6 outputs when Low |
| OEA1 | 47 | Input | Enables the A0 outputs when High |
| OEA2 | 20 | Input | Enables the A1 – A3 outputs when High |
| OEA3 | 24 | Input | Enables the A4 – A6 outputs when High |
| BUS GND | 41, 39, 37, 35, 33, 31, 29, 27 | GND | Bus ground (0V) |
| LOGIC GND | 1, 5, 7, 11, 13, 15, 19 | GND | Logic ground (0V) |
| BUS $V_{CC}$ | 23, 43 | Power | Positive supply voltage |
| LOGIC $V_{CC}$ | 17, 49 | Power | Positive supply voltage |
| BIAS V | 48 | Power | Positive supply voltage |
| TMS | 42 | Input | Test Mode Select (no-connect) |
| TCK | 44 | Input | Test Clock (no-connect) |
| TDI | 22 | Input | Test Data In (shorted to TDO) |
| TDO | 21 | Output | Test Data Out (TDI) |

## ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

| SYMBOL | PARAMETER | | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | -0.5 to +7.0 | V |
| $V_{IN}$ | Input voltage | AI0 – AI6, OEB0, $\overline{OEBn}$, OEAn | -1.2 to +7.0 | V |
| | | $\overline{B0}$ – $\overline{B6}$ | -1.2 to +5.5 | |
| $I_{IN}$ | Input current | | -18 to +5.0 | mA |
| $V_{OUT}$ | Voltage applied to output in High output state | | -0.5 to +$V_{CC}$ | V |
| $I_{OUT}$ | Current applied to output in Low output state | AO0 – AO6 | 48 | mA |
| | | $\overline{B0}$ – $\overline{B6}$ | 200 | |
| $T_{STG}$ | Storage temperature | | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | COMMERCIAL LIMITS $V_{CC}$ = 5V±10%; $T_{amb}$ = 0 to +70°C | | | INDUSTRIAL LIMITS $V_{CC}$ = 5V±10%; $T_{amb}$ = -40 to +85°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | Except $\overline{B0}$–$\overline{B6}$ | 2.0 | | | 2.0 | | | V |
| | | $\overline{B0}$ – $\overline{B6}$ | 1.62 | 1.55 | | 1.62 | 1.55 | | |
| $V_{IL}$ | Low-level input voltage | Except $\overline{B0}$–$\overline{B6}$ | | | 0.8 | | | 0.8 | V |
| | | $\overline{B0}$ – $\overline{B6}$ | | | 1.47 | | | 1.47 | |
| $I_{IK}$ | Input clamp current | | | | -18 | | | -18 | mA |
| $I_{OH}$ | High-level output current | AO0 – AO6 | | | -3 | | | -3 | mA |
| $I_{OL}$ | Low-level output current | AO0 – AO6 | | | 24 | | | 24 | mA |
| | | $\overline{B0}$ – $\overline{B6}$ | | | 100 | | | 100 | |
| $C_{OB}$ | Output capacitance on B port | | | 6 | 7 | | 6 | 7 | pF |
| $T_{amb}$ | Operating free-air temperature range | | 0 | | +70 | -40 | | +85 | °C |

## FUNCTION TABLE

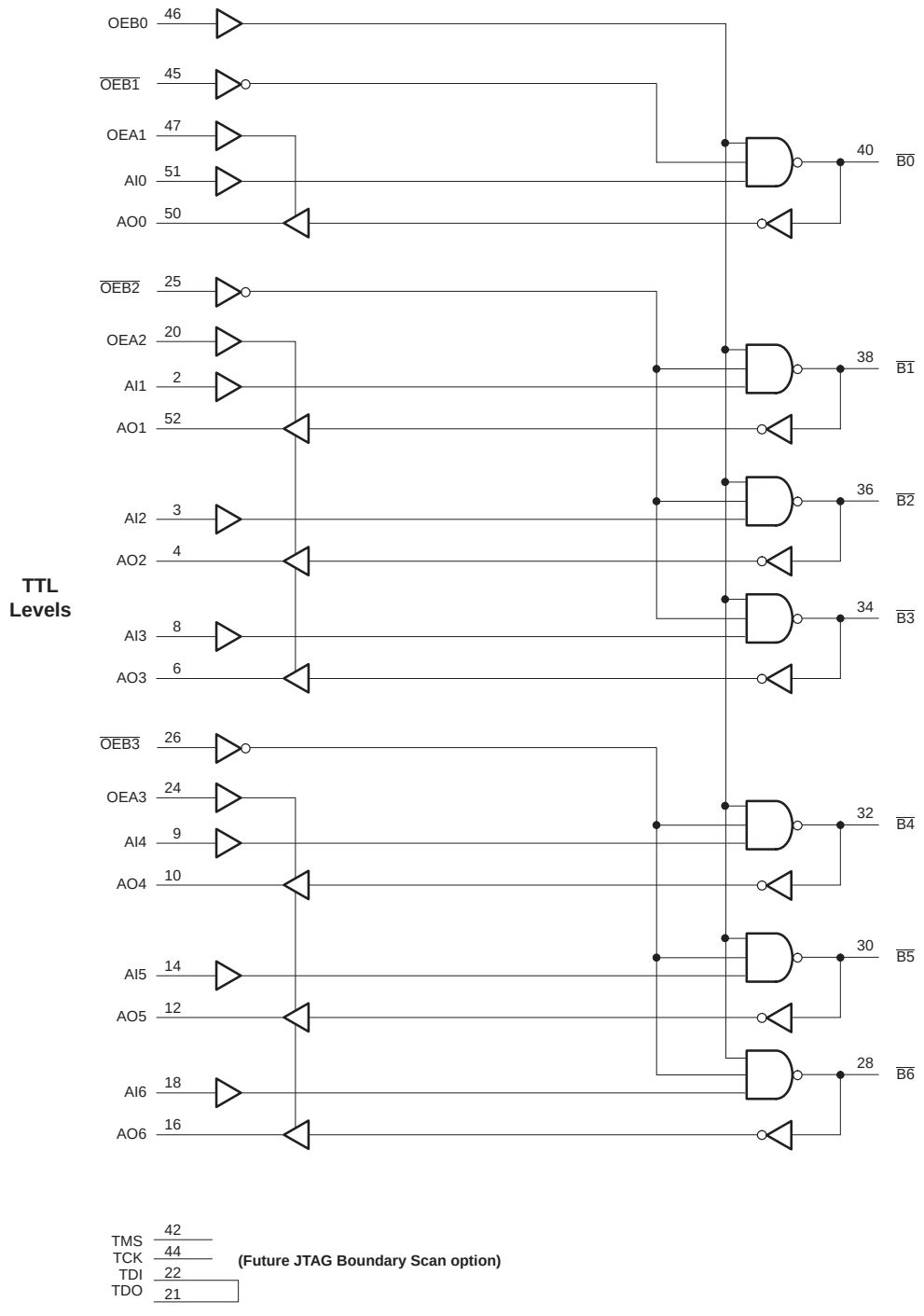
| MODE | INPUTS | | | | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | AIn | $\overline{Bn}$* | OEB0 | $\overline{OEB1}$ | $\overline{OEB2}$ | $\overline{OEB3}$ | OEA1 | OEA2 | OEA3 | AOn | $\overline{Bn}$* |
| AIn to $\overline{Bn}$ | L | — | H | L | L | L | L | L | L | Z | H** |
| | H | — | H | L | L | L | L | L | L | Z | L |
| | L | — | H | L | L | L | H | H | H | L | H** |
| | H | — | H | L | L | L | H | H | H | H | L |
| AI0 to $\overline{B0}$ | L | — | H | L | X | X | L | L | L | Z | H** |
| | H | — | H | L | X | X | L | L | L | Z | L |
| | L | — | H | L | X | X | H | H | H | L | H** |
| | H | — | H | L | X | X | H | H | H | H | L |
| AI1 – AI3 to $\overline{B1}$ – $\overline{B3}$ | L | — | H | X | L | X | L | L | L | Z | H** |
| | H | — | H | X | L | X | L | L | L | Z | L |
| | L | — | H | X | L | X | H | H | H | L | H** |
| | H | — | H | X | L | X | H | H | H | H | L |
| AI4 – AI6 to $\overline{B4}$ – $\overline{B6}$ | L | — | H | X | X | L | L | L | L | Z | H** |
| | H | — | H | X | X | L | L | L | L | Z | L |
| | L | — | H | X | X | L | H | H | H | L | H** |
| | H | — | H | X | X | L | H | H | H | H | L |
| Disable $\overline{Bn}$ outputs | X | X | L | X | X | X | X | X | X | X | H** |
| | X | X | X | H | H | H | X | X | X | X | H** |
| Disable $\overline{B0}$ outputs | X | X | H | H | X | X | X | X | X | X | H** |
| Disable $\overline{B1}$ – $\overline{B3}$ outputs | X | X | H | X | H | X | X | X | X | X | H** |
| Disable $\overline{B4}$ – $\overline{B6}$ outputs | X | X | H | X | X | H | X | X | X | X | H** |
| $\overline{Bn}$ to AOn | X | L | L | X | X | X | H | H | H | H | Input |
| | X | H | L | X | X | X | H | H | H | L | Input |
| | X | L | X | H | H | H | H | H | H | H | Input |
| | X | H | X | H | H | H | H | H | H | L | Input |
| $\overline{B0}$ to AO0 | X | L | L | X | X | X | H | X | X | H | Input |
| | X | H | L | X | X | X | H | X | X | L | Input |
| | X | L | X | H | H | H | H | X | X | H | Input |
| | X | H | X | H | H | H | H | X | X | L | Input |
| $\overline{B1}$ – $\overline{B3}$ to AO1 – AO3 | X | L | L | X | X | X | X | H | X | H | Input |
| | X | H | L | X | X | X | X | H | X | L | Input |
| | X | L | X | H | H | H | X | H | X | H | Input |
| | X | H | X | H | H | H | X | H | X | L | Input |
| $\overline{B4}$ – $\overline{B6}$ to AO4 – AO6 | X | L | L | X | X | X | X | X | H | H | Input |
| | X | H | L | X | X | X | X | X | H | L | Input |
| | X | L | X | H | H | H | X | X | H | H | Input |
| | X | H | X | H | H | H | X | X | H | L | Input |
| Disable AOn outputs | X | X | X | X | X | X | L | L | L | Z | X |
| Disable AO0 outputs | X | X | X | X | X | X | L | X | X | Z | X |
| Disable AO1 – AO3 outputs | X | X | X | X | X | X | X | L | X | Z | X |
| Disable AO4 – AO6 outputs | X | X | X | X | X | X | X | X | L | Z | X |

**NOTES:**

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

Z = High-impedance (OFF) state
— = Input not externally driven
H** = Goes to level of pull-up voltage
B* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.

## LOGIC DIAGRAM




LOGIC $V_{CC}$ = 17, 49
LOGIC GND = 1, 5, 7, 11, 13, 15, 19
BUS $V_{CC}$ = 23, 43
BUS GND = 27, 29, 31, 33, 35, 37, 39, 41
BIAS V = 48

*SG00071*

## LIVE INSERTION SPECIFICATIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{BIASV}$ | Bias pin voltage | $V_{CC}$ = 0 to 5.25V, $\overline{Bn}$ = 0 to 2.0V | 4.5 | | 5.5 | V |
| $I_{BIASV}$ | Bias pin DC current | $V_{CC}$ = 0 to 4.75V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V | | | 1 | mA |
| | | $V_{CC}$ = 4.5 to 5.5V, $\overline{Bn}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V | | | 10 | µA |
| $V_{\overline{Bn}}$ | Bus voltage during prebias | $\overline{B0}$ – $\overline{B8}$ = 0V, Bias V = 5.0V | 1.62 | | 2.1 | V |
| $I_{LM}$ | Fall current during prebias | $\overline{B0}$ – $\overline{B8}$ = 2V, Bias V = 4.5 to 5.5V | 1 | | | µA |
| $I_{HM}$ | Rise current during prebias | $\overline{B0}$ – $\overline{B8}$ = 1V, Bias V = 4.5 to 5.5V | -1 | | | µA |
| $I_{\overline{Bn}PEAK}$ | Peak bus current during insertion | $V_{CC}$ = 0 to 5.25V, $\overline{B0}$ – $\overline{B8}$ = 0 to 2.0V, Bias V = 4.5 to 5.5V, OEB0 = 0.8V, $t_r$ = 2ns | | | 10 | mA |
| $I_{OL}OFF$ | Power up current | $V_{CC}$ = 0 to 5.25V, OEB0 = 0.8V | | | 100 | µA |
| | | $V_{CC}$ = 0 to 2.2V, OEB0 = 0 to 5V | | | 100 | |
| $t_{GR}$ | Input glitch rejection | $V_{CC}$ = 5.0V | 1.0 | 1.35 | | ns |

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

| SYMBOL | PARAMETER | | TEST CONDITIONS[1] | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP[2] | MAX | |
| $I_{OH}$ | High level output current | $\overline{B0}$ – $\overline{B6}$ | $V_{CC}$ = MAX, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $V_{OH}$ = 2.1V | | | 100 | µA |
| $I_{OFF}$ | Power-off output current | $\overline{B0}$ – $\overline{B6}$ | $V_{CC}$ = 0.0V, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $V_{OH}$ = 2.1V | | | 100 | µA |
| $V_{OH}$ | High-level output voltage | AO0 – AO6 [3] | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OH}$ = -3mA | 2.5 | 2.85 | | V |
| $V_{OL}$ | Low-level output voltage | AO0 – AO6 [3] | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OL}$ = 24mA | | 0.33 | 0.5 | V |
| | | $\overline{B0}$ – $\overline{B6}$ | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OL}$ = 80mA | .75 | 1.0 | 1.10 | |
| | | | $V_{CC}$ = MIN, $V_{IL}$ = MAX, $V_{IH}$ = MIN, $I_{OL}$ = 100mA | | | 1.15 | |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = $I_{IK}$ | | | -1.2 | V |
| $I_I$ | Input current at maximum input voltage | OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6 | $V_{CC}$ = MAX, $V_I$ = GND or 5.5V | | | ±50 | µA |
| $I_{IH}$ | High-level input current | OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6 | $V_{CC}$ = MAX, $V_I$ = 2.7V | | | 20 | µA |
| | | $\overline{B0}$ – $\overline{B6}$ | $V_{CC}$ = MAX, $V_I$ = 2.1V | | | 100 | |
| $I_{IL}$ | Low-level input current | OEB0, $\overline{OEBn}$, OEAn, AI0 – AI6 | $V_{CC}$ = MAX, $V_I$ = 0.5V | | | -20 | µA |
| | | $\overline{B0}$ – $\overline{B6}$ | $V_{CC}$ = MAX, $V_I$ = 0.75V | | | -100 | |
| $I_{OZH}$ | Off-state output current | AO0 – AO6 | $V_{CC}$ = MAX, $V_O$ = 2.7V | | | 50 | µA |
| $I_{OZL}$ | Off-state output current | AO0 – AO6 | $V_{CC}$ = MAX, $V_O$ = 0.5V | | | -50 | µA |
| $I_O$ | Output current | AO0 – AO6 only | $V_{CC}$ = MAX | -30 | -55 | -150 | mA |
| $I_{CC}$ | Supply current (total) | $I_{CCZ}$ (standby) | $V_{CC}$ = MAX | | 19 | 30 | mA |
| | | $I_{CCB}$, AIn to $\overline{Bn}$ | $V_{CC}$ = MAX, outputs Low or High | | 40 | 60 | |
| | | $I_{CCA}$, $\overline{Bn}$ to AOn | $V_{CC}$ = MAX, outputs Low | | 22 | 35 | |
| | | $I_{CCA}$, $\overline{Bn}$ to AOn | $V_{CC}$ = MAX, outputs High | | 19 | 35 | |

**NOTES:**
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
2. All typical values are at $V_{CC}$ = 5V, $T_A$ = 25°C.
3. Due to test equipment limitations, actual test conditions are $V_{IH}$ = 1.8V and $V_{IL}$ = 1.3V for the B side.

## AC ELECTRICAL CHARACTERISTICS (Commercial)

| SYMBOL | PARAMETER | TEST CONDITION | A PORT LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = 5V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = 0 to 70°C, $V_{CC}$ = 5V±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>$\overline{Bn}$ to AOn | Waveform 1, 2 | 1.8<br>1.6 | 3.4<br>3.2 | 5.0<br>4.9 | 1.6<br>1.6 | 5.5<br>5.0 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time,<br>OEA to AOn | Waveform 4, 5 | 2.2<br>2.0 | 5.0<br>4.0 | 6.5<br>6.5 | 2.0<br>1.8 | 10.0<br>8.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time,<br>OEA to AOn | Waveform 4, 5 | 1.5<br>1.8 | 3.3<br>3.0 | 4.8<br>5.0 | 1.2<br>1.5 | 5.0<br>5.5 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, AOn Port<br>(10% to 90% or 90% to 10%) | Test Circuit and Waveforms | 1.5<br>1.5 | 2.2<br>2.4 | 3.0<br>3.0 | 1.5<br>1.5 | 3.5<br>3.5 | ns |
| $t_{SK}(o)$ | Output skew between receivers in same package[1] | Waveform 3 | | 0.4 | 1.0 | | 1.0 | ns |
| **SYMBOL** | **PARAMETER** | **TEST CONDITION** | **B PORT LIMITS** | | | | | **UNIT** |
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = 5V, $C_D$ = 30pF, $R_U$ = 9Ω | | | $T_{amb}$ = 0 to 70°C, $V_{CC}$ = 5V±10%, $C_D$ = 30pF, $R_U$ = 9Ω | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>AIn to $\overline{Bn}$ | Waveform 1, 2 | 2.4<br>1.5 | 3.7<br>2.7 | 4.9<br>4.4 | 1.9<br>1.5 | 5.7<br>5.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>OEB0 to $\overline{Bn}$ | Waveform 2 | 2.4<br>1.9 | 3.7<br>3.5 | 4.9<br>4.9 | 1.9<br>1.8 | 6.4<br>5.4 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>$\overline{OEB1}$ to $\overline{Bn}$ | Waveform 1 | 2.4<br>1.9 | 4.0<br>3.6 | 5.5<br>5.5 | 1.9<br>2.5 | 5.9<br>5.9 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, $\overline{Bn}$ Port<br>(1.3V to 1.8V) | Test Circuit and Waveforms | 1.0<br>0.5 | 1.4<br>1.1 | 3.0<br>3.0 | 1.0<br>0.5 | 3.0<br>3.0 | ns |
| $t_{SK}(o)$ | Output skew between drivers in same package[1] | Waveform 3 | | 0.3 | 1.0 | | 1.0 | ns |
| **SYMBOL** | **PARAMETER** | **TEST CONDITION** | $R_U$ = 16.5Ω | | | $R_U$ = 16.5Ω | | **UNIT** |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>AIn to $\overline{Bn}$ | Waveform 1, 2 | 2.5<br>1.6 | 3.8<br>2.8 | 5.0<br>4.5 | 2.0<br>1.6 | 5.8<br>5.1 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>OEB0 to $\overline{Bn}$ | Waveform 2 | 2.5<br>2.0 | 3.8<br>3.6 | 5.0<br>5.0 | 2.0<br>1.9 | 6.5<br>5.5 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>$\overline{OEB1}$ to $\overline{Bn}$ | Waveform 1 | 2.5<br>2.0 | 4.1<br>3.7 | 5.6<br>5.6 | 2.0<br>2.6 | 6.0<br>6.0 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, $\overline{Bn}$ Port<br>(1.3V to 1.8V) | Test Circuit and Waveforms | 1.0<br>0.5 | 1.5<br>1.1 | 3.0<br>3.0 | 1.0<br>0.5 | 3.0<br>3.0 | ns |
| $t_{SK}(o)$ | Output skew between drivers in same package[1] | Waveform 3 | | 0.3 | 1.0 | | 1.0 | ns |

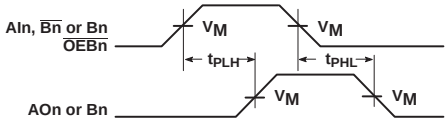
**NOTES:**
1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, $V_{CC}$, loading, etc.).

## AC ELECTRICAL CHARACTERISTICS (Industrial)

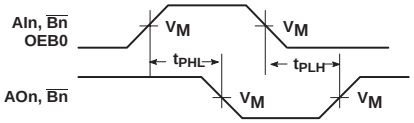
| SYMBOL | PARAMETER | TEST CONDITION | A PORT LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = 5V, $C_L$ = 50pF, $R_L$ = 500Ω | | | $T_{amb}$ = -40 to +85°C, $V_{CC}$ = 5V±10%, $C_L$ = 50pF, $R_L$ = 500Ω | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>$\overline{Bn}$ to AOn | Waveform 1, 2 | 1.8<br>1.6 | 3.4<br>3.2 | 5.0<br>4.9 | 1.6<br>1.6 | 5.5<br>5.5 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output enable time,<br>OEA to AOn | Waveform 4, 5 | 2.2<br>2.0 | 5.0<br>4.0 | 6.5<br>6.5 | 1.5<br>1.5 | 8.0<br>8.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output disable time,<br>OEA to AOn | Waveform 4, 5 | 1.5<br>1.5 | 3.3<br>3.0 | 4.8<br>5.0 | 0.8<br>1.2 | 6.0<br>6.0 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, AOn Port<br>(10% to 90% or 90% to 10%) | Test Circuit and Waveforms | 1.5<br>1.5 | 2.2<br>2.4 | 3.0<br>3.0 | 1.5<br>1.5 | 3.5<br>3.5 | ns |
| $t_{SK}(o)$ | Output skew between receivers in same package[1] | Waveform 3 | | 0.4 | 1.0 | | 1.0 | ns |
| **SYMBOL** | **PARAMETER** | **TEST CONDITION** | **B PORT LIMITS** | | | | | **UNIT** |
| | | | $T_{amb}$ = +25°C, $V_{CC}$ = 5V, $C_D$ = 30pF, $R_U$ = 9Ω | | | $T_{amb}$ = -40 to +85°C, $V_{CC}$ = 5V±10%, $C_D$ = 30pF, $R_U$ = 9Ω | | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>AIn to $\overline{Bn}$ | Waveform 1, 2 | 2.4<br>1.5 | 3.7<br>2.7 | 4.9<br>4.4 | 1.9<br>1.5 | 5.9<br>5.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>OEB0 to $\overline{Bn}$ | Waveform 2 | 2.4<br>1.9 | 3.7<br>3.5 | 4.9<br>4.9 | 1.9<br>1.8 | 6.4<br>5.9 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>$\overline{OEB1}$ to $\overline{Bn}$ | Waveform 1 | 2.4<br>1.9 | 4.0<br>3.6 | 5.5<br>5.5 | 1.9<br>1.5 | 6.8<br>6.8 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, $\overline{Bn}$ Port<br>(1.3V to 1.8V) | Test Circuit and Waveforms | 1.0<br>0.5 | 1.4<br>1.1 | 3.0<br>3.0 | 1.0<br>0.5 | 3.0<br>3.0 | ns |
| $t_{SK}(o)$ | Output skew between drivers in same package[1] | Waveform 3 | | 0.3 | 1.0 | | 1.0 | ns |
| **SYMBOL** | **PARAMETER** | **TEST CONDITION** | **$R_U$ = 16.5Ω** | | | **$R_U$ = 16.5Ω** | | **UNIT** |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation delay,<br>AIn to $\overline{Bn}$ | Waveform 1, 2 | 2.5<br>1.6 | 3.8<br>2.8 | 5.0<br>4.5 | 2.0<br>1.6 | 6.0<br>5.1 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>OEB0 to $\overline{Bn}$ | Waveform 2 | 2.5<br>2.0 | 3.8<br>3.6 | 5.0<br>5.0 | 2.0<br>1.9 | 6.5<br>6.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Enable/disable time,<br>$\overline{OEB1}$ to $\overline{Bn}$ | Waveform 1 | 2.5<br>2.0 | 4.1<br>3.7 | 5.5<br>5.5 | 2.0<br>1.6 | 6.9<br>6.9 | ns |
| $t_{TLH}$<br>$t_{THL}$ | Transition time, $\overline{Bn}$ Port<br>(1.3V to 1.8V) | Test Circuit and Waveforms | 1.0<br>0.5 | 1.5<br>1.1 | 3.0<br>3.0 | 1.0<br>0.5 | 3.0<br>3.0 | ns |
| $t_{SK}(o)$ | Output skew between drivers in same package[1] | Waveform 3 | | 0.3 | 1.0 | | 1.0 | ns |

**NOTES:**
1. $|t_{PN}actual - t_{PM}actual|$ for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, $V_{CC}$, loading, etc.).

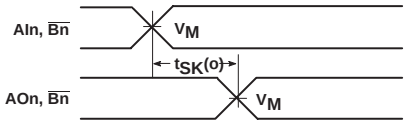
## AC WAVEFORMS



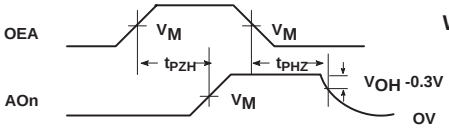

**Waveform 1. Propagation Delay for Data or Output Enable to Output**



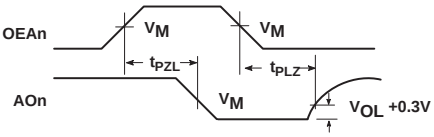

**Waveform 2. Propagation Delay for Data or Output Enable to Output**




**Waveform 3. Output Skews**




**Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

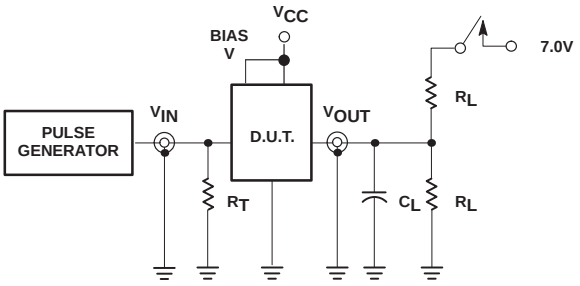



**Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

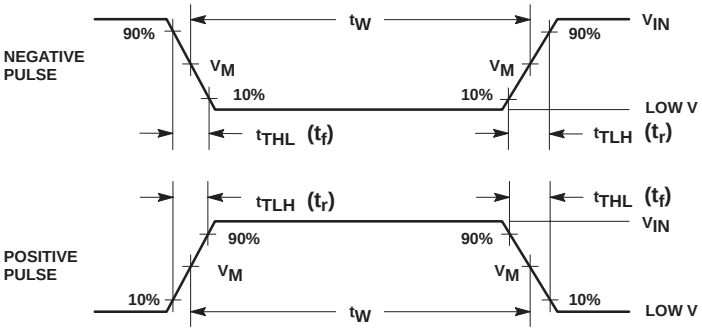
**NOTE:** $V_M$ = 1.55V for $\overline{Bn}$, $V_M$ = 1.5V for all others.

*SG00079*

## TEST CIRCUIT AND WAVEFORMS




**Test Circuit for 3-State Outputs on A Port**



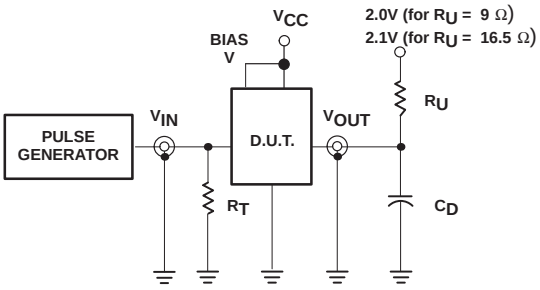

$V_M$ = 1.55V for $\overline{Bn}$, $V_M$ = 1.5V for all others.

**Input Pulse Definitions**

**SWITCH POSITION**

| TEST | SWITCH |
|---|---|
| $t_{PLZ}$, $t_{PZL}$ | closed |
| All other | open |

| Family FB+ | INPUT PULSE REQUIREMENTS | | | | | |
|---|---|---|---|---|---|---|
| | Amplitude | Low V | Rep. Rate | $t_W$ | $t_{TLH}$ | $t_{THL}$ |
| A Port | 3.0V | 0.0V | 1MHz | 500ns | 2.5ns | 2.5ns |
| B Port | 2.0V | 1.0V | 1MHz | 500ns | 2.5ns | 2.5ns |



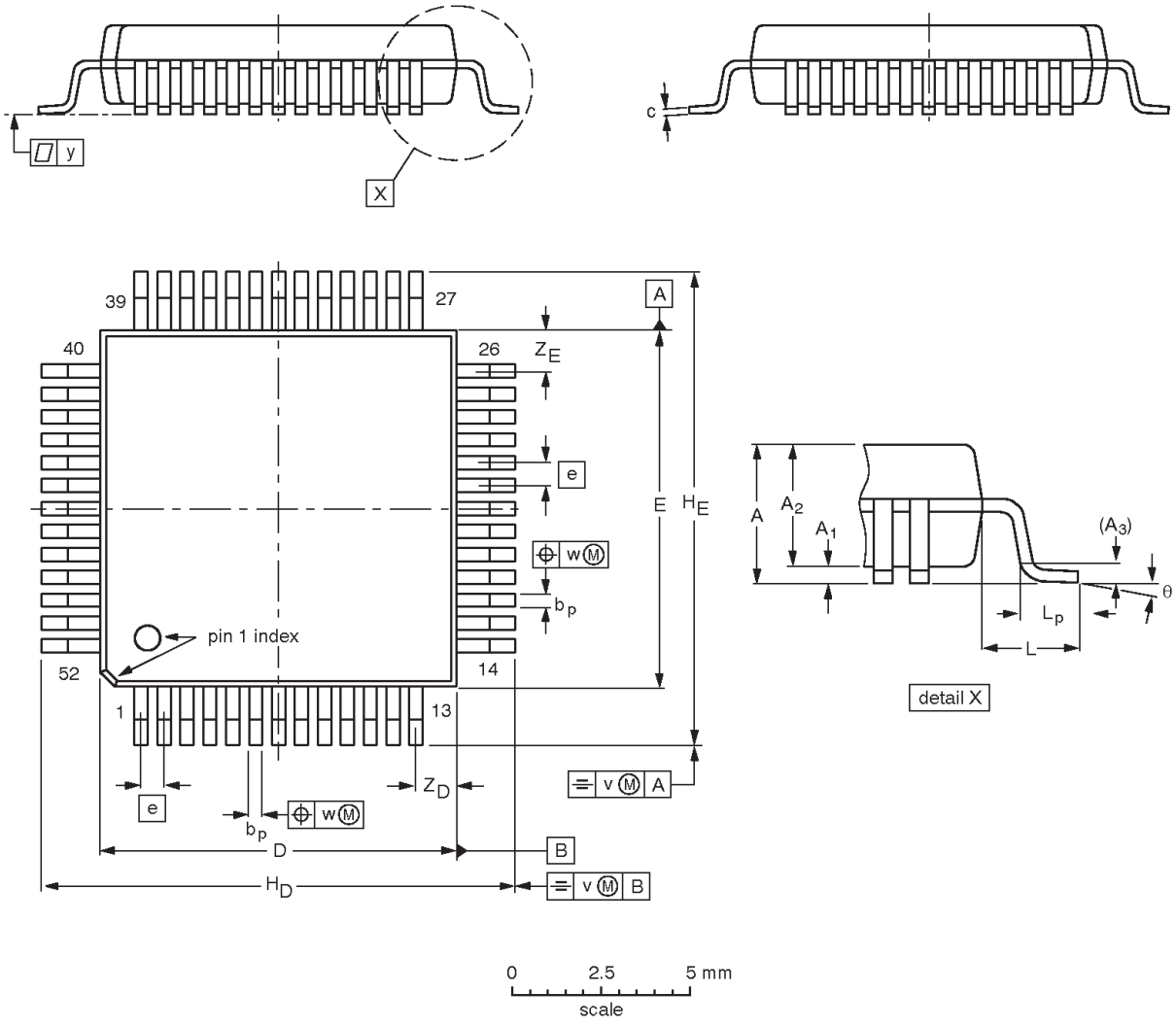

**Test Circuit for Outputs on B Port**

**DEFINITIONS:**

$R_L$ = Load Resistor; see AC CHARACTERISTICS for value.
$C_L$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.
$C_D$ = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
$R_U$ = Pull up resistor; see AC CHARACTERISTICS for value.

*SG00059*

**QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm SOT379-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.45 | 0.45<br>0.25 | 2.10<br>1.95 | 0.25 | 0.38<br>0.22 | 0.23<br>0.13 | 10.1<br>9.9 | 10.1<br>9.9 | 0.65 | 13.45<br>12.95 | 13.45<br>12.95 | 1.60 | 0.95<br>0.65 | 0.20 | 0.12 | 0.10 | 1.24<br>0.95 | 1.24<br>0.95 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT379-1 | | MO-108 | | | | ~~95-02-04~~<br>97-08-04 |

## Data sheet status

| Data sheet status | Product status | Definition [1] |
|---|---|---|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
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| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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