

PHD95N03LT

N-channel enhancement mode field-effect transistor

Rev. 01 — 18 July 2001

Product data

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™¹ technology.

Product availability:

PHD95N03LT in SOT428 (D-PAK).

2. Features

- Low on-state resistance
- Fast switching.

3. Applications

- High frequency computer motherboard DC to DC converters

4. Pinning information

Table 1: Pinning - SOT428, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p>Top view MBK091</p> <p>SOT428 (D-Pak)</p>	<p>MBB076</p>
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		

[1] It is not possible to make connection to pin 2 of the SOT428 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.



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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	–	25	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V	–	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C	–	115	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A	5	7	mΩ
		$V_{GS} = 5$ V; $I_D = 25$ A	7.5	9	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

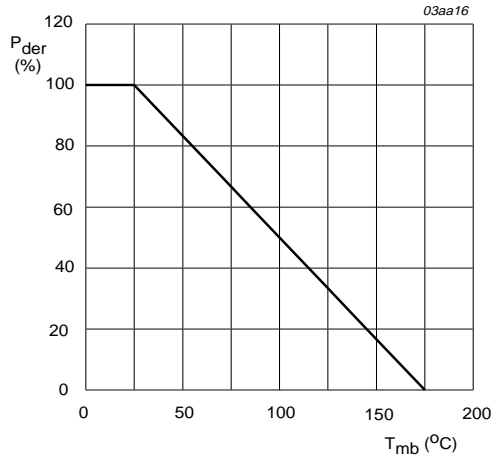
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 175 °C	–	25	V
V_{DGR}	drain-gate voltage (DC)	$T_j = 25$ to 175 °C; $R_{GS} = 20$ kΩ	–	25	V
V_{GS}	gate-source voltage (DC)		–	±15	V
V_{GSM}	gate-source voltage	$t_p \leq 50$ μs; pulsed; duty cycle 25 %; $T_j \leq 150$ °C	–	±20	V
I_D	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; Figure 2 and 3	–	75	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; Figure 2	–	61	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	240	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	115	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	240	A

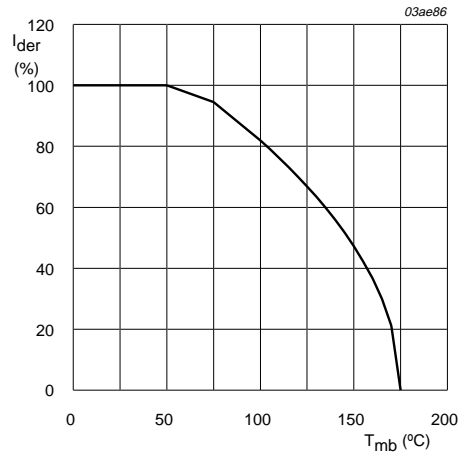
Avalanche ruggedness

E_{AS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 75$ A; $t_p = 0.1$ ms; $V_{DD} = 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C;	–	120	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; $V_{DD} = 15$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C	–	75	A



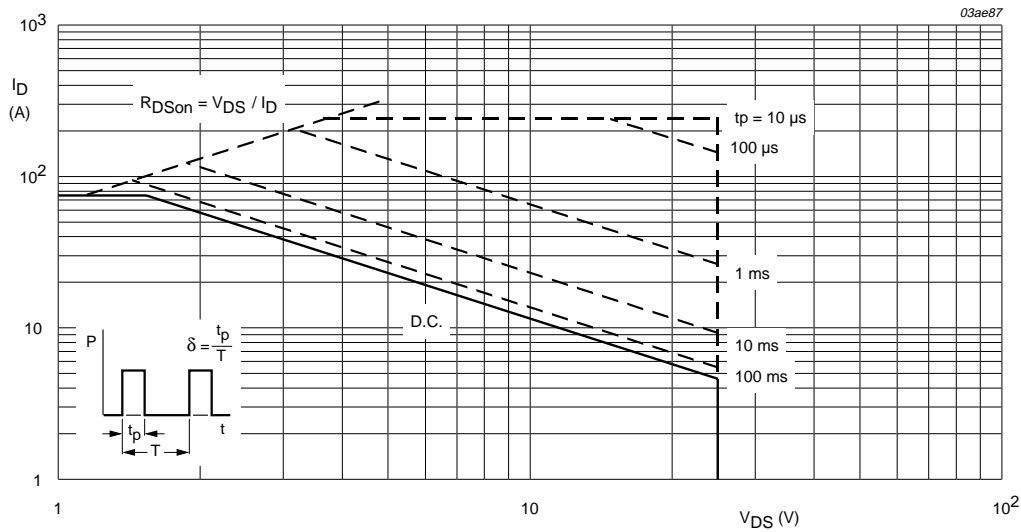
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	50	K/W

7.1 Transient thermal impedance

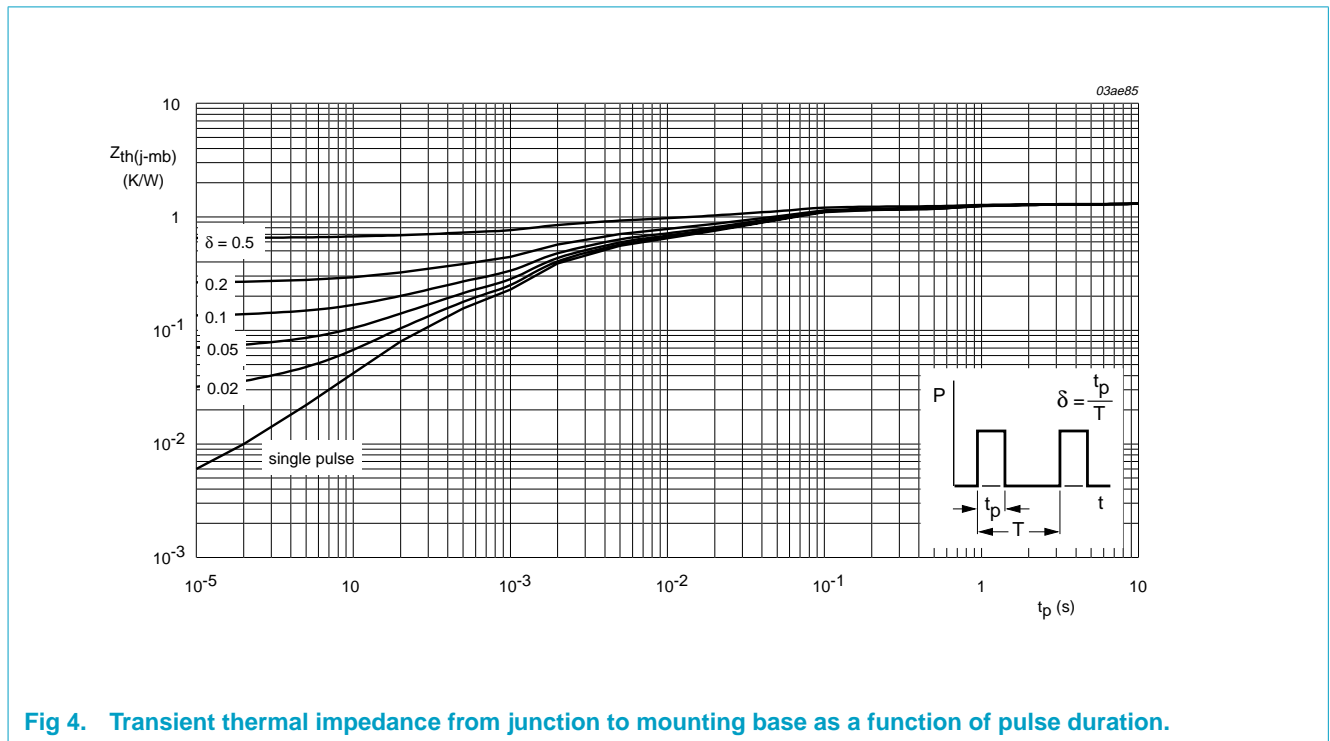
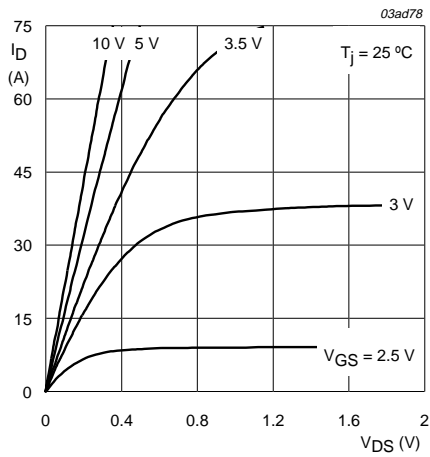


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

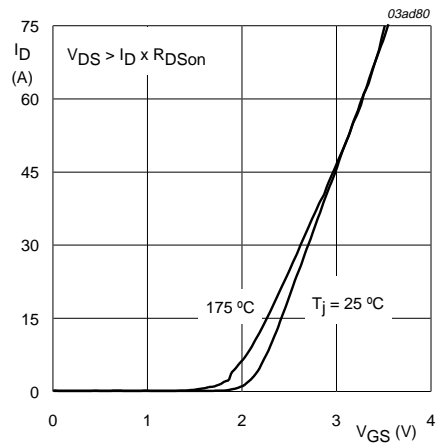
Table 5: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	25	–	–	V
		$T_j = -55\text{ °C}$	22	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	–	–	V
		$T_j = -55\text{ °C}$	–	–	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	–	0.05	10	μA
		$T_j = 175\text{ °C}$	–	–	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$	–	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	–	7.5	9	$\text{m}\Omega$
		$T_j = 175\text{ °C}$	–	13	15.5	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; Figure 7 and 8 $T_j = 25\text{ °C}$	–	5	7	$\text{m}\Omega$
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 50\text{ A}$	–	50	–	S
$Q_{g(tot)}$	total gate charge	$I_D = 50\text{ A}$; $V_{DD} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; Figure 13	–	43	–	nC
Q_{gs}	gate-source charge		–	12	–	nC
Q_{gd}	gate-drain (Miller) charge		–	16	–	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; Figure 11	–	2200	–	pF
C_{oss}	output capacitance		–	770	–	pF
C_{rss}	reverse transfer capacitance		–	500	–	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$; $I_D = 15\text{ A}$; $V_{GS} = 10\text{ V}$; $R_G = 6\text{ }\Omega$; resistive load	–	10	20	ns
t_r	turn-on rise time		–	30	50	ns
$t_{d(off)}$	turn-off delay time		–	110	140	ns
t_f	turn-off fall time		–	80	100	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	–	0.85	1.2	V
		$I_S = 40\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	–	0.9	–	V



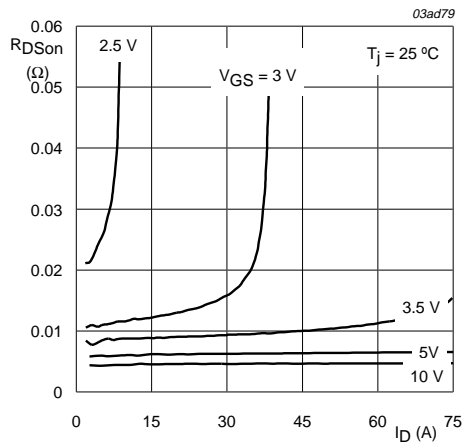
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



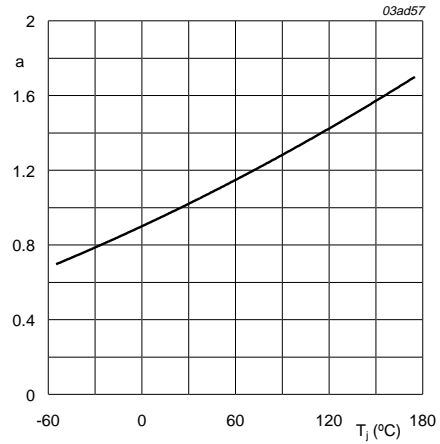
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} \geq I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



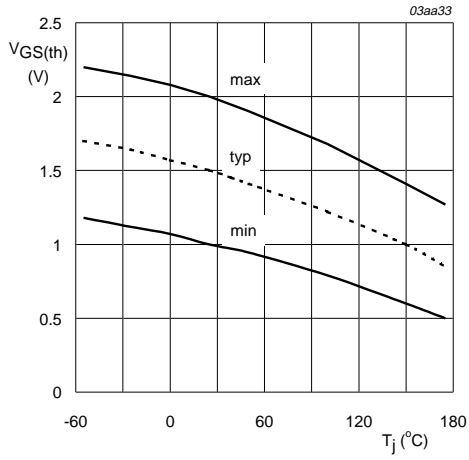
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



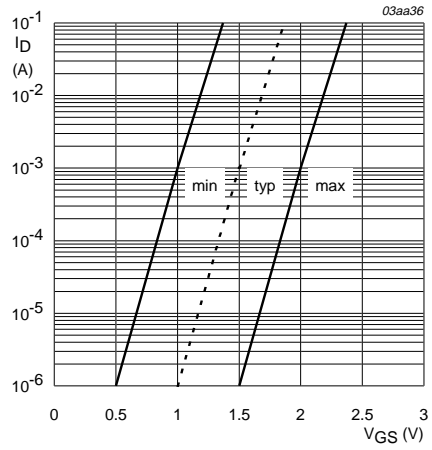
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



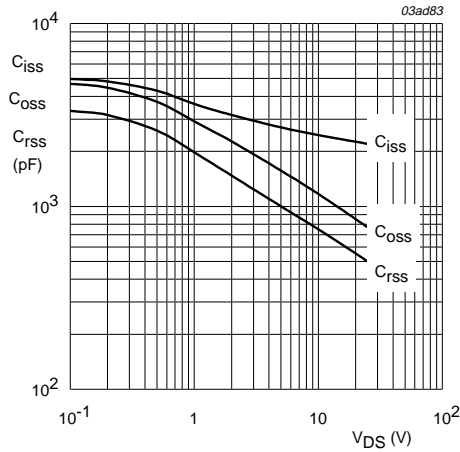
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



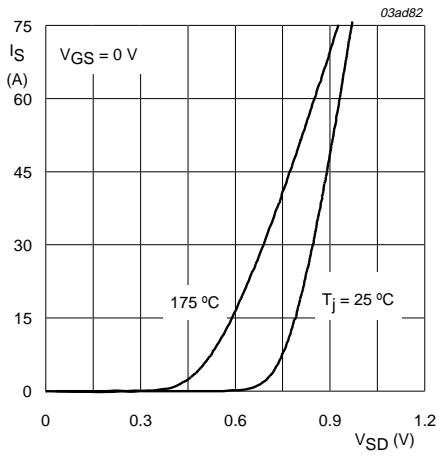
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



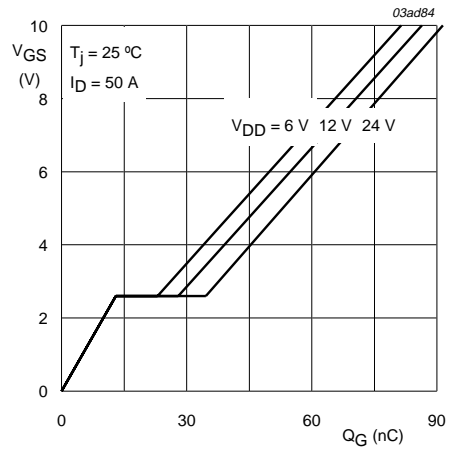
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25$ °C and 175 °C; $V_{GS} = 0$ V

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 50$ A; $V_{DD} = 24$ V, 12 V and 6 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads
(one lead cropped)

SOT428

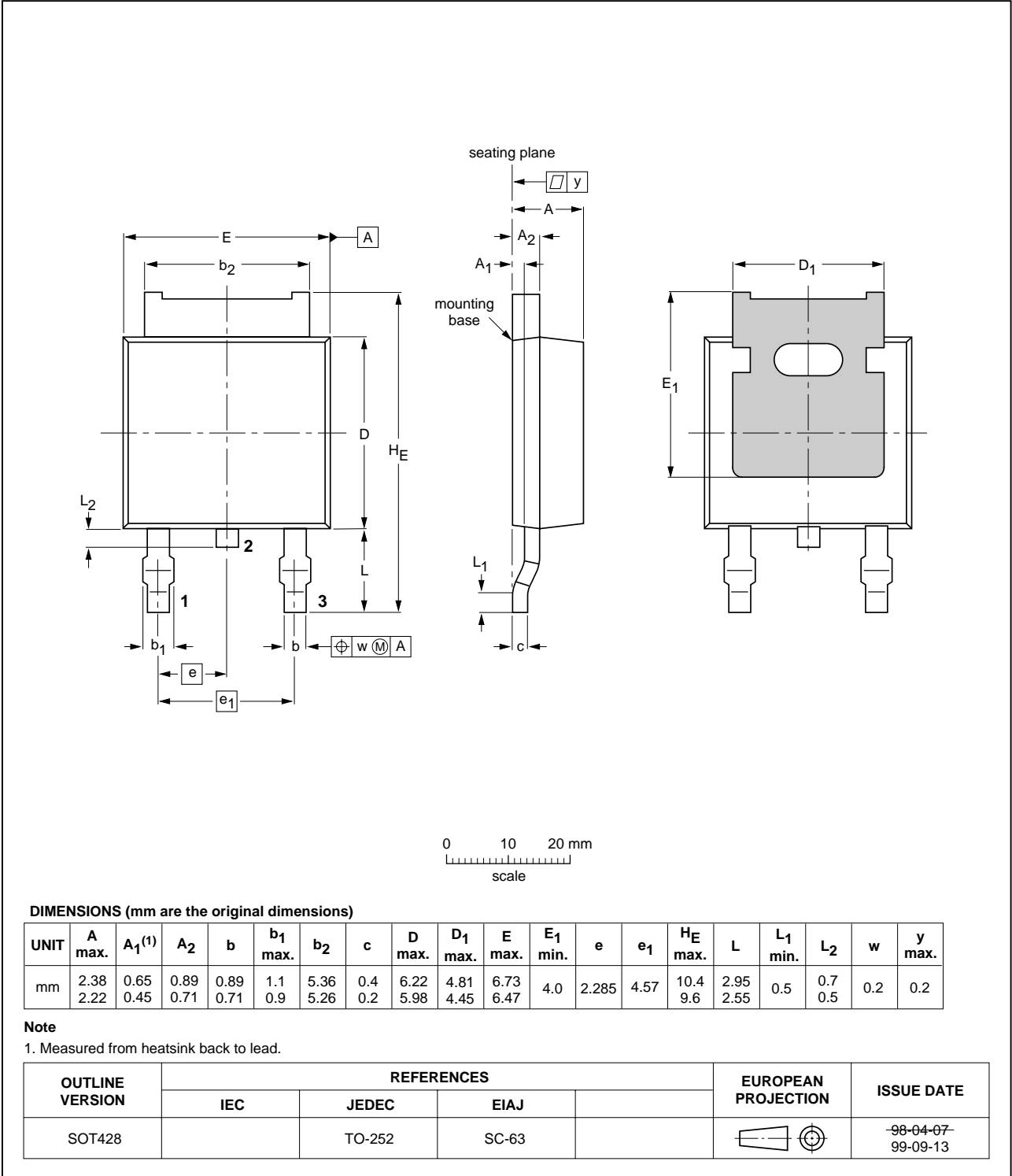


Fig 14. SOT428 (D-PAK).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010718	-	Product data; initial version

11. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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