

# PHP47NQ10T; PHB47NQ10T

N-channel enhancement mode field-effect transistor

Rev. 01 — 16 May 2001

Product data

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

PHP47NQ10T in SOT78 (TO-220AB)

PHB47NQ10T in SOT404 (D<sup>2</sup>-PAK).

## 2. Features

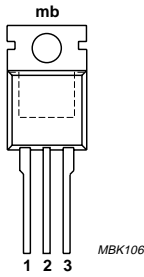
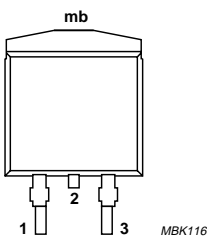
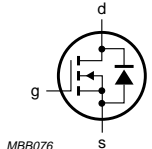
- Fast switching
- Very low on-state resistance.

## 3. Applications

- DC to DC converters
- Switched mode power supplies.

## 4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 SOT78 (TO-220AB)	 SOT404 (D <sup>2</sup> -PAK)
2	drain (d) <sup>[1]</sup>		
3	source (s)		
mb	mounting base; connected to drain (d)		
		 MBB076	

[1] It is not possible to make connection to pin 2 of the SOT404 package.

1. TrenchMOS is a trademark of Royal Philips Electronics.



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## 5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	100	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V	–	47	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C	–	166	W
$T_j$	junction temperature		–	175	°C
$R_{DSon}$	drain-source on-state resistance	$T_j = 25$ °C; $V_{GS} = 10$ V; $I_D = 25$ A	20	28	mΩ

## 6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

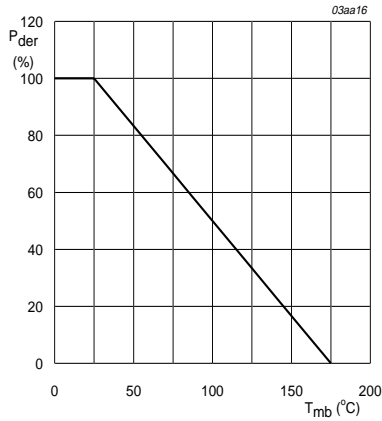
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $175$ °C	–	100	V
$V_{DGR}$	drain-gate voltage (DC)	$T_j = 25$ to $175$ °C; $R_{GS} = 20$ kΩ	–	100	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current (DC)	$T_{mb} = 25$ °C; $V_{GS} = 10$ V Figure 2 and 3	–	47	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V Figure 2	–	33	A
$I_{DM}$	peak drain current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	187	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; Figure 1	–	166	W
$T_{stg}$	storage temperature		–55	175	°C
$T_j$	operating junction temperature		–55	175	°C

### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{mb} = 25$ °C	–	47	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	187	A

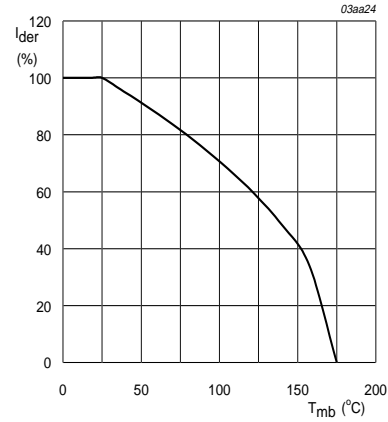
### Avalanche ruggedness

$E_{AS}$	non-repetitive avalanche energy	unclamped inductive load; $I_{AS} = 30$ A; $t_p = 0.1$ ms; $V_{DD} \leq 25$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; starting $T_j = 25$ °C; Figure 4	–	45	mJ
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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

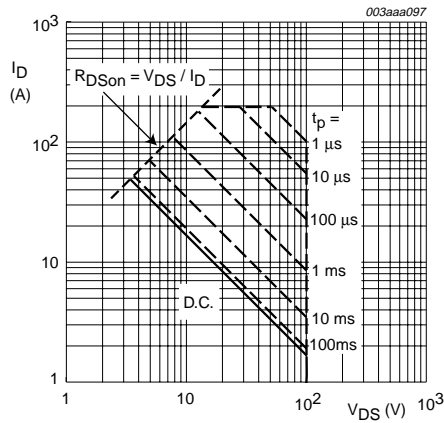
**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$$V_{GS} \geq 10 \text{ V}$$

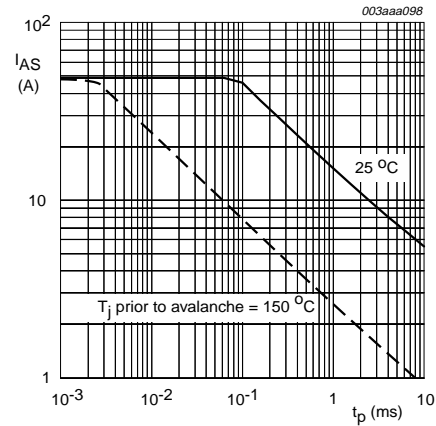
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of mounting base temperature.**



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**



Unclamped inductive load;  $V_{DD} \leq 25 \text{ V}$ ;  $R_{GS} = 50 \Omega$ ;  $V_{GS} = 5 \text{ V}$ ; starting  $T_j = 25^{\circ}C$  and  $150^{\circ}C$ .

**Fig 4. Non-repetitive avalanche ruggedness current as a function of pulse duration.**

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 5	0.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT78 package; vertical in still air.	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT404 package; mounted on printed circuit board; minimum footprint.	50	K/W

### 7.1 Transient thermal impedance

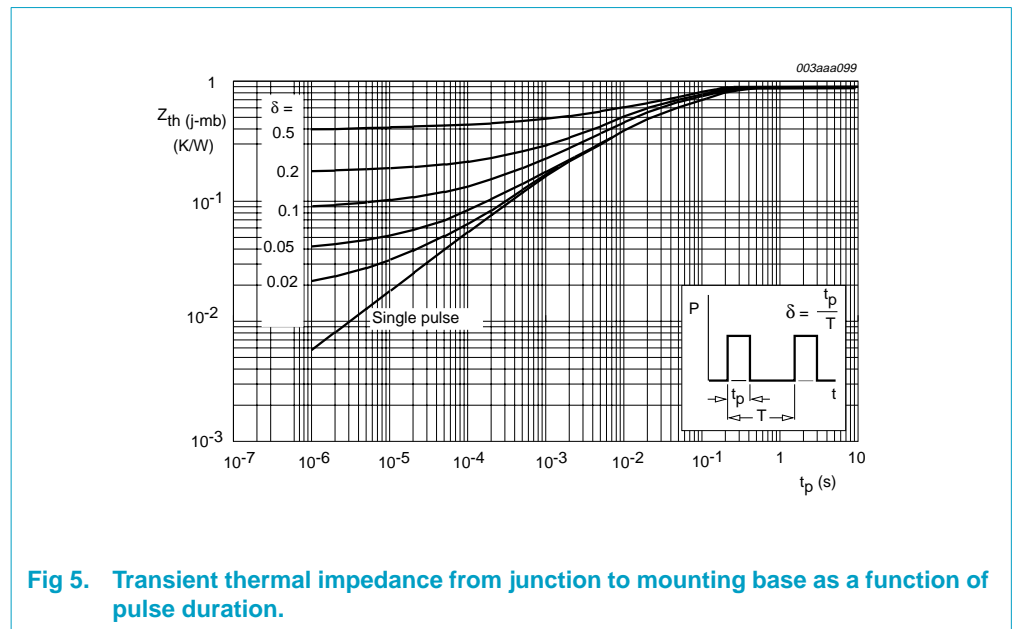
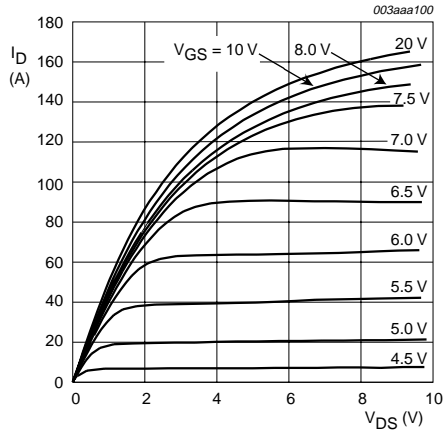


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 8. Characteristics

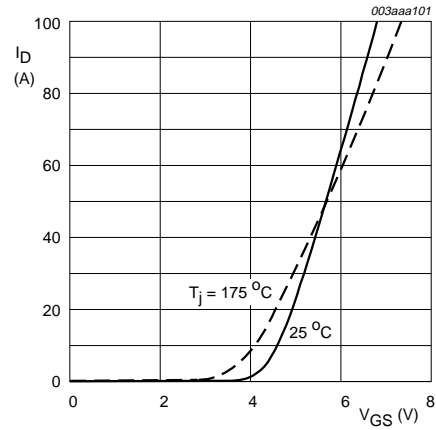
**Table 5: Characteristics**
 $T_j = 25\text{ °C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$	100	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; Figure 10				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 100\ \text{V}$				
		$T_j = 25\text{ °C}$	–	0.05	10	$\mu\text{A}$
		$T_j = 175\text{ °C}$	–	–	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{DS} = 0\ \text{V}$ ; $V_{GS} = \pm 20\ \text{V}$	–	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$ ; $I_D = 25\ \text{A}$ ; Figure 8 and 9				
		$T_j = 25\text{ °C}$	–	20	28	m $\Omega$
		$T_j = 175\text{ °C}$	–	–	76	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$I_D = 40\ \text{A}$ ; $V_{DD} = 80\ \text{V}$ ; $V_{GS} = 10\ \text{V}$ ; Figure 15	–	66	–	nC
$Q_{gs}$	gate-source charge		–	12	–	nC
$Q_{gd}$	gate-drain (Miller) charge		–	21	–	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\ \text{V}$ ; $V_{DS} = 25\ \text{V}$ ; $f = 1\ \text{MHz}$ ; Figure 13	–	2320	3100	pF
$C_{oss}$	output capacitance		–	315	378	pF
$C_{rss}$	reverse transfer capacitance		–	187	256	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\ \text{V}$ ; $R_D = 1.2\ \Omega$ ; $V_{GS} = 10\ \text{V}$ ; $R_G = 10\ \Omega$	–	15	23	ns
$t_r$	rise time		–	70	105	ns
$t_{d(off)}$	turn-off delay time		–	83	116	ns
$t_f$	fall time		–	45	63	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$ ; $V_{GS} = 0\ \text{V}$ ; Figure 14	–	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 47\ \text{A}$ ;	–	66	–	ns
$Q_r$	recovered charge	$dI_S/dt = -100\ \text{A}/\mu\text{s}$ ; $V_{GS} = -10\ \text{V}$ ; $V_R = 30\ \text{V}$	–	0.24	–	$\mu\text{C}$



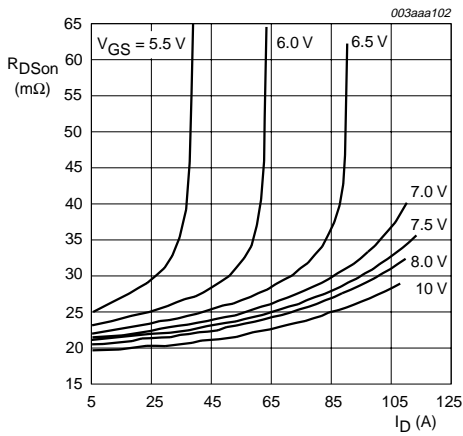
$T_j = 25\text{ }^\circ\text{C}$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values.**



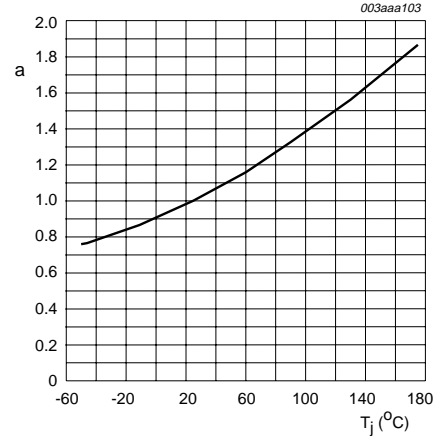
$T_j = 25\text{ }^\circ\text{C}$  and 175  $^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



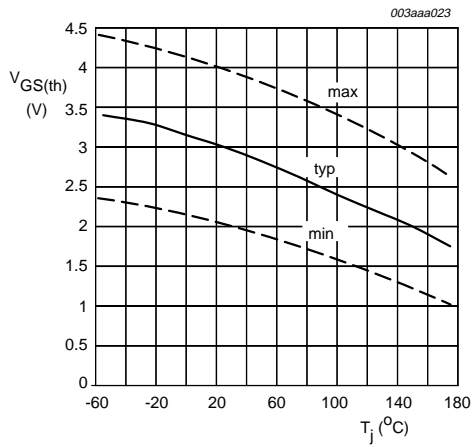
$T_j = 25\text{ }^\circ\text{C}$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values.**



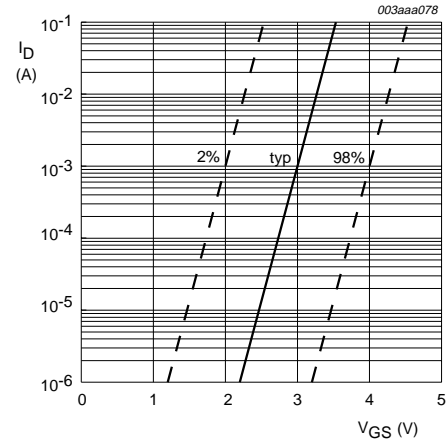
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature.**



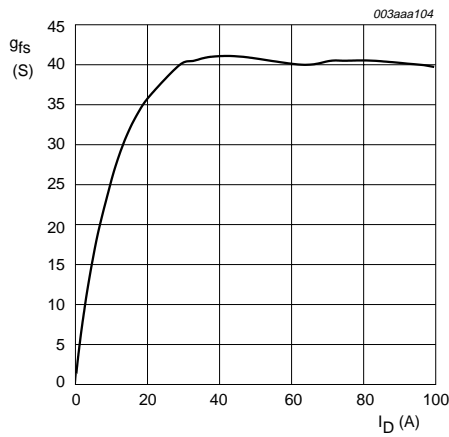
$I_D = 1 \text{ mA}$ ;  $V_{DS} = V_{GS}$

**Fig 10. Gate-source threshold voltage as a function of junction temperature.**



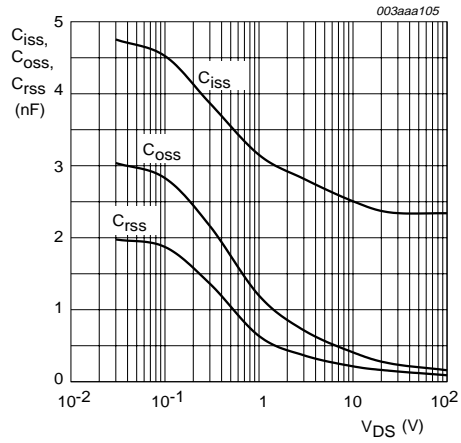
$T_j = 25 \text{ }^{\circ}C$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage.**



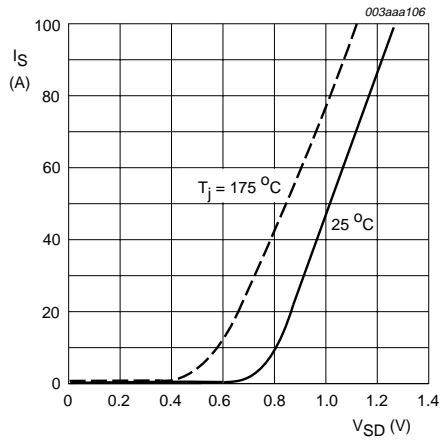
$T_j = 25 \text{ }^{\circ}C$ ;  $V_{DS} = 25 \text{ V}$

**Fig 12. Forward transconductance as a function of drain current; typical values.**



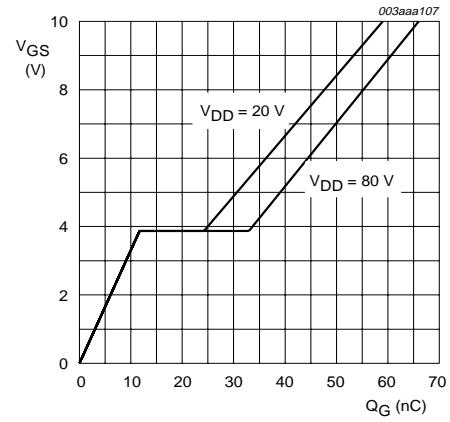
$V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 40\text{ A}$ ;  $V_{DD} = 20\text{ V}$  and  $80\text{ V}$

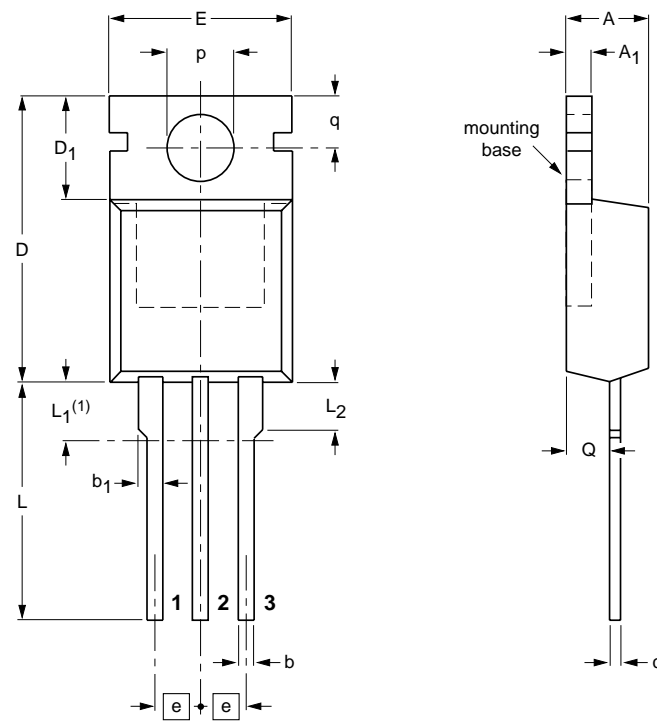
**Fig 15. Gate-source voltage as a function of gate charge; typical values.**



## 9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> <sup>(1)</sup>	L <sub>2</sub> max.	p	q	Q
mm	4.5	1.39	0.9	1.3	0.7	15.8	6.4	10.3	2.54	15.0	3.30	3.0	3.8	3.0	2.6
	4.1	1.27	0.7	1.0	0.4	15.2	5.9	9.7		13.5	2.79		3.6	2.7	2.2

**Note**

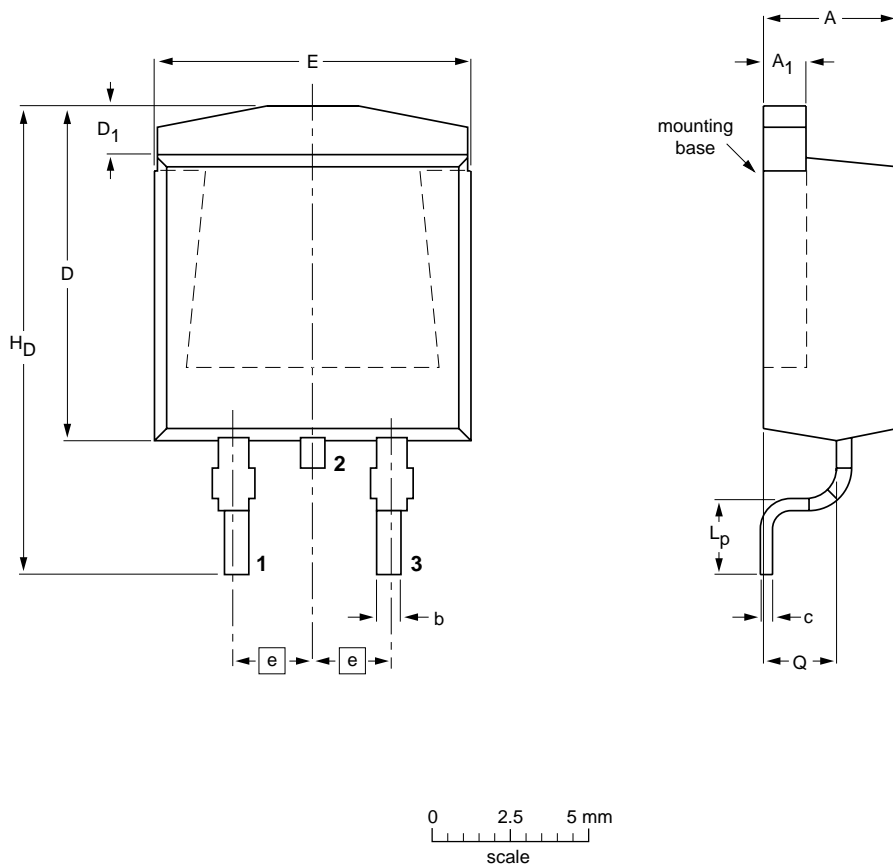
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			00-09-07- 01-02-16

Fig 16. SOT78 (TO-220AB)

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D max.	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						99-06-25 01-02-12

Fig 17. SOT404 (D<sup>2</sup>-PAK).

## 10. Revision history

Table 6: Revision history

Rev	Date	PCPN	Description
01	20010516	-	Product data. Initial version.

## 11. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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