DATA SHEET

TZA1000
QIC read-write amplifier

Preliminary specification
Supersedes data of 1998 Mar 11
File under Integrated Circuits, IC01

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Philips
Semiconductors

PHILIPS

QIC read-write amplifier TZA1000

FEATURES

- 3-wire serial interface for programming
- On-chip Digital-to-Analog Converters (DAC) for:
  - MR (Magneto Resistive) sense bias current
  - MR DC bias current
  - Write current
- Low noise differential input stage: typically 0.65 nV/√Hz (Z_i = 0 Ω)
- Magnetic feedback circuit to handle large output signals
- MR DC bias current circuit
- Very fast write current rise and fall times with near rail-to-rail voltage swing
- Maximum write current of 100 mA: ready for high coercivity tape
- Low noise read amplifier for reading track height servo signals with the write coil
- Very few external components required
- On board registers for easy format or bit rate selection
- Fast read-after-write recovery time
- Test circuit for yoke-type heads
- Switchable differentiator for yoke-type heads, with programmable cut-off frequencies
- Anti-aliasing low-pass filter, with programmable cut-off frequencies
- AGC (Automatic Gain Control) options: internally (digitally) controlled, externally controlled or fixed gain
- Hold input for fast AGC freeze
- Input for fast reader/writer (track height servo) signal selection
- Power fail detection on both 5 and 12 V lines (status can be read from the read register)
- Write unsafe detection
- Provides an accurate reference voltage (for AD conversion)
- Very simple interconnection with the SZA1000 QIC digital equalizer
- +5 V ±10% and +12 V ±10% supply voltages
- Low power standby, active and test modes.

RELATED DOCUMENTS

- SZA1000 QIC digital equalizer data sheet
- Application notes for TZA1000 and SZA1000.

Both are available from Philips Semiconductors.

GENERAL DESCRIPTION

The TZA1000 is a single-chip read-write amplifier for single-channel QIC (Quarter Inch Cartridge) systems with MR heads. It can be used with both SIG (Sensor in Gap)- and yoke-type MR heads and is designed to be used in conjunction with the Philips SZA1000 digital equalizer IC (although it can also function as a stand alone unit). This combination is flexible enough to be used with all popular tape backup formats including QIC 80, QIC 3010, QIC 3020, QIC 3080, QIC 5010, Travan 1, Travan 2, Travan 3 and Travan 4 and to be forward compatible with their single channel successors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	read circuit supply voltage		4.5	5	5.5	V
V_{DD2}	FB and write circuit supply voltage		4.5	5	5.5	V
V_{DD3}	sense current circuit supply voltage		10.8	12	13.2	V
I_{DD1}; I_{DD2}	read/FB and write circuit supply current					
	Read mode		–	69	–	mA
	Write mode	I_{write} = 30 mA	–	105	–	mA
I_{DD3}	sense current circuit supply current	I_{sense} = 16 mA	15.0	16.2	19.0	mA
$V_{n(i)(eq)}$	equivalent input noise voltage	Z_{source} = 0 Ω	–	0.65	0.8	nV/√Hz
f_{clk}	clock frequency		–	–	24	MHz
T_{amb}	recommended operating temperature		0	–	70	°C
T_j	recommended junction temperature		0	–	125	°C
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	–	66	–	K/W

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA1000	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

BLOCK DIAGRAM

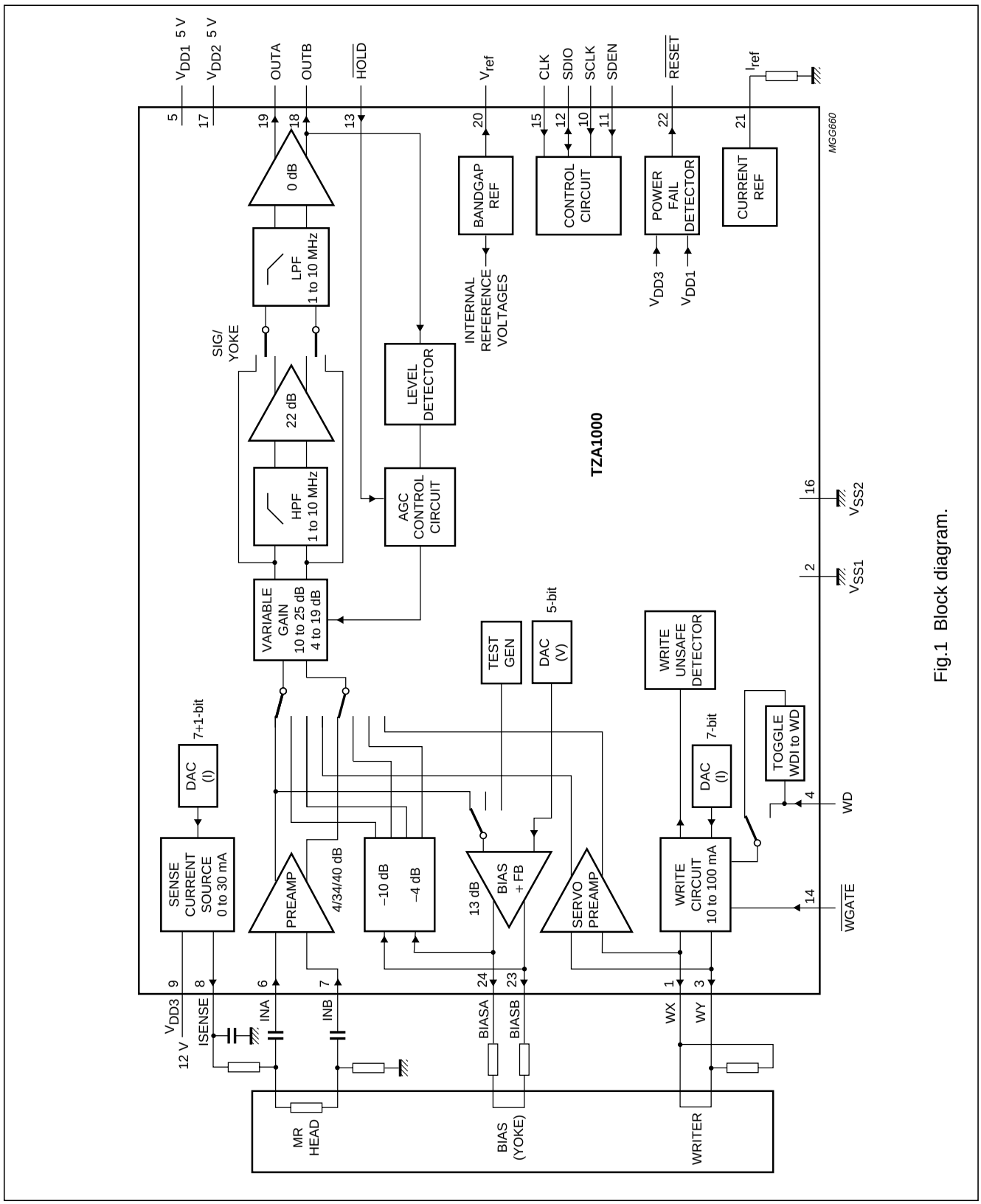


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE(1)
WX	1	write current to head	O
V_{SS1}	2	large signal ground	P
WY	3	write current to head	O
WD	4	write data	I(2)
V_{DD1}	5	large signal +5 V	P
INA	6	read signal from MR	I
INB	7	read signal from MR	I
ISENSE	8	sense current for MR	O
V_{DD3}	9	+12 V for sense current supply	P
SCLK	10	serial interface clock	I(2)
SDEN	11	serial interface enable	I(2)
SDIO	12	serial interface data I/O	I/O
$\overline{HOLD}$	13	hold AGC; active LOW	I(2)
$\overline{WGATE}$	14	write gate; active LOW	I(2)
CLK	15	clock input	I(2)
V_{SS2}	16	small signal ground	P
V_{DD2}	17	small signal +5 V	P
OUTB	18	output to equalizer	O
OUTA	19	output to equalizer	O
V_{ref}	20	2 V reference output	O
I_{ref}	21	current reference resistor	note 3
$\overline{RESET}$	22	reset for microcontroller; active LOW	O
BIASB	23	bias current for yoke heads	O
BIASA	24	bias current for yoke heads	O

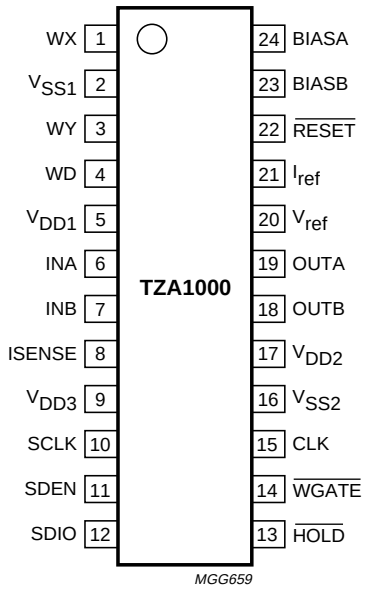


Fig.2 Pin configuration.

Notes

1. Pin type abbreviations: O = output, I = input, P = power supply.
2. Digital inputs: LOW: $<0.3V_{DD}$; HIGH: $>0.7V_{DD}$.
3. Use only for connecting current reference resistor.

See Chapter “Equivalent pin circuits” for the I/O configuration of the analog pins.

FUNCTIONAL DESCRIPTION

The preamplifier

The gain and dynamic range of the symmetrical low noise preamplifier can be varied to accommodate a wide variation in input signal amplitude (see Table 11). The 40 dB and 34 dB gain settings are provided for normal use. The 40 dB setting offers the lowest noise figure. The 4 dB gain setting is intended for IC testing only.

The servo preamplifier

This low noise preamplifier can be used for reading signals, such as QIC 3095 (Travan 4) servo signals, via the recording head write coil. Servo mode is selected either by resetting bits AI0 and AI1 in the control register (see Table 9) or by means of the $\overline{\text{HOLD}}$ pin (the HSM control bit must be set when $\overline{\text{HOLD}}$ goes LOW; see Table 7). When servo mode is selected, the maximum total gain is set automatically regardless of, and without overwriting, gain settings. Fast switch-over from read mode to servo mode can thus be achieved without having to alter register values.

Variable gain stage and AGC

The input to the variable gain stage can be switched to the preamplifier output, to the output of the bias/FB (Feed Back) circuit, or to the servo preamplifier output. When using magnetic feedback, the bias/FB circuit output should be selected (see Table 9).

The AGC range is 15 dB. The gain is programmable in 1 dB steps (see Table 12). If the output signal is too small, a digital control circuit will increase the gain from minimum to maximum in approximately 10 ms. If the output signal is too large, the gain will be reduced from maximum to minimum in approximately 0.2 ms. These values assume a 24 MHz clock frequency. The upper limit of the gain control range can be extended by 6 dB by setting the G6DB bit in the control register via the serial interface (see Table 13).

The AGC is frozen while the $\overline{\text{HOLD}}$ input is LOW, the TZA1000 is writing, or the IC is in servo mode.

The AGC can be operated internally, running on the CLK clock signal on pin 15 ($\overline{\text{HOLD}}$ HIGH and GFXD LOW; see Table 12), or externally by means of a software algorithm (GFXD HIGH). When operated externally, either the DN bit in the status read register (see Table 17) or the level measurement in the digital equalizer IC (SZA1000) can be used as input to the algorithm.

The AGC will maintain outputs OUTA and OUTB at 1.1 V (p-p). Additional level adjustment points are provided by the 34 or 40 dB preamplifier gain switch (see Table 11) and the −10 or −4 dB bias output attenuation switch (see Table 9).

High-pass filter

The HPF (High-Pass Filter) is used to differentiate yoke-type head signals. It is followed by an additional gain stage (21 dB). The HPF cut-off frequency is coupled to the cut-off frequency of the LPF (Low-Pass Filter), and is selectable in 4 steps: 1, 2, 4 and 10 MHz (see Table 2). The HPF can be bypassed for SIG heads (see Table 8).

Low-pass filter

The second order low-pass filter is used to attenuate high frequency noise above the signal bandwidth, mainly to provide anti-aliasing filtering for the A/D converter in the digital equalizer. The cut-off frequency of the LPF is selectable in 4 steps: 1, 2, 4 and 10 MHz (see Table 2).

Sense current circuit

The sense current circuit is a programmable current source, operating from the 12 V supply (V_{DD3}). It can be programmed to supply a current between 0 and 15 mA, with 7-bit resolution. The current range can be doubled, then ranging from 0 to 30 mA, by setting the SDB bit in the control register (see Table 15). The sense current circuit can be disabled by resetting the ENS bit (see Table 4).

This is the only circuit on the IC that uses the 12 V supply. The output must be decoupled with a low impedance capacitor (10 μF recommended) to reduce noise coupling into the head.

For the current source circuit to operate correctly, the voltage difference between V_{DD3} (pin 9) and ISENSE (pin 8) must be at least 1.6 V.

Bias and magnetic feedback circuit

This circuit can be used to generate AC and DC bias currents (for a yoke-type MR head, for instance). The DC bias output voltage is programmable between 0 and 1.4 V, with 5-bit resolution (see Table 3). The DC current generated is this voltage divided by the total bias resistance (head coil + total series resistance).

The AC signal input to the circuit can be switched to the preamplifier output (see Table 10). In this way, magnetic feedback inside the head can be achieved. This limits head distortion, and prevents head saturation from large tape signals, like QIC 80 recordings.

The open loop gain of the feedback loop depends on head sensitivity, the selected sense current (see Table 15), and the selected preamplifier gain (see Table 11). The values of the external resistors connected in series with the bias conductor can be used to set the gain. For loop stability at high frequencies, the bandwidth of the magnetic feedback amplifier is limited to 5 MHz.

In closed loop mode, the effective cut-off frequency for the playback signals will increase with the feedback factor. For this reason the read signal can be taken from the output of the bias circuit.

To prevent loop instability at low frequencies, the preamplifier input capacitors should be chosen such that the cut-off frequency at that point is well above, or well below, the internal cut-off frequency of the AC coupling between the preamplifier and the bias circuit (input impedance of the preamplifier is typically 2 kΩ).

The maximum (peak AC) current that the bias circuit can deliver can be adjusted to achieve an optimum balance between required current range and power consumption (see Table 3). The AC circuit is switched off when the TZA1000 is writing, and the maximum current is switched to 10 mA. This limits power dissipation during writing.

Test generator

This circuit generates a test signal with a frequency $\frac{1}{16}$ that of the signal at the CLK input (pin 15). By switching the AC input of the bias circuit to the internal test generator (see Table 10), the read channel can be tested. The differential output value is typically 100 mV (p-p).

This facility can also be used to adjust the DC bias voltage while monitoring the signal at the read element in the head. The optimum DC bias level setting is just before the output from the read head reaches its peak.

Write circuit

The write circuit is a differential current source that can generate a near rail-to-rail output voltage to get the shortest current transition time. Writing is enabled when $\overline{\text{WGATE}}$ is LOW. The polarity of the current depends on the WD input pin. The WDM bit in the control register determines the write signal mode: WD (Non-Return to Zero) or WDI (Return to Zero; see Table 14). When WDI mode is selected, the polarity of the write current is reversed at every falling edge of the WD input. When WD mode is selected, the polarity of the write current is reversed when the polarity of WD changes. The write current is programmable between 0 and 125 mA, with 7-bit resolution (see Table 14).

The IC is specified for a write current of up to 100 mA. Overshoot caused by an inductive load can be minimized by means of a single external resister local to the IC.

Write unsafe detector

The write unsafe detector will detect an open write coil, or one shorted to ground. The circuit is enabled only while the TZA1000 is writing. A resistance to GND or V_{DD} of less than 10 Ω, or a series resistance greater that about 300 Ω, will be detected (these values are write-current dependant). If an error occurs, the WUS status bit is set. This bit can be read via the serial interface. The WUS bit will remain set until the status byte is read.

Power fail detector

The power fail detector will detect a low voltage on the 5 V (V_{DD1}) or 12 V (V_{DD3}) supply lines. The thresholds are 3.75 V for V_{DD1} and 9 V for V_{DD3}. A power failure is detected if the voltage is below the threshold for 1 µs or longer. If a 5 V power failure occurs, the status bit PF5 is set. If a 12 V power failure occurs, the status bit PF12 is set. These bits can be read via the serial interface, and will remain HIGH until the status byte is read.

When a 5 V power failure occurs, the $\overline{\text{RESET}}$ output goes LOW and the write circuit is disabled (in addition to PF5 being set). The $\overline{\text{RESET}}$ output has an internal 18 kΩ pull down resistor to guarantee a LOW level at the output even when a power failure occurs. During normal operation, the $\overline{\text{RESET}}$ pin should not be held LOW by an external circuit, since this will switch the IC into test mode.

DACs

There are 3 internal DACs:

1. The Sense DAC: current DAC; 7-bit resolution
2. The Write DAC: current DAC; 7-bit resolution
3. The Bias DAC: voltage DAC; 5-bit resolution.

The Sense and Write DAC current settings are a function of the reference current I_{ref} (at the I_{ref} pin). I_{ref} is multiplied by a 7-bit factor: S0 to S6 for the sense DAC, W0 to W6 for the write DAC (see Tables 14 and 15). If the resistance between I_{ref} and GND is increased (or decreased), the DAC output currents will be decreased (or increased) by the same factor. In this way, the DAC output current ranges can be adjusted.

The current values specified, and the equations used to calculate Sense and Write currents (see Tables 14 and 15), are for a 430 Ω resistance between I_{ref} and GND. This resistance can be varied between 250 Ω and 1 kΩ, giving a $\pm 2 \times$ DAC modification range. For reasons of noise and stability, the voltage at the I_{ref} pin should not be used in any other part of the circuit.

Clock handling

The TZA1000 has 2 clock inputs:

CLK: the general clock input, pin 15

SCLK: the serial interface clock input, pin 10.

CLK is used for status register read and write cycle timing and for operating the internal AGC. When the AGC is not being used and serial communications are not active, CLK may be switched off. This can help reduce crosstalk on the printed circuit board.

When accessing the status register, the CLK frequency must be at least $16 \times$ SCLK frequency. It is recommended that the 24 MHz clock supplied by the SZA1000 be used directly.

Serial interface

The 3 wire serial interface recognizes 8-bit addresses and 8-bit data. To read data from the status register, hex address FF must be transmitted. The IC will then respond with the contents of the 8-bit status register.

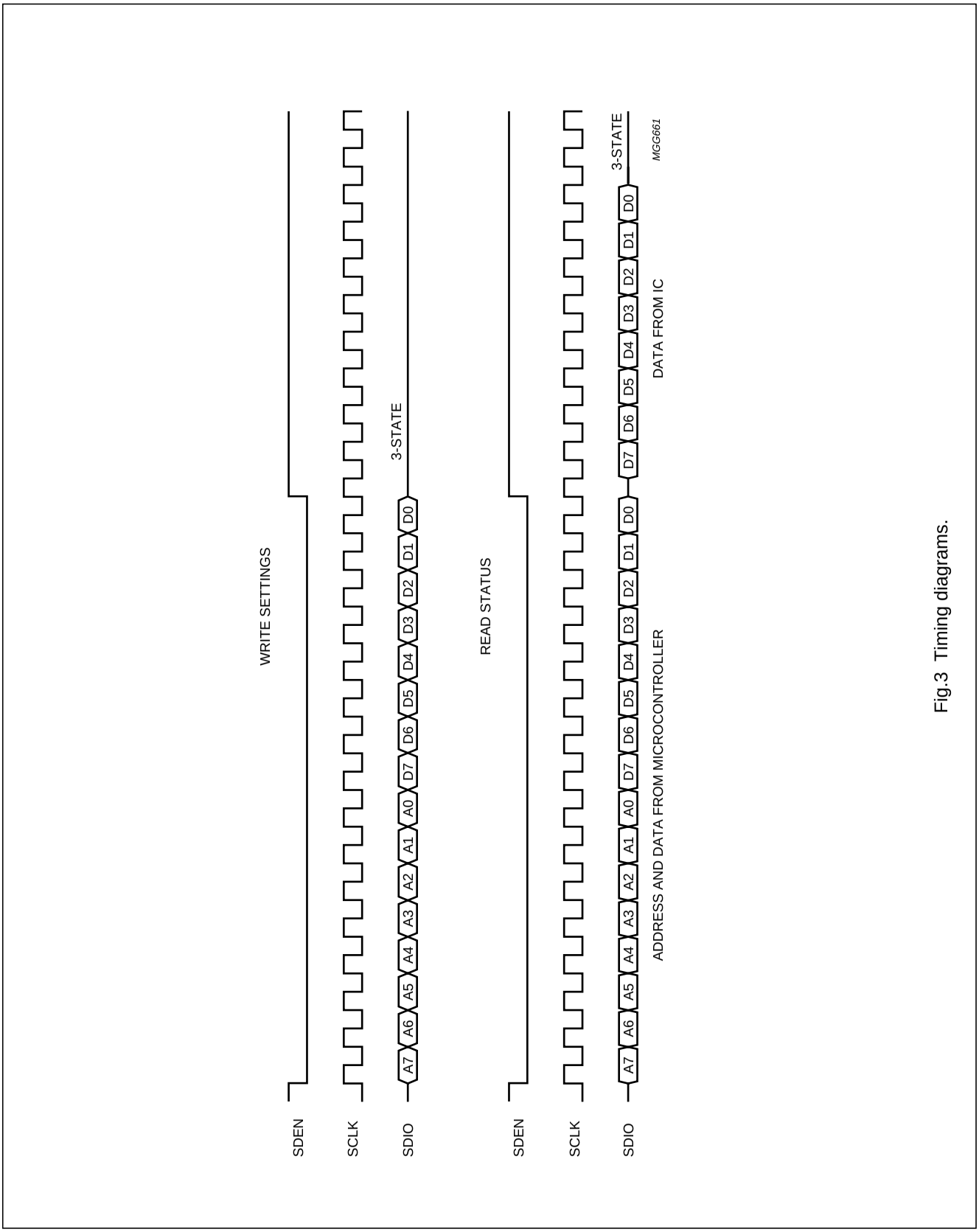


Fig.3 Timing diagrams.

CONTROL REGISTER

The control register contains six 8-bit entries configured as shown in Table 1.

Table 1 Control register settings

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
0	–	FC1	FC0	ENFB1	ENFB0	ENS	ENRD	ENREF
1	HSM	DIFF	AI1	AI0	FBI1	FBI0	PG1	PG0
2	–	–	G6DB	GFXD	G3	G2	G1	G0
3	–	–	–	B4	B3	B2	B1	B0
4	WDM	W6	W5	W4	W3	W2	W1	W0
5	SDB	S6	S5	S4	S3	S2	S1	S0

Control bits

Control bit functions are detailed in Tables 2 to 17.

Table 2 HPF and LPF cut-off frequency

FC1	FC0	FREQUENCY
0	0	1 MHz
0	1	2 MHz
1	0	4 MHz
1	1	10 MHz

Table 3 Bias current settings; note 1

ENFB1	ENFB0	BIAS CIRCUIT	$I_{bias(min)}$	$I_{bias(max)}$
0	0	off	0	0
0	1	on	–10 mA	+10 mA
1	0	on	0	+10 mA
1	1	on	–10 mA	+20 mA

Note

1. Control bits B0 to B4 make up a 5-bit number between 0 and 31. The DC bias voltage between BIASA and BIASB (pins 23 and 24) is B $\times$ 45 mV. BIASA is positive with respect to BIASB.

Table 4 Sense current circuit

ENS	SENSE CURRENT CIRCUIT
0	disabled
1	enabled

Table 5 Read circuits (excluding preamplifiers)

ENRD	READ CIRCUITS
0	disabled
1	enabled

Table 6 Internal reference voltages

ENREF	INTERNAL REF. VOLTAGES
0	disabled
1	enabled

Table 7 $\overline{\text{HOLD}}$ pin function

HSM	FUNCTION
0	AGC hold on or off
1	select servo or data preamplifier

Table 8 HPF circuit

DIFF	HPF CIRCUIT
0	bypassed
1	on

Table 9 Variable gain circuit input select

HSM	$\overline{\text{HOLD}}$	AI1	AI0	INPUT
0	X	0	0	servo preamplifier
0	X	0	1	preamplifier
0	X	1	0	bias output –10 dB
0	X	1	1	bias output –4 dB
1	1	0	0	servo preamplifier
1	1	0	1	preamplifier
1	1	1	0	bias output –10 dB
1	1	1	1	bias output –4 dB
1	0	X	X	servo preamplifier

Table 10 Bias circuit input

FBI1	FBI0	INPUT
0	0	no signal
0	1	preamplifier
1	0	test generator
1	1	preamplifier

Table 11 Preamplifier gain

PG1	PG0	GAIN
0	0	0
0	1	34 dB
1	0	4 dB
1	1	40 dB

Table 12 AGC setting

HSM	$\overline{\text{HOLD}}$	GFXD	AGC
0	1	0	on
0	0	0	frozen at last value
1	1	0	on
1	0	0	no AGC at servo mode: maximum gain
X	X	1	off, gain set by G0 to G3; note 1

Note

1. Control bits G0 to G3 make up a 4-bit number used to program the gain in 1 dB steps (from 4 to 19 dB if G6DB is 0, from 10 to 25 dB if G6DB is 1; see Table 13).

Table 13 Variable gain circuit range select

G6DB	RANGE
0	4 to 19 dB
1	10 to 25 dB

Table 14 Write mode select; note 1

WDM	EXPECTED INPUT SIGNAL	FUNCTION
0	WDI	on
1	WD	bypassed

Note

1. Control bits W0 to W6 make up a 7-bit number between 0 and 127. Write current is $\frac{125 \times (W + 1)}{128}$ mA (R_{ref} = 430 Ω).

Table 15 Sense current range select; note 1

SDB	CURRENT
0	0 to 15 mA
1	0 to 30 mA

Note

1. Control bits S0 to S6 make up a 7-bit number between 0 and 127. Sense current is $\frac{15 \times (S + 1)}{128}$ mA when SDB = 0 and $\frac{30 \times (S + 1)}{128}$ mA when SDB = 1 (R_{ref} = 430 Ω).

Status

A status byte, located at address FF, contains the following status bits:

Table 16 Status byte settings

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
FF	AG3[1]	AG2[1]	AG1[1]	AG0[1]	DN[2]	PF5[3]	WUS[4]	PF12[5]

Notes

1. Actual gain. Allows the gain to be determined while the AGC is on.
2. This bit can be used for microcontroller gain control, with the AGC off (see Table 17).
3. Power failure detected on the +5 V supply (V_{DD1}).
4. Write unsafe detected: head open or short circuited.
5. Power failure detected on the +12 V supply (V_{DD3}).

Table 17 Sense current range select.

DN	GAIN
0	can be increased
1	can be decreased

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD1}	read circuit supply voltage		−0.3	+5.5	V
V_{DD2}	FB and write circuit supply voltage		−0.3	+5.5	V
V_{DD3}	sense current circuit supply voltage		−0.3	+13.2	V
I_{DD1}	read circuit supply current		−	150	mA
I_{DD2}	FB and write circuit supply current		−	35	mA
I_{DD3}	sense current circuit supply current		−	35	mA
$I_{I(n)}$	input current on remaining pins		−10	+10	mA
P_{tot}	maximum total power dissipation		−	1000	mW
T_{amb}	ambient temperature		0	+70	°C
T_j	junction temperature	note 1	0	+135	°C
T_{stg}	storage temperature		−50	+150	°C
$V_{ES(HB)}$	electrostatic handling: human body model	note 2	−1000	+1000	V
$V_{ES(MM)}$	electrostatic handling: machine model	note 3	−200	+200	V

Notes

1. Maximum permissible ambient temperature is dependent on internal dissipation. T_j is the discriminating factor. $T_j = (R_{th(j-a)} \times P_{tot}) + T_{amb}$, where P_{tot} is the total dissipation in the package.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor through a 25 Ω series resistor and a 2.5 μH series inductance.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air	66	K/W

QUALITY SPECIFICATION

In accordance with “*SNW-FQ-611E*”.

CHARACTERISTICS

V_{DD1} = V_{DD2} = 5 V ±5%; V_{DD3} = 12 V ±5%; T_{amb} = 25 °C ±5%; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	read circuit supply voltage		4.5	5.0	5.5	V
V_{DD2}	FB and write circuit supply voltage		4.5	5.0	5.5	V
V_{DD3}	sense current circuit supply voltage		10.8	12.0	13.2	V
I_{DD1}	read circuit supply current					
	Rd	I_{bias} = −10 to +10 mA	–	31	–	mA
	Wr	I_{write} = 30 mA	–	70	–	mA
I_{DD2}	FB and write circuit supply current					
	Rd	max gain	–	38	–	mA
	Wr		–	36	–	mA
I_{DD3}	sense current circuit supply current	I_{sense} = 16 mA	15.0	16.2	19.0	mA
V_{ref}	reference voltage	pin 20; I_O = 0 to 3 mA	1.9	2.0	2.1	V
I_{20}	current on pin 20 (V_{ref})					
	source		–	–	3.0	mA
	sink		–	–	50	μA
V_{21}	voltage at pin 21 (I_{ref})		1.2	1.3	1.4	V
I_{ref}	reference current (pin 21)		1	3	5	mA
Read section						
$G_{v(pa)}$	preamplifier voltage gain	PG1 = 1; PG0 = 1	37	38.6	41	dB
		PG1 = 0; PG0 = 1	32	32.7	34	dB
		PG1 = 1; PG0 = 0	3	4.1	6	dB
$G_{v(agc)}$	AGC amplifier voltage gain	G6DB = 1; G = 15; note 1	23	24.4	26	dB
$\Delta G_{v(agc)}$	AGC voltage gain control range	note 2	–	22	–	dB
$G_{v(yoke)}$	yoke amplifier voltage gain		19	21	23	dB
$f_{coupling}$	−3 dB AC coupling frequency	input to output	2	5	10	kHz
$f_{-3dB(cutoff)(HPF)}$	HPF −3 dB cut-off frequency	FC1 = FC1 = 0	–	1.0	–	MHz
		FC1 = 0; FC1 = 1	–	2.0	–	MHz
		FC1 = 1; FC1 = 0	–	4.7	–	MHz
		FC1 =FC1 = 1	–	10	–	MHz
$f_{-3dB(cutoff)(LPF)}$	LPF −3 dB cut-off frequency	FC1 = FC1 = 0	–	1.1	–	MHz
		FC1 = 0; FC1 = 1	–	2	–	MHz
		FC1 = 1; FC1 = 0	–	4.3	–	MHz
		FC1 =FC1 = 1	–	11	–	MHz
$V_{n(i)(eq)(preamp)}$	equivalent input noise voltage: preamplifier	Z_{source} = 0 Ω	–	0.65	0.8	nV/√Hz

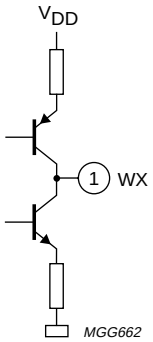
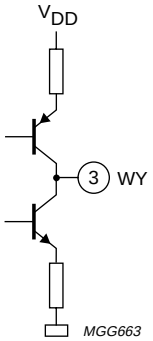
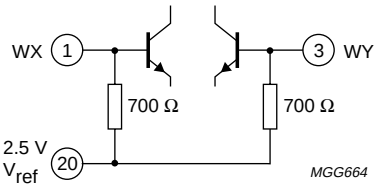
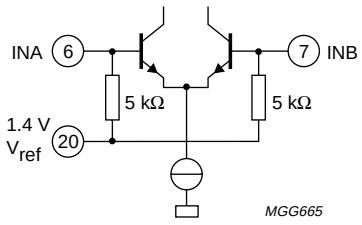
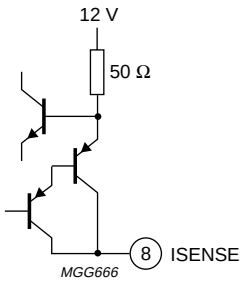
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_i	input impedance		1	1.84	4	kΩ
$V_{I(6,7)}$	DC input voltage; pins 6 and 7		1.2	1.3	1.4	V
THD	total harmonic distortion	at 34 and 40 dB gain settings; $V_{o(p-p)}$ = 1 V	–	–	–40	dB
$G_{v(servo)}$	servo preamplifier voltage gain	WX-WY to output	62	66	70	dB
$V_{n(i)(eq)(servo)}$	equivalent input noise voltage: servo pre-amp	Z_{source} = 0 Ω	–	1.8	2.8	nV/√Hz
$V_{I(1,3))}$	DC input voltage pins 1 and 3		2.4	2.5	2.6	V
I_{sense}	sense current	R_{ref} = 430 Ω; S = 64; note 3	14.6	15.2	15.8	mA
$I_{sense(max)}$	maximum sense current	all conditions; note 4	33	–	–	mA
$\Delta V_{VDD3-ISENSE}$	voltage difference between V_{DD3} and ISENSE (pins 9 and 8)		1.6	–	13.2	V
$RES_{DAC(SENSE)}$	sense DAC resolution		–	7	–	bits
$Z_{o(sense)}$	output impedance of sense current source	f = 1 kHz; $I_{o(sen)}$ = 16 mA	10	–	–	kΩ
$G_{v(FB)}$	FB amplifier voltage gain		11.5	13	14.5	dB
$B_{(-3dB)}$	–3 dB bandwidth of FB amplifier		–	5	–	MHz
$f_{coupling(FBamp)}$	–3 dB AC coupling of FB amplifier		–	3	–	kHz
I_{bias}	bias current amplitude (peak-to-peak)	ENFB1 = 0; ENFB0 = 1	–10	–	+10	mA
		ENFB1 = 1; ENFB0 = 0	0	–	+9	mA
		ENFB1 = ENFB0 = 1	–10	–	+20	mA
$V_{O(23,24)}$	DC voltage level of FB outputs (pins 23 and 24)	B = 0; see Table 3	1.6	1.8	2.0	V
$\Delta V_{BIASA-BIASB}$	voltage difference between BIASA and BIASB (pins 23 and 24) at maximum DC bias voltage	B = 31; see Table 3; bias load 88 Ω	1.4	1.52	1.6	V
$RES_{DAC(BIAS)}$	bias DAC resolution		–	5	–	bits
$V_{O(18,19)}$	read amplifier DC output voltage (pins 18 and 19)		2.4	2.5	2.6	V
$\Delta V_{OO(18,19)}$	read amplifier DC offset voltage (voltage change at pins 18 and 19)		–	–	100	mV
$V_{o(rms)(18,19)}$	output voltage (RMS value; pins 18 and 19)		–	–	0.5	V
I_o	guaranteed output current		1.5	–	–	mA
$V_{O(AGCL)}$	lower AGC detection voltage level at OUTB		2.15	2.2	2.25	V
$V_{O(AGCH)}$	upper AGC detection voltage level at OUTB		2.75	2.8	2.85	V

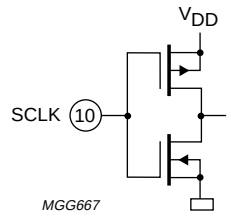
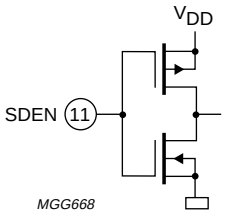
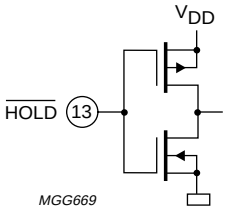
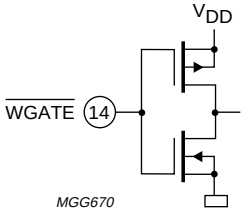
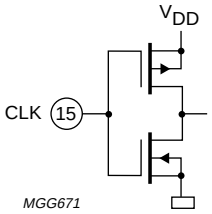
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{hys(AGC)}$	hysteresis in AGC detection level		65	75	85	mV
B_{AGC}	AGC bandwidth		–	1.5	–	MHz
f_{clk}	operational clock	note 5	0	24	24	MHz
Write section						
I_{write}	write current	R_{head} = 10 Ω; R_{ref} = 430Ω; 0-peak; W = 32; note 6	27.3	28.8	30.3	mA
$I_{write(max)}$	maximum write current	R_{head} = 10 Ω; note 7	60	80	–	mA
ΔI_{write}	difference between positive and negative write currents	I_{write} = 30 mA;	–	0	5	%
$t_{t(iwrite)(Rload)}$	write current transition time	note 8				
	resistive load	resistive load, 10 Ω	–	4	–	ns
	head load	R_{head} = 10 Ω; L_{head} = 200 nH	–	6	12	ns
$V_{o(p-p)(1,3)}$	output voltage swing (peak-to-peak value)		3	–	–	V
t_{R-W}	read to write time		–	0.2	–	µs
t_{W-R}	write to read time		–	10	–	µs
Δt_{WD}	WD pulse asymmetry	in WDI mode; note 9	–	0	1	ns
t_{WDIH}	WDI pulse time HIGH		5	–	–	ns
t_{WDIL}	WDI pulse time LOW		5	–	–	ns
$R_{det(WUS)}$	WUS detection resistance level	short circuited to V_{DD} or V_{SS}; I_{write} = 30 mA	–	–	10	Ω
		open; I_{write} = 30 mA	150	–	–	Ω

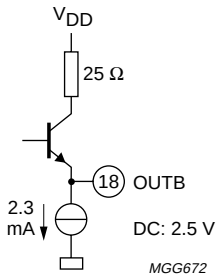
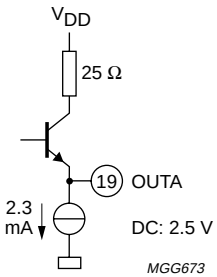
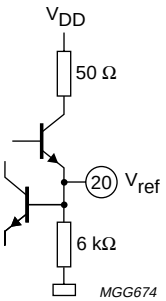
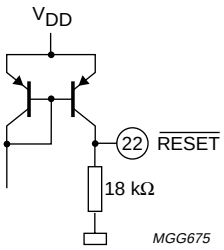
Notes

1. G is a 4-bit number contained in control bits G0 to G3 (see Table 12).
2. 6 dB step via a fixed setting, and 16 dB (in 1 dB steps) via AGC control.
3. S is a 7-bit number contained in control bits S0 to S6 (see Table 15).
4. The TZA1000 is guaranteed to operate reliably with sense currents of up to 33 mA.
5. The operational clock frequency (pin 15) must be >16 times higher the SCLK frequency to ensure reliable serial transfer.
6. W is a 7-bit number contained in control bits W0 to W6 (see Table 14). A more accurate calculation of the write current would be given by: $I_c = I_t - 0.003 \times I_t^2$, where $I_t = 125 (W + 1) / 128$, I_t the target current and I_c the write current.
7. The TZA1000 is guaranteed to supply a write current of up to 60 mA.
8. 10 to 90% of a total current reversal.
9. Difference between negative-to-positive and positive-to-negative current slopes.

EQUIVALENT PIN CIRCUITS

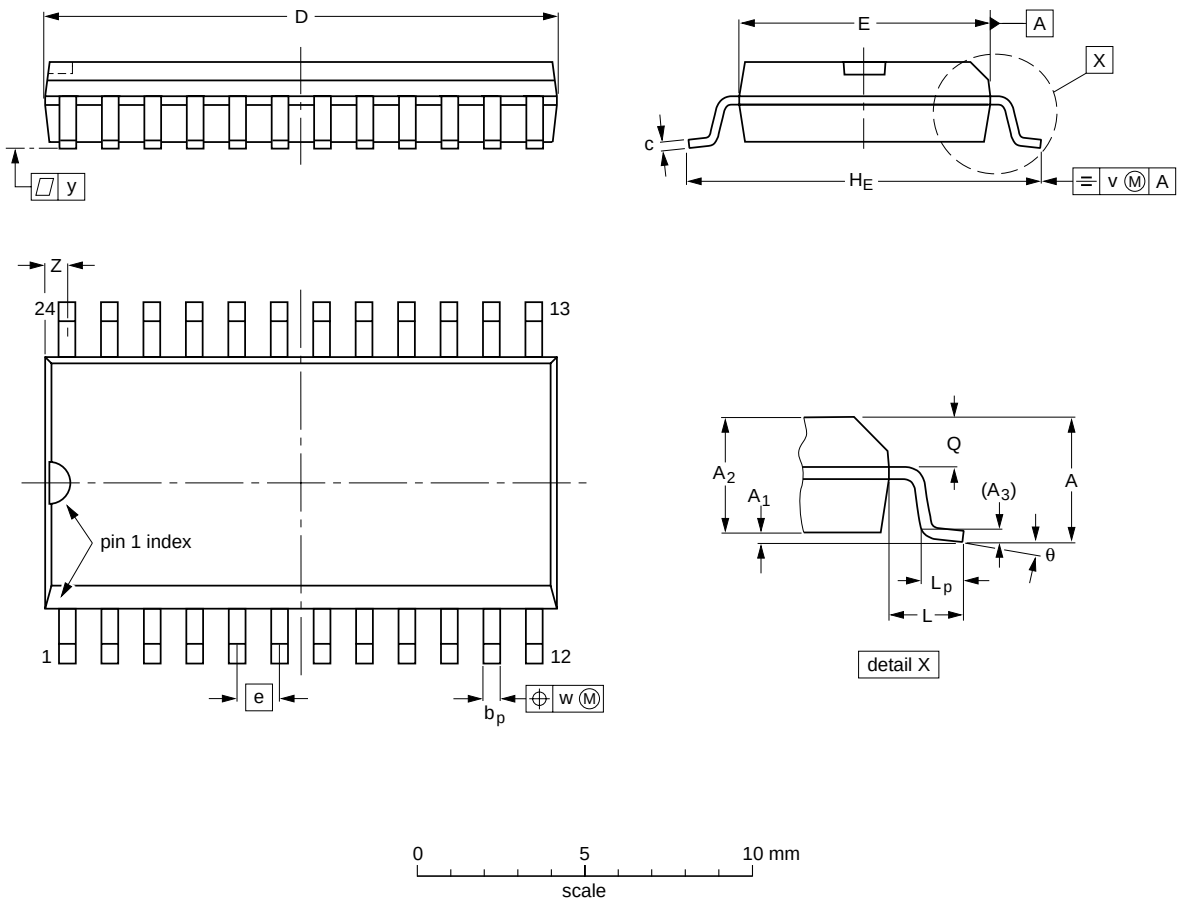
PIN	DESCRIPTION	EQUIVALENT PIN CIRCUIT
1	write output stage	
3	write output stage	
1,3,20	servo input configuration	
6,7,20	input configuration	
8	sense output configuration	

PIN	DESCRIPTION	EQUIVALENT PIN CIRCUIT
10	digital input configuration	
11	digital input configuration	
13	digital input configuration	
14	digital input configuration	
15	digital input configuration	

PIN	DESCRIPTION	EQUIVALENT PIN CIRCUIT
18	output configuration	
19	output configuration	
20	V_{ref} output configuration	
22	reset output configuration	

PACKAGE OUTLINE

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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