## INTEGRATED CIRCUITS

## DATA SHEET

# **74ALS10A**Triple 3-Input NAND gate

Product specification

1991 Feb 08

IC05 Data Handbook





## **Triple 3-input NAND gate**

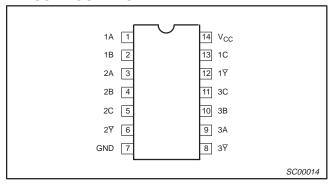
## **74ALS10A**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS10A	4.0ns	1.8mA

## **ORDERING INFORMATION**

	ORDER CODE		
DESCRIPTION	COMMERCIAL RANGE $V_{CC}$ = 5V $\pm 10\%$ , $T_{amb}$ = 0°C to $\pm 70$ °C	DRAWING NUMBER	
14-pin plastic DIP	74ALS10AN	SOT27-1	
14-pin plastic SO	74ALS10AD	SOT108-1	

## **PIN CONFIGURATION**

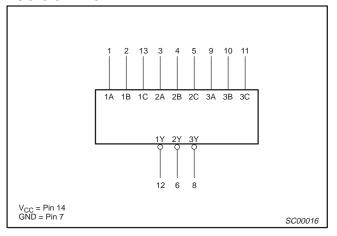


## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

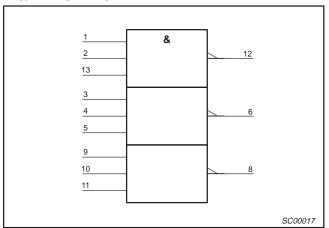
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
nA, nB, nC	Data inputs	1.0/1.0	20μA/0.1mA
n∀	Data outputs	20/80	0.4mA/8mA

**NOTE**: One (1.0) ALS unit load is defined as: 20μA in the High state and 0.1mA in the Low state.

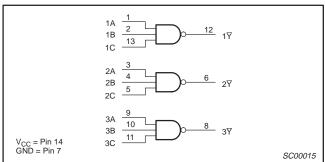
## **LOGIC SYMBOL**



## **IEC/IEEE SYMBOL**



## **LOGIC DIAGRAM**



## **FUNCTION TABLE**

	INPUTS	OUTPUT	
nA	nB	nC	n₹
Н	Н	Н	L
L	Х	Х	Н
Х	L	Х	Н
Х	Х	L	Н

H = High voltage level L = Low voltage level

X = Don't care

## Triple 3-input NAND gate

74ALS10A

#### **ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	−0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	16	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

#### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		UNIT		
STIVIBUL	PARAMETER	MIN	NOM	MAX	UNII
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>lk</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-0.4	mA
I <sub>OL</sub>	Low-level output current			8	mA
T <sub>amb</sub>	Operating free-air temperature range	0		+70	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS		UNIT			
STIMBUL			TEST CONDITIONS	MIN	TYP <sup>2</sup>	MAX	UNII	
V <sub>OH</sub>	High-level output voltage		$V_{CC}\pm 10\%$ , $V_{IL}=MAX$ , $V_{IH}=MIN$	$I_{OH} = -0.4 \text{mA}$	V <sub>CC</sub> - 2			V
V	Low lovel output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX,	$I_{OL} = 4mA$		0.25	0.40	V
V <sub>OL</sub>	Low-level output voltage		V <sub>IH</sub> = MIN	$I_{OL} = 8mA$		0.35	0.50	V
V <sub>IK</sub>	Input clamp voltage		$V_{CC} = MIN, I_I = I_{IK}$			-0.73	-1.5	V
II	Input current at maximum input vo	oltage	$V_{CC} = MAX, V_I = 7.0V$				0.1	mA
I <sub>IH</sub>	High-level input current		$V_{CC} = MAX, V_I = 2.7V$				20	μΑ
I <sub>IL</sub>	Low-level input current		$V_{CC} = MAX, V_I = 0.5V$				-0.1	mA
Io	Output current <sup>3</sup>		$V_{CC} = MAX, V_O = 2.25V$		-30		-112	mA
1	Supply ourrant (total)	I <sub>CCH</sub>	V MAY	$V_I = 0V$		0.5	0.6	mA
Icc	Supply current (total)		$V_{CC} = MAX$	V <sub>I</sub> = 4.5V		1.6	2.2	mA

#### NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at  $V_{CC}$  = 5V,  $T_{amb}$  = 25°C.

3. The output conditions have been chosen to produce a current that closely approximate one half of the true short-circuit output current, I<sub>OS</sub>.

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## Triple 3-input NAND gate

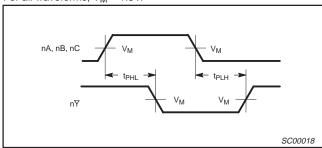
74ALS10A

#### **AC ELECTRICAL CHARACTERISTICS**

			LIM		
SYMBOL	PARAMETER	TEST CONDITION	T <sub>amb</sub> = 0°C V <sub>CC</sub> = +5. C <sub>L</sub> = 50pF,		UNIT
			MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nA, nB, nC to $\overline{\text{NY}}$	Waveform 1	2.0 2.0	11.0 10.0	ns

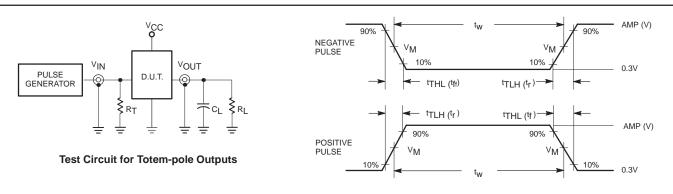
## **AC WAVEFORMS**

For all waveforms,  $V_M = 1.3V$ .



Waveform 1. Propagation Delay for Data to Output

## **TEST CIRCUIT AND WAVEFORMS**



### **DEFINITIONS:**

R<sub>L</sub> = Load resistor;

see AC electrical characteristics for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

Innut	Pulse	Definition
IIIput	ruise	Dellillilloll

Family		INPUT PULSE REQUIREMENTS								
Family	Amplitude	$V_{\text{M}}$	Rep.Rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>				
74ALS	3.5V	1.3V	1MHz	500ns	2.0ns	2.0ns				

SC00005

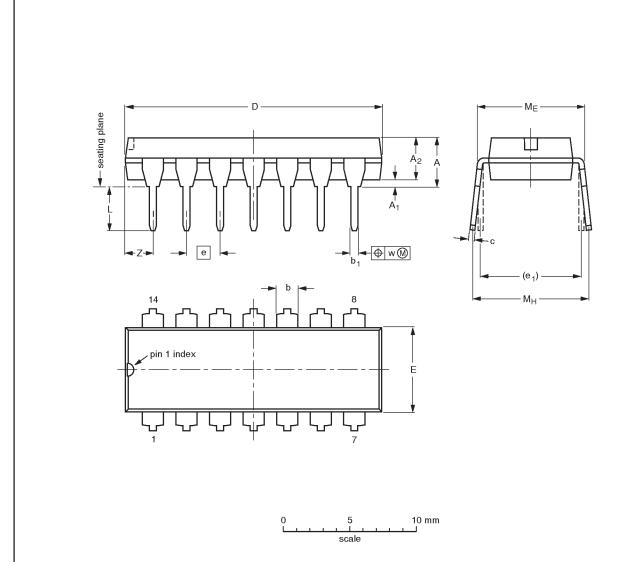
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## Triple 3-input NAND gate

74ALS10A

## DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



#### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	e <sub>1</sub>	L	ME	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	EC JEDEC EIAJ PROJECTION		ISSUE DATE	
SOT27-1	050G04	MO-001AA			<del>92-11-17</del> 95-03-11

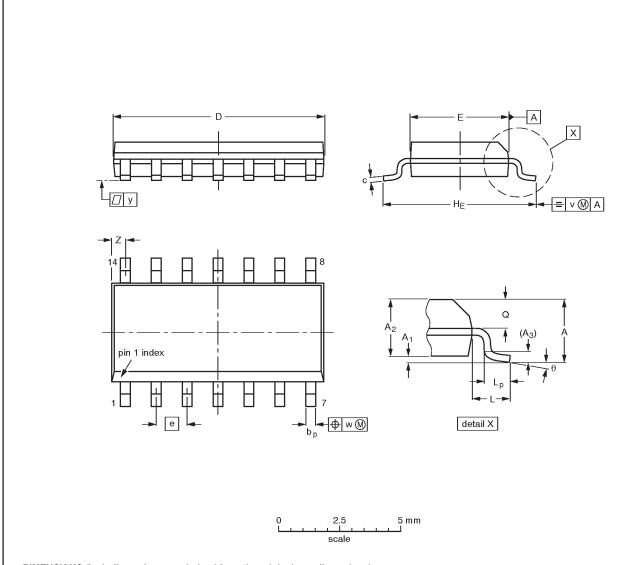
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## Triple 3-input NAND gate

74ALS10A

## SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Ø	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01		0.0098 0.0075		0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT108-1	076E06\$	MS-012AB				<del>91-08-13</del> 95-01-23	

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## Triple 3-input NAND gate

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DEFINITIONS							
Data Sheet Identification	Product Status	Definition					
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.					
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Phil Semiconductors reserves the right to make changes at any time without notice in order to improve des and supply the best possible product.					
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