INTEGRATED CIRCUITS

DATA SHEET

89C535/89C536/89C538

CMOS single-chip 8-bit microcontrollers with FLASH program memory

Preliminary specification

1997 June 05

IC20 Data Handbook

Philips Semiconductors

PHILIPS

DESCRIPTION

The 89C535/89C536/89C538 are Single-Chip 8-Bit Microcontrollers manufactured in advanced CMOS process and are derivatives of the 80C51 microcontroller family. All the devices have the same instruction set as the 80C51.

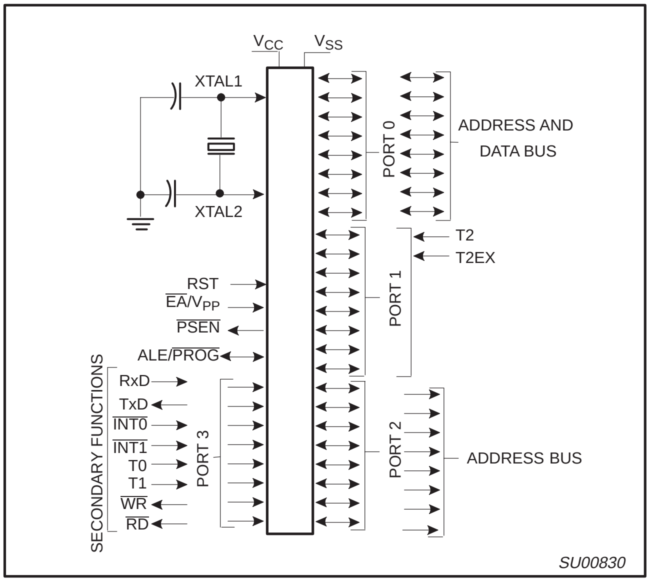
The devices also have four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, two-priority-level, nested interrupt structure, UART and on-chip oscillator and timing circuits. For systems that require extra data memory capability up to 64k bytes, each can be expanded using standard TTL-compatible memories and logic.

The 89C535/89C536/89C538 contain a non-volatile FLASH EPROM program memory (8K bytes in 89C535, 16k bytes in the 89C536, and 64k bytes in the 89C538). The devices have 512 bytes of RAM data memory.

FEATURES

- 80C51 Central Processing Unit
- 8k x 8 (89C535) 16k × 8 (89C536) or 64k × 8 (89C538), FLASH EPROM Program Memory
- 512 × 8 RAM, externally expandable to 64k × 8 Data Memory
- Three 16-bit counter/timers
- Up to 3 external interrupt request inputs
- 6 interrupt sources with 2 priority levels
- Four 8-bit I/O ports
- Full-duplex UART
- Power control modes
  - Idle mode
  - Power down mode, with wakeup from power down using external interrupt
- 44-pin PLCC and QFP packages

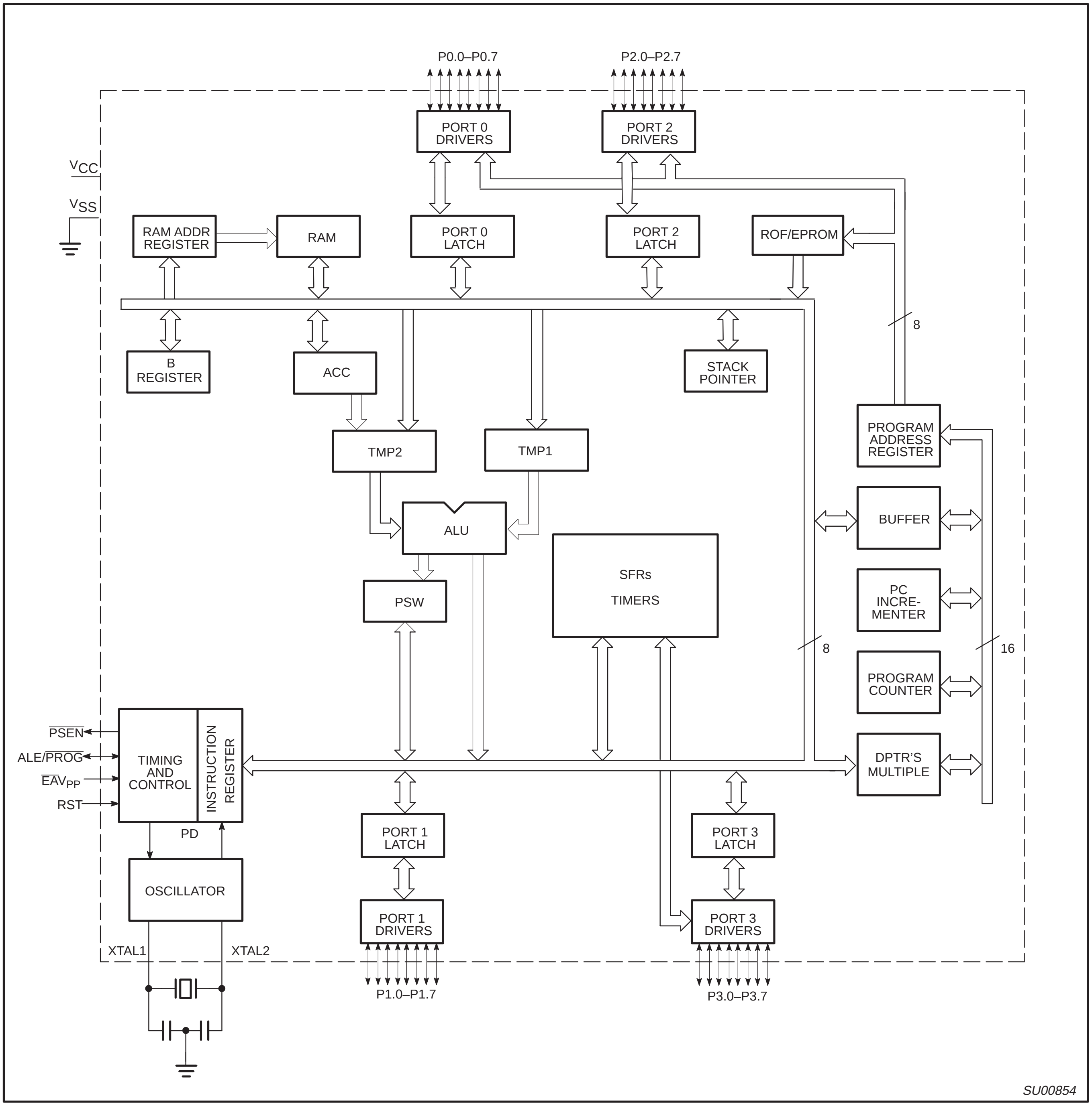
LOGIC SYMBOL



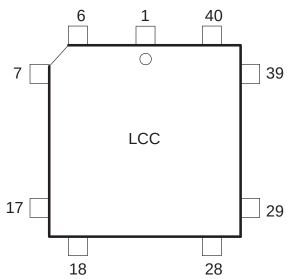
ORDERING INFORMATION

PART NUMBER	MEMORY SIZE	TEMPERATURE RANGE (°C) AND PACKAGE	FREQ. (MHz)	DRAWING NUMBER
P89C535NBA A	8k bytes	0 to +70, 44-pin Plastic Leaded Chip Carrier	33	SOT187-2
P89C536NBA A	16k bytes	0 to +70, 44-pin Plastic Leaded Chip Carrier	33	SOT187-2
P89C536NBB B	16k bytes	0 to +70, 44-pin Plastic Quad Flat Package	33	SOT307-2
P89C538NBA A	64k bytes	0 to +70, 44-pin Plastic Leaded Chip Carrier	33	SOT187-2
P89C538NBB B	64k bytes	0 to +70, 44-pin Plastic Quad Flat Package	33	SOT307-2

BLOCK DIAGRAM



CERAMIC AND PLASTIC LEADED CHIP CARRIER PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	V_{SS}	16	P3.4/T0	31	P2.7/A15
2	P1.0/T2	17	P3.5/T1	32	$\overline{PSEN}$
3	P1.1/T2EX	18	P3.6/$\overline{WR}$	33	ALE/$\overline{PROG}$
4	P1.2/ECI	19	P3.7/$\overline{RD}$	34	NIC*
5	P1.3	20	XTAL2	35	$\overline{EA}$/V_{PP}
6	P1.4	21	XTAL1	36	P0.7/AD7
7	P1.5	22	V_{SS}	37	P0.6/AD6
8	P1.6	23	V_{CC}	38	P0.5/AD5
9	P1.7	24	P2.0/A8	39	P0.4/AD4
10	RST	25	P2.1/A9	40	P0.3/AD3
11	P3.0/RxD	26	P2.2/A10	41	P0.2/AD2
12	NIC*	27	P2.3/A11	42	P0.1/AD1
13	P3.1/TxD	28	P2.4/A12	43	P0.0/AD0
14	P3.2/$\overline{INT0}$	29	P2.5/A13	44	V_{CC}
15	P3.3/$\overline{INT1}$	30	P2.6/A14		

* NO INTERNAL CONNECTION

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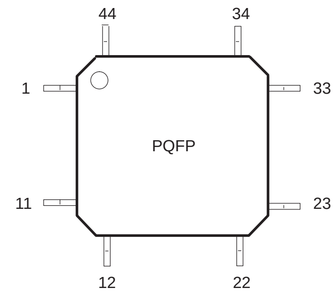
PLASTIC QUAD FLAT PACK PIN FUNCTIONS



Pin	Function	Pin	Function	Pin	Function
1	P1.5	16	V_{SS}	31	P0.6/AD6
2	P1.6	17	V_{CC}	32	P0.5/AD5
3	P1.7	18	P2.0/A8	33	P0.4/AD4
4	RST	19	P2.1/A9	34	P0.3/AD3
5	P3.0/RxD	20	P2.2/A10	35	P0.2/AD2
6	NIC*	21	P2.3/A11	36	P0.1/AD1
7	P3.1/TxD	22	P2.4/A12	37	P0.0/AD0
8	P3.2/$\overline{INT0}$	23	P2.5/A13	38	V_{CC}
9	P3.3/$\overline{INT1}$	24	P2.6/A14	39	V_{SS}
10	P3.4/T0	25	P2.7/A15	40	P1.0/T2
11	P3.5/T1	26	$\overline{PSEN}$	41	P1.1/T2EX
12	P3.6/$\overline{WR}$	27	ALE/$\overline{PROG}$	42	P1.2
13	P3.7/$\overline{RD}$	28	NIC*	43	P1.3
14	XTAL2	29	$\overline{EA}$/V_{PP}	44	P1.4
15	XTAL1	30	P0.7/AD7		

* NO INTERNAL CONNECTION

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PIN DESCRIPTIONS

MNEMONIC	PIN NUMBER LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	1, 22	16, 39	I	**Ground:** 0V reference.
V_{CC}	23, 44	17, 38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification and received code bytes during EEPROM programming. External pull-ups are required during program verification.
P1.0–P1.7	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification.
				Alternate functions for Port 1 include:
	2	40	I/O	**T2 (P1.0):** Timer/Counter 2 external count input
	3	41	I	**T2EX (P1.1):** Timer/Counter 2 Reload/Capture
P2.0–P2.7	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. Some Port 2 pins receive the high order address bits during EEPROM programming and verification.
P3.0–P3.7	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	11	5	I	**RxD (P3.0):** Serial input port
	13	7	O	**TxD (P3.1):** Serial output port
	14	8	I	**$\overline{\text{INT0}}$ (P3.2):** External interrupt
	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt
	16	10	I	**T0 (P3.4):** Timer 0 external input
	17	11	I	**T1 (P3.5):** Timer 1 external input
	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
RST	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{\text{PROG}}$	33	27	O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EEPROM programming.
$\overline{\text{PSEN}}$	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the processor is executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory. If $\overline{\text{EA}}$ is held high, the device executes from internal program memory. This pin also receives the 12V programming supply voltage (V_{PP}) during EPROM programming. $\overline{\text{EA}}$ is internally latched on Reset.
XTAL1	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

Table 1. Special Function Registers

SYMBOL	DESCRIPTION	DIRECT ADDRESS	BIT ADDRESS, SYMBOL, OR ALTERNATIVE PORT FUNCTION MSB							LSB	RESET VALUE
ACC*	Accumulator	E0H	E7	E6	E5	E4	E3	E2	E1	E0	00H
B*	B register	F0H	F7	F6	F5	F4	F3	F2	F1	F0	00H
DPTR:	Data Pointer (2 bytes)										
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
			AF	AE	AD	AC	AB	AA	A9	A8	
IE*	Interrupt Enable	A8H	EA	–	ET2	ES	ET1	EX1	ET0	EX0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP*	Interrupt Priority	B8H	–	–	PT2	PS	PT1	PX1	PT0	PX0	x0000000B
			87	86	85	84	83	82	81	80	
P0*	Port 0	80H	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	FFH
			97	96	95	94	93	92	91	90	
P1*	Port 1	90H	–	–	–	–	–	–	T2EX	T2	FFH
			A7	A6	A5	A4	A3	A2	A1	A0	
P2*	Port 2	A0H	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	FFH
			B7	B6	B5	B4	B3	B2	B1	B0	
P3*	Port 3	B0H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD	FFH
PCON#	Power Control	87H	SMOD	–	–	–	GF1	GF0	PD	IDL	0xxxx000B
			D7	D6	D5	D4	D3	D2	D1	D0	
PSW*	Program Status Word	D0H	CY	AC	F0	RS1	RS0	OV	–	P	00H
RACAP2H#	Timer 2 Capture High	CBH									00H
RACAP2L#	Timer 2 Capture Low	CAH									00H
SBUF	Serial Data Buffer	99H									xxxxxxxxB
			9F	9E	9D	9C	9B	9A	99	98	
SCON*	Serial Control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SP	Stack Pointer	81H									07H
			8F	8E	8D	8C	8B	8A	89	88	
TCON*	Timer Control	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
			CF	CE	CD	CC	CB	CA	C9	C8	
T2CON*	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	00H
TH0	Timer High 0	8CH									00H
TH1	Timer High 1	8DH									00H
TH2#	Timer High 2	CDH									00H
TL0	Timer Low 0	8AH									00H
TL1	Timer Low 1	8BH									00H
TL2#	Timer Low 2	CCH									00H
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	00H

* SFRs are bit addressable.
\# SFRs are modified from or added to the 80C51 SFRs.
– Reserved bits.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up. Ports 1, 2, and 3 will asynchronously be driven to their reset condition when a voltage above V_{IH1} (min.) is applied to RESET.

LOW POWER MODES

Idle Mode

In the idle mode (see Table 2), the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

Power-Down Mode

To save even more power, a Power Down mode (see Table 2) can be invoked by software. In this mode, the oscillator is stopped and the instruction that invoked Power Down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values down to 2.0V and care must be taken to return V_{CC} to the minimum specified operating voltages before the Power Down Mode is terminated.

Either a hardware reset or external interrupt can be used to exit from Power Down. Reset redefines all the SFRs but does not change the on-chip RAM. An external interrupt allows both the SFRs and the on-chip RAM to retain their values.

To properly terminate Power Down the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize (normally less than 10ms).

With an external interrupt, INT0 and INT1 must be enabled and configured as level-sensitive. Holding the pin low restarts the oscillator but bringing the pin back high completes the exit. Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put the device into Power Down.

Design Consideration

- To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to memory.

ONCE™ Mode

The ONCE (“On-Circuit Emulation”) Mode facilitates testing and debugging of systems without the device having to be removed from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 8XC51FA/FB is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

Table 2. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

TIMER 2 OPERATION

Timer 2

Timer 2 is a 16-bit Timer/Counter which can operate as either an event timer or an event counter, as selected by C/T2* in the special function register T2CON (see Figure 1). Timer 2 has three operating modes:Capture, Auto-reload, and Baud Rate Generator, which are selected by bits in the T2CON as shown in Table 3.

Capture Mode

In the capture mode there are two options which are selected by bit EXEN2 in T2CON. If EXEN2=0, then timer 2 is a 16-bit timer or counter (as selected by C/T2* in T2CON) which, upon overflowing sets bit TF2, the timer 2 overflow bit. This bit can be used to generate an interrupt (by enabling the Timer 2 interrupt bit in the IE register/SFR table). If EXEN2= 1, Timer 2 operates as described above, but with the added feature that a 1- to -0 transition at external input T2EX causes the current value in the Timer 2 registers, TL2 and TH2, to be captured into registers RCAP2L and RCAP2H, respectively. In addition, the transition at T2EX causes bit EXF2 in T2CON to be set, and EXF2 like TF2 can generate an interrupt (which vectors to the same location as Timer 2 overflow interrupt. The Timer 2 interrupt service routine can interrogate TF2 and EXF2 to determine which event caused the interrupt). The capture mode is illustrated in Figure 2 (There is no reload value for TL2 and TH2 in this mode. Even when a capture event occurs from T2EX, the counter keeps on counting T2EX pin transitions or osc/12 pulses.).

Auto-Reload Mode

In the 16-bit auto-reload mode, Timer 2 can be configured as either a timer or counter (C/T2* in T2CON).

Figure 3 shows the auto–reload mode of Timer 2. In this mode there are two options selected by bit EXEN2 in T2CON register. If EXEN2=0, then Timer 2 counts up to 0FFFFH and sets the TF2 (Overflow Flag) bit upon overflow. This causes the Timer 2 registers to be reloaded with the 16-bit value in RCAP2L and RCAP2H.

The values in RCAP2L and RCAP2H are preset by software. If EXEN2=1, then a 16-bit reload can be triggered either by an overflow or by a 1-to-0 transition at input T2EX. This transition also sets the EXF2 bit. The Timer 2 interrupt, if enabled, can be generated when either TF2 or EXF2 are 1.

The external flag EXF2 toggles when Timer 2 underflows or overflows. This EXF2 bit can be used as a 17th bit of resolution if needed. The EXF2 flag does not generate an interrupt in this mode of operation.

(MSB) (LSB)

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$

Symbol	Position	Name and Significance
TF2	T2CON.7	Timer 2 overflow flag set by a Timer 2 overflow and must be cleared by software. TF2 will not be set when either RCLK or TCLK = 1.
EXF2	T2CON.6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 will cause the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON.5	Receive clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TCLK	T2CON.4	Transmit clock flag. When set, causes the serial port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON.3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of a negative transition on T2EX if Timer 2 is not being used to clock the serial port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON.2	Start/stop control for Timer 2. A logic 1 starts the timer.
$C/\overline{T2}$	T2CON.1	Timer or counter select. (Timer 2) 0 = Internal timer (OSC/12) 1 = External event counter (falling edge triggered).
$CP/\overline{RL2}$	T2CON.0	Capture/Reload flag. When set, captures will occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads will occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the timer is forced to auto-reload on Timer 2 overflow.

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Figure 1. Timer/Counter 2 (T2CON) Control Register

Table 3. Timer 2 Operating Modes

RCLK + TCLK	$CP/\overline{RL2}$	TR2	MODE
0	0	1	16-bit Auto-reload
0	1	1	16-bit Capture
1	X	1	Baud rate generator
X	X	0	(off)

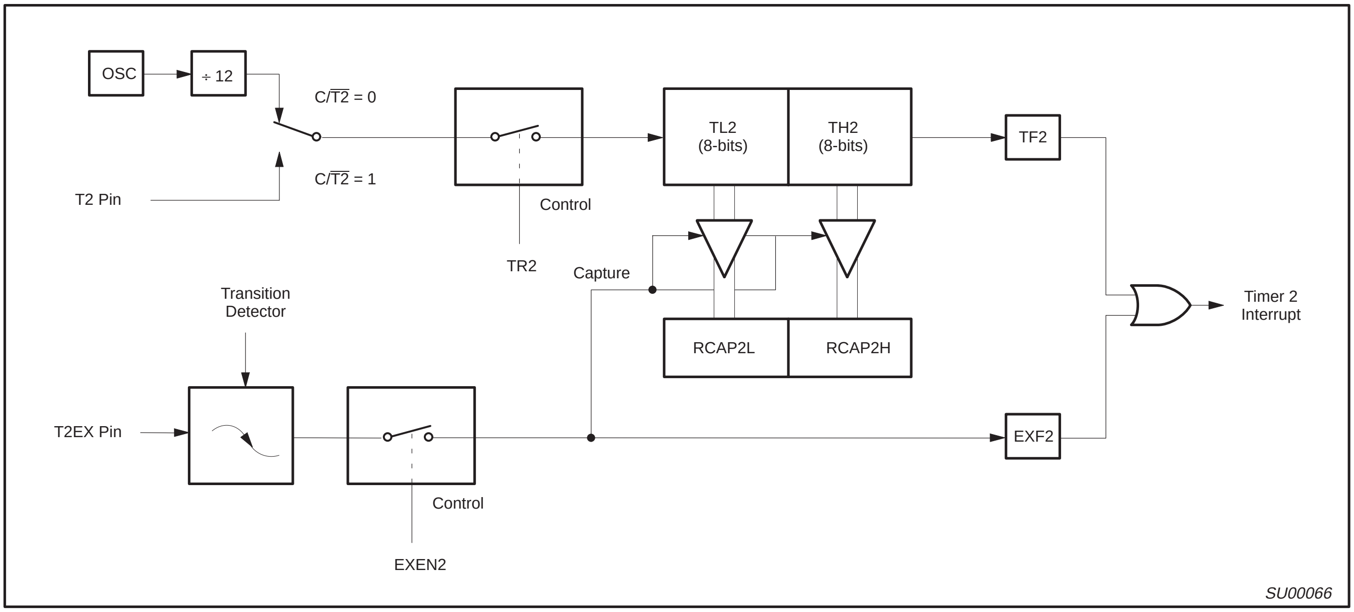

Figure 2. Timer 2 in Capture Mode

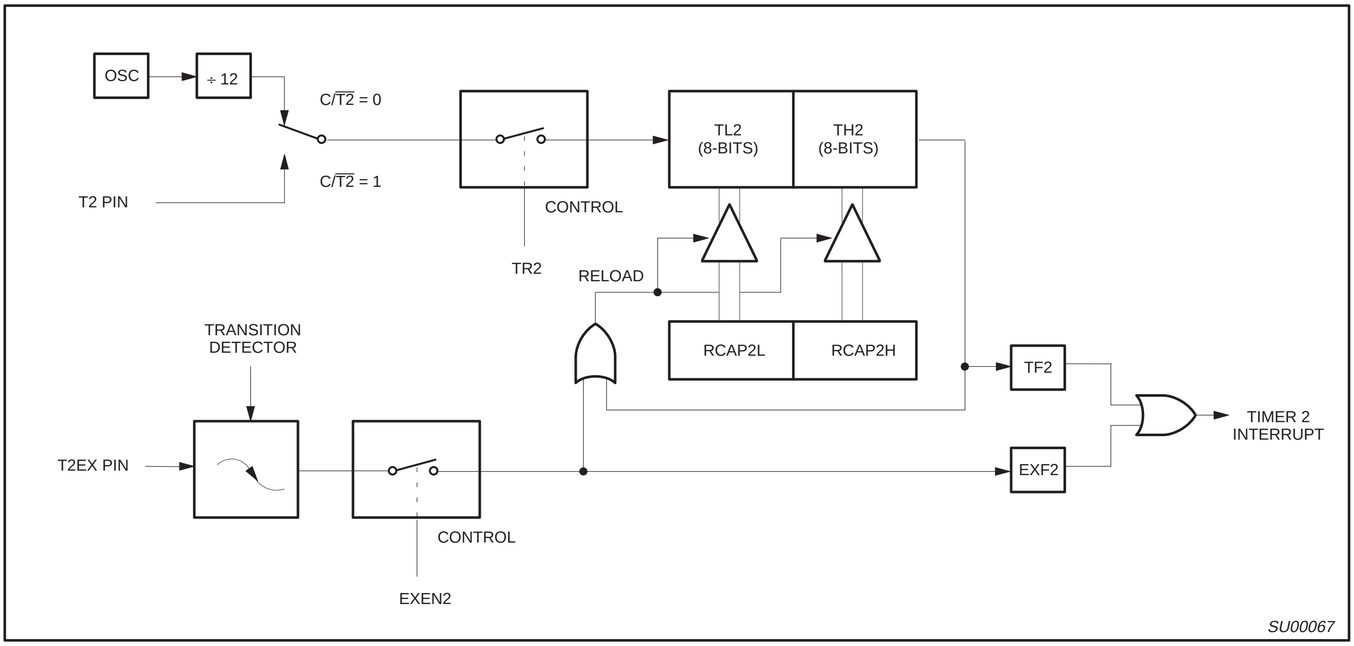

Figure 3. Timer 2 in Auto-Reload Mode

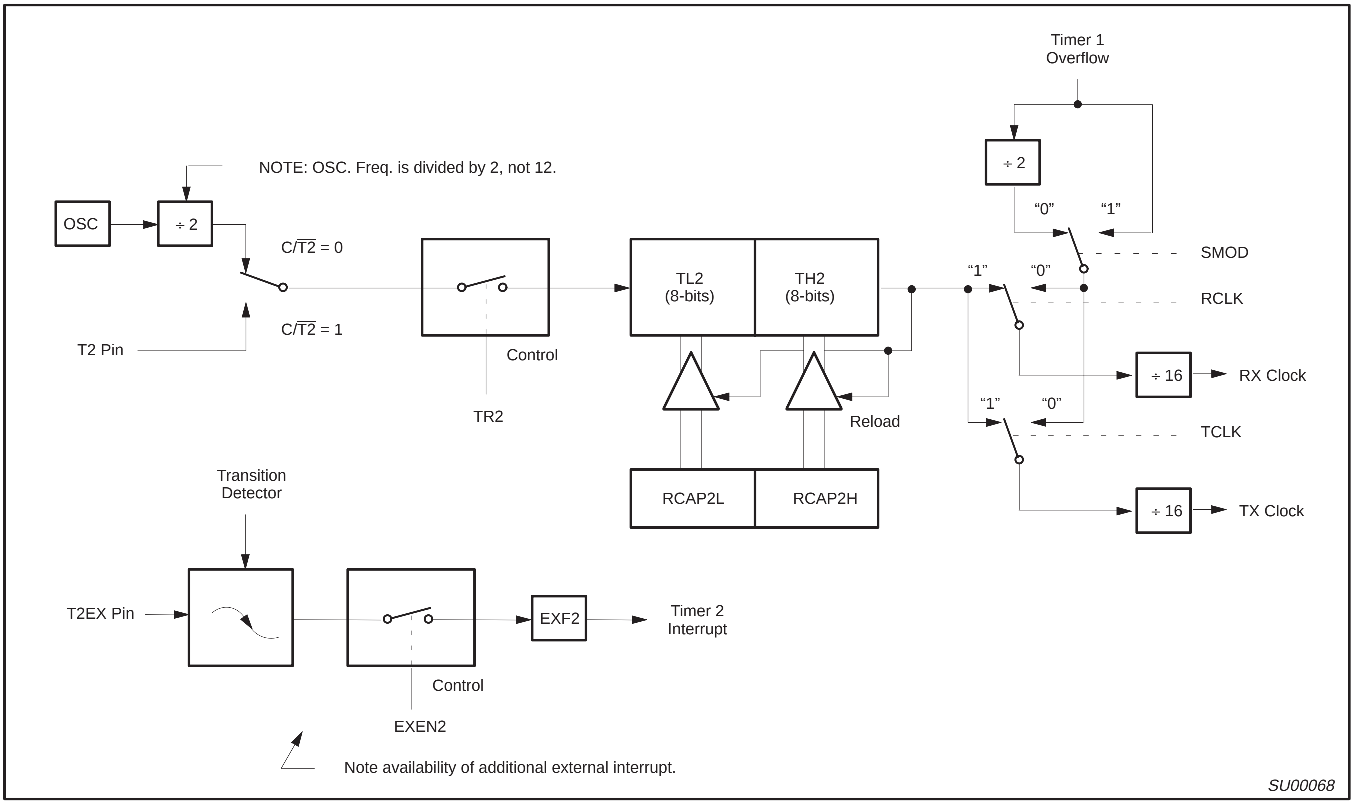

Figure 4. Timer 2 in Baud Rate Generator Mode

Table 4. Timer 2 Generated Commonly Used Baud Rates

Baud Rate	Osc Freq	Timer 2	
		RCAP2H	RCAP2L
375K	12MHz	FF	FF
9.6K	12MHz	FF	D9
2.8K	12MHz	FF	B2
2.4K	12MHz	FF	64
1.2K	12MHz	FE	C8
300	12MHz	FB	1E
110	12MHz	F2	AF
300	6MHz	FD	8F
110	6MHz	F9	57

Baud Rate Generator Mode

Bits TCLK and/or RCLK in T2CON (Table 3) allow the serial port transmit and receive baud rates to be derived from either Timer 1 or Timer 2. When TCLK= 0, Timer 1 is used as the serial port transmit baud rate generator. When TCLK= 1, Timer 2 is used as the serial port transmit baud rate generator. RCLK has the same effect for the serial port receive baud rate. With these two bits, the serial port can have different receive and transmit baud rates – one generated by Timer 1, the other by Timer 2.

Figure 4 shows the Timer 2 in baud rate generation mode. The baud rate generation mode is like the auto-reload mode,in that a rollover in TH2 causes the Timer 2 registers to be reloaded with the 16-bit value in registers RCAP2H and RCAP2L, which are preset by software.

The baud rates in modes 1 and 3 are determined by Timer 2's overflow rate given below:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

The timer can be configured for either "timer" or "counter" operation. In many applications, it is configured for "timer" operation (C/T2*=0). Timer operation is different for Timer 2 when it is being used as a baud rate generator.

Usually, as a timer it would increment every machine cycle (i.e., 1/12 the oscillator frequency). As a baud rate generator, it increments every state time (i.e., 1/2 the oscillator frequency). Thus the baud rate formula is as follows:

$$\text{Modes 1 and 3 Baud Rates} = \frac{\text{Oscillator Frequency}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where: (RCAP2H, RCAP2L)= The content of RCAP2H and RCAP2L taken as a 16-bit unsigned integer.

The Timer 2 as a baud rate generator mode shown in Figure 4, is valid only if RCLK and/or TCLK = 1 in T2CON register. Note that a rollover in TH2 does not set TF2, and will not generate an interrupt. Thus, the Timer 2 interrupt does not have to be disabled when Timer 2 is in the baud rate generator mode. Also if the EXEN2 (T2 external enable flag) is set, a 1-to-0 transition in T2EX (Timer/counter 2 trigger input) will set EXF2 (T2 external flag) but will not cause a reload from (RCAP2H, RCAP2L) to (TH2,TL2). Therefore when Timer 2 is in use as a baud rate generator, T2EX can be used as an additional external interrupt, if needed.

When Timer 2 is in the baud rate generator mode, one should not try to read or write TH2 and TL2. As a baud rate generator, Timer 2 is incremented every state time (osc/2) or asynchronously from pin T2; under these conditions, a read or write of TH2 or TL2 may not be accurate. The RCAP2 registers may be read, but should not be written to, because a write might overlap a reload and cause write and/or reload errors. The timer should be turned off (clear TR2) before accessing the Timer 2 or RCAP2 registers.

Table 4 shows commonly used baud rates and how they can be obtained from Timer 2.

Summary Of Baud Rate Equations

Timer 2 is in baud rate generating mode. If Timer 2 is being clocked through pin T2(P1.0) the baud rate is:

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If Timer 2 is being clocked internally , the baud rate is:

$$\text{Baud Rate} = \frac{f_{OSC}}{[32 \times [65536 - (\text{RCAP2H}, \text{RCAP2L})]]}$$

Where f_{OSC}= Oscillator Frequency

To obtain the reload value for RCAP2H and RCAP2L, the above equation can be rewritten as:

$$\text{RCAP2H}, \text{RCAP2L} = 65536 - \left(\frac{f_{OSC}}{32 \times \text{Baud Rate}}\right)$$

Timer/Counter 2 Set-up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set, separately, to turn the timer on. see Table 5 for set-up of Timer 2 as a timer. Also see Table 6 for set-up of Timer 2 as a counter.

Table 5. Timer 2 as a Timer

MODE	T2CON	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
Receive only	24H	26H
Transmit only	14H	16H

Table 6. Timer 2 as a Counter

MODE	TMOD	
	INTERNAL CONTROL (Note 1)	EXTERNAL CONTROL (Note 2)
16-bit	02H	0AH
Auto-Reload	03H	0BH

NOTES:
1. Capture/reload occurs only on timer/counter overflow.
2. Capture/reload occurs on timer/counter overflow and a 1-to-0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generator mode.

Serial Interface

The 89C538/536 has a standard 80C51 serial port. This serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (throughTxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1, Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through jRxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. Reception is initiated in the other modes by the incoming start bit if REN = 1.

Serial Port Control Register

The serial port control and status register is the Special FunctionRegister SCON, shown in Figure 5. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Additional details of serial port operation may be found in the 80C51 Family Hardware Description found in the *Philips 80C51–Based 8–Bit Microcontroller Data Handbook, IC20*.

SCON Address = 98H Reset Value = 0000 0000B

Bit Addressable

	SM0	**SM1**	**SM2**	**REN**	**TB8**	**RB8**	**TI**	**RI**
Bit:	7	6	5	4	3	2	1	0

Symbol	Function
SM0	Serial Port Mode Bit 0
SM1	Serial Port Mode Bit 1

SM0	SM1	Mode	Description	Baud Rate**
0	0	0	shift register	$f_{OSC}/12$
0	1	1	8-bit UART	variable
1	0	2	9-bit UART	$f_{OSC}/64$ or $f_{OSC}/32$
1	1	3	9-bit UART	variable

Symbol	Function
SM2	Enables the Automatic Address Recognition feature in Modes 2 or 3. If SM2 = 1 then Rl will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In Mode 1, if SM2 = 1 then Rl will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in Modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In Mode 1, if SM2 = 0, RB8 is the stop bit that was received. In Mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in Mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

NOTE:
**f_{OSC} = oscillator frequency

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Figure 5. SCON: Serial Port Control Register

Interrupt Priority Structure

The 89C535/536/538 has a 6-source two-level interrupt structure (see Table 7). There are 2 SFRs associated with the interrupts on the 89C535/536/538. They are the IE and IP. (See Figures 6 and 7.)

The function of the IPH SFR is simple and when combined with the IP SFR determines the priority of each interrupt. The priority of each interrupt is determined as shown in the following table:

PRIORITY BITS	INTERRUPT PRIORITY LEVEL
IP.x	
0	Level 0 (lowest priority)
1	Level 1 (highest priority)

An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

Table 7. Interrupt Table

SOURCE	POLLING PRIORITY	REQUEST BITS	HARDWARE CLEAR?	VECTOR ADDRESS
X0	1	IE0	N (L)[1] Y (T)[2]	03H
T0	2	TP0	Y	0BH
X1	3	IE1	N (L) Y (T)	13H
T1	4	TF1	Y	1BH
SP	5	R1, TI	N	23H
T2	6	TF2, EXF2	N	2BH

NOTES:
1. L = Level activated
2. T = Transition activated

IE (0A8H)

7	6	5	4	3	2	1	0
EA	—	ET2	ES	ET1	EX1	ET0	EX0

Enable Bit = 1 enables the interrupt.
Enable Bit = 0 disables it.

BIT	SYMBOL	FUNCTION
IE.7	EA	Global disable bit. If EA = 0, all interrupts are disabled. If EA = 1, each interrupt can be individually enabled or disabled by setting or clearing its enable bit.
IE.6	—	Not implemented.
IE.5	ET2	Timer 2 interrupt enable bit.
IE.4	ES	Serial Port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt 1 enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt 0 enable bit.

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Figure 6. IE Registers

IP (0B8H)

7	6	5	4	3	2	1	0
—	—	PT2	PS	PT1	PX1	PT0	PX0

Priority Bit = 1 assigns higher priority
Priority Bit = 0 assigns lower priority

BIT	SYMBOL	FUNCTION
IP.7	—	Not implemented, reserved for future use.
IP.6	—	Not implemented, reserved for future use.
IP.5	PT2	Timer 2 interrupt priority bit.
IP.4	PS	Serial Port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt 1 priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt 0 priority bit.

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Figure 7. IP Registers

Expanded Data RAM Addressing

The 89C535/536/538 has internal data memory that is mapped into four separate segments: the lower 128 bytes of RAM, upper 128 bytes of RAM, 128 bytes Special Function Register (SFR), and 256 bytes expanded RAM (ERAM).

The four segments are:

1. The Lower 128 bytes of RAM (addresses 00H to 7FH) are directly and indirectly addressable.
2. The Upper 128 bytes of RAM (addresses 80H to FFH) are indirectly addressable only.
3. The Special Function Registers, SFRs, (addresses 80H to FFH) are directly addressable only.
4. The 256-bytes expanded RAM (ERAM, 00H – FFH) are indirectly accessed by move external instruction, MOVX.

The Lower 128 bytes can be accessed by either direct or indirect addressing. The Upper 128 bytes can be accessed by indirect addressing only. The Upper 128 bytes occupy the same address space as the SFRs. That means they have the same address, but are physically separate from SFR space.

When an instruction accesses an internal location above address 7FH, the CPU knows whether the access is to the upper 128 bytes of data RAM or to SFR space by the addressing mode used in the instruction. Instructions that use direct addressing access SFR space. For example:

MOV 0A0H,#data

accesses the SFR at location 0A0H (which is P2). Instructions that use indirect addressing access the Upper 128 bytes of data RAM.

For example:

MOV @R0,#data

where R0 contains 0A0H, accesses the data byte at address 0A0H, rather than P2 (whose address is 0A0H).

The ERAM can be accessed by indirect addressing and MOVX instructions. This part of memory is physically located on-chip, logically occupies the first 256-bytes of external data memory.

The ERAM is indirectly addressed, using the MOVX instruction in combination with any of the registers R0, R1 of the selected bank or DPTR. An access to ERAM will not affect ports P0, P3.6 (WR#) and P3.7 (RD#). P2 SFR is output during external addressing.
For example,

MOVX @R0,#data

where R0 contains 0A0H, accesses the ERAM at address 0A0H rather than external memory. An access to external data memory locations higher than FFH (i.e., 0100H to FFFFH) will be performed with the MOVX DPTR instructions in the same way as in the standard 80C51, so with P0 and P2 as data/address bus, and P3.6 and P3.7 as write and read timing signals. Refer to Figure 8.

External data memory cannot be accessed using the MOVX with R0 or R1. This will always access the ERAM.

The stack pointer (SP) may be located anywhere in the 256 bytes RAM (lower and upper RAM) internal data memory. The stack may not be located in the ERAM.

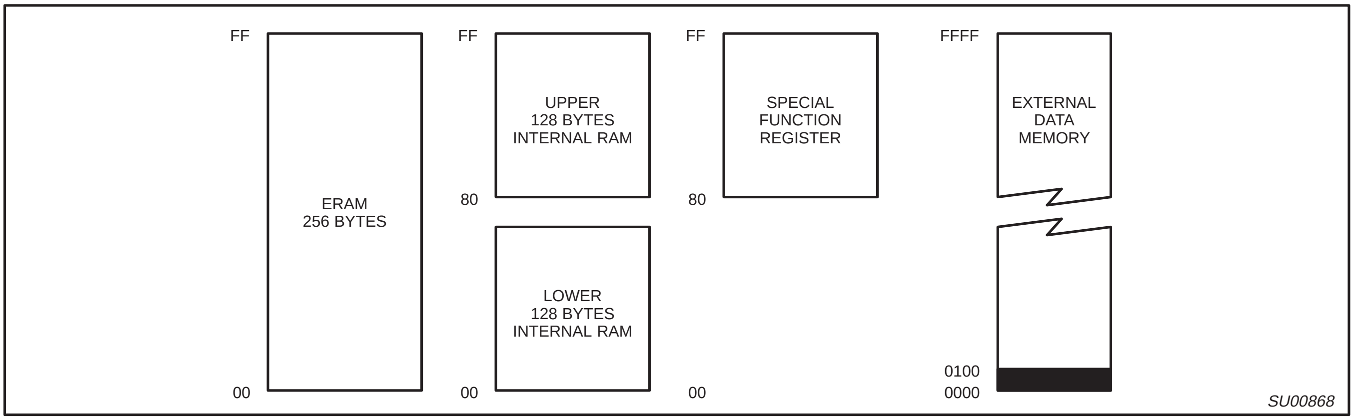


Figure 8. Internal and External Data Memory Address Space

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Operating temperature under bias	0 to +70	°C
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ pin to V_{SS}	0 to +13.0	V
Voltage on any other pin to V_{SS}	–0.5 to +6.5	V
Maximum I_{OL} per I/O pin	15	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C; 5V ±10%; V_{SS} = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{IL}	Input low voltage	4.5V < V_{CC} < 5.5V	–0.5	0.2V_{CC}–0.1	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)		0.2V_{CC}+0.9	V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST		0.7V_{CC}	V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, 3 [6]	V_{CC} = 4.5V I_{OL} = 1.6mA[1]		0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$ [5, 6]	V_{CC} = 4.5V I_{OL} = 3.2mA[1]		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [2]	V_{CC} = 4.5V I_{OH} = –30µA	V_{CC} – 0.7		V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[7], $\overline{PSEN}$[2]	V_{CC} = 4.5V I_{OH} = –800µA	V_{CC} – 0.7		V
I_{IL}	Logical 0 input current, ports 1, 2, 3	V_{IN} = 0.4V	–1	–50	µA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3	V_{IN} = 2.0V See note 3		–650	µA
I_{LI}	Input leakage current, port 0	0.45 < V_{IN} < V_{CC} – 0.3		±10	µA
I_{CC}	Power supply current (see Figure 16): Active mode Idle mode Power-down mode or clock stopped (see Figure 20 for conditions)	See note 4 V_{CC} = 5.5V FREQ = 24 MHz T_{amb} = 0°C to 70°C		 60 25 100	 mA mA µA
R_{RST}	Internal reset pull-down resistor		40	225	kΩ

NOTES:

1. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
2. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the V_{CC}–0.7 specification when the address bits are stabilizing.
3. Pins of ports 1, 2 and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
4. See Figures 17 through 20 for I_{CC} test conditions.
   Active mode: $I_{CC(MAX)}$ = 0.9 × FREQ. + 1.1mA
   Idle mode: $I_{CC(MAX)}$ = 0.18 × FREQ. +1.0mA; See Figure 16.
5. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 15mA
   Maximum I_{OL} per 8-bit port: 26mA
   Maximum total I_{OL} for all outputs: 71mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
7. ALE is tested to V_{OH1}, except when ALE is off then V_{OH} is the voltage specification.
8. Pin capacitance is characterized but not tested. Pin capacitance is less than 25pF. Pin capacitance of ceramic package is less than 15pF (except $\overline{EA}$ is 25pF).

AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V[1, 2, 3]

SYMBOL	FIGURE	PARAMETER	VARIABLE CLOCK		33MHz CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	9	Oscillator frequency Speed versions : N (33MHz)	3.5	33	3.5	33	MHz
t_{LHLL}	9	ALE pulse width	$2t_{CLCL}-40$		21		ns
t_{AVLL}	9	Address valid to ALE low	$t_{CLCL}-25$		5		ns
t_{LLAX}	9	Address hold after ALE low	$t_{CLCL}-25$		5		ns
t_{LLIV}	9	ALE low to valid instruction in		$4t_{CLCL}-65$		55	ns
t_{LLPL}	9	ALE low to $\overline{PSEN}$ low	$t_{CLCL}-25$		5		ns
t_{PLPH}	9	$\overline{PSEN}$ pulse width	$3t_{CLCL}-45$		45		ns
t_{PLIV}	9	$\overline{PSEN}$ low to valid instruction in		$3t_{CLCL}-60$		30	ns
t_{PXIX}	9	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	9	Input instruction float after $\overline{PSEN}$		$t_{CLCL}-25$		5	ns
t_{AVIV}	9	Address to valid instruction in		$5t_{CLCL}-80$		70	ns
t_{PLAZ}	9	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{RLRH}	10, 11	$\overline{RD}$ pulse width	$6t_{CLCL}-100$		82		ns
t_{WLWH}	10, 11	$\overline{WR}$ pulse width	$6t_{CLCL}-100$		82		ns
t_{RLDV}	10, 11	$\overline{RD}$ low to valid data in		$5t_{CLCL}-90$		60	ns
t_{RHDX}	10, 11	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	10, 11	Data float after $\overline{RD}$		$2t_{CLCL}-28$		32	ns
t_{LLDV}	10, 11	ALE low to valid data in		$8t_{CLCL}-150$		90	ns
t_{AVDV}	10, 11	Address to valid data in		$9t_{CLCL}-165$		105	ns
t_{LLWL}	10, 11	ALE low to $\overline{RD}$ or $\overline{WR}$ low	$3t_{CLCL}-50$	$3t_{CLCL}+50$	40	140	ns
t_{AVWL}	10, 11	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	$4t_{CLCL}-75$		45		ns
t_{QVWX}	10, 11	Data valid to $\overline{WR}$ transition	$t_{CLCL}-30$		0		ns
t_{WHQX}	10, 11	Data hold after $\overline{WR}$	$t_{CLCL}-25$		5		ns
t_{QVWH}	11	Data valid to $\overline{WR}$ high	$7t_{CLCL}-130$		80		ns
t_{RLAZ}	10, 11	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	10, 11	$\overline{RD}$ or $\overline{WR}$ high to ALE high	$t_{CLCL}-25$	$t_{CLCL}+25$	5	55	ns
External Clock							
t_{CHCX}	13	High time	17	$t_{CLCL}-t_{CLCX}$			ns
t_{CLCX}	13	Low time	17	$t_{CLCL}-t_{CHCX}$			ns
t_{CLCH}	13	Rise time		5			ns
t_{CHCL}	13	Fall time		5			ns
Shift Register							
t_{XLXL}	12	Serial port clock cycle time	$12t_{CLCL}$		360		ns
t_{QVXH}	12	Output data setup to clock rising edge	$10t_{CLCL}-133$		167		ns
t_{XHQX}	12	Output data hold after clock rising edge	$2t_{CLCL}-80$		50		ns
t_{XHDX}	12	Input data hold after clock rising edge	0		0		ns
t_{XHDV}	12	Clock rising edge to input data valid		$10t_{CLCL}-133$		167	ns

NOTES:
1. Parameters are valid over operating temperature range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. Interfacing the microcontroller to devices with float times up to 45ns is permitted. This limited bus contention will not cause damage to Port 0 drivers.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always ‘t’ (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

A – Address
C – Clock
D – Input data
H – Logic level high
I – Instruction (program memory contents)
L – Logic level low, or ALE
P – $\overline{PSEN}$
Q – Output data
R – $\overline{RD}$ signal
t – Time
V – Valid
W – $\overline{WR}$ signal
X – No longer a valid logic level
Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.
t_{LLPL} =Time for ALE low to $\overline{PSEN}$ low.

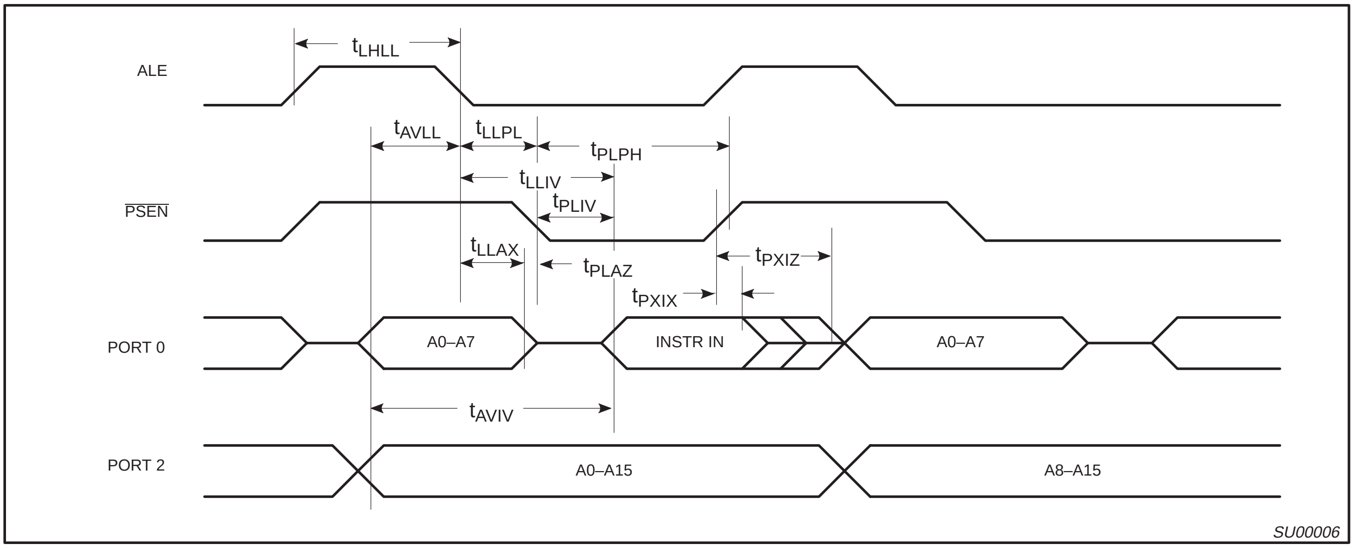


Figure 9. External Program Memory Read Cycle

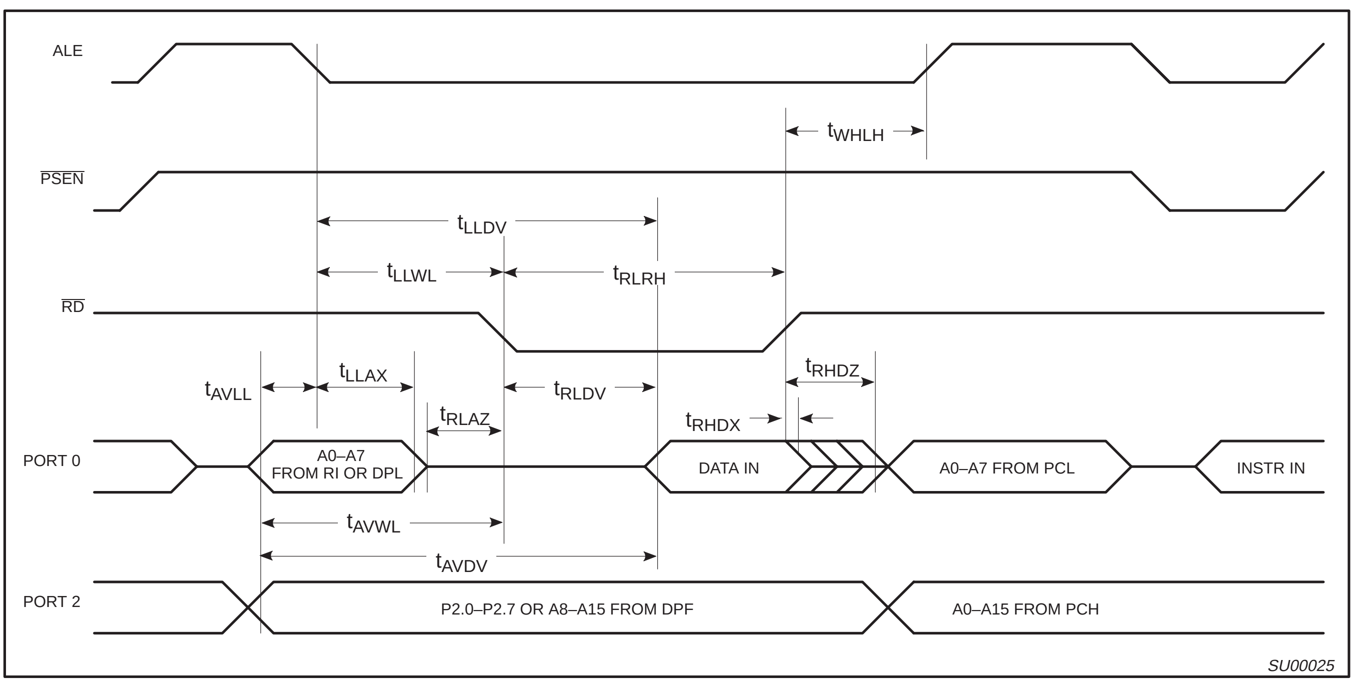


Figure 10. External Data Memory Read Cycle

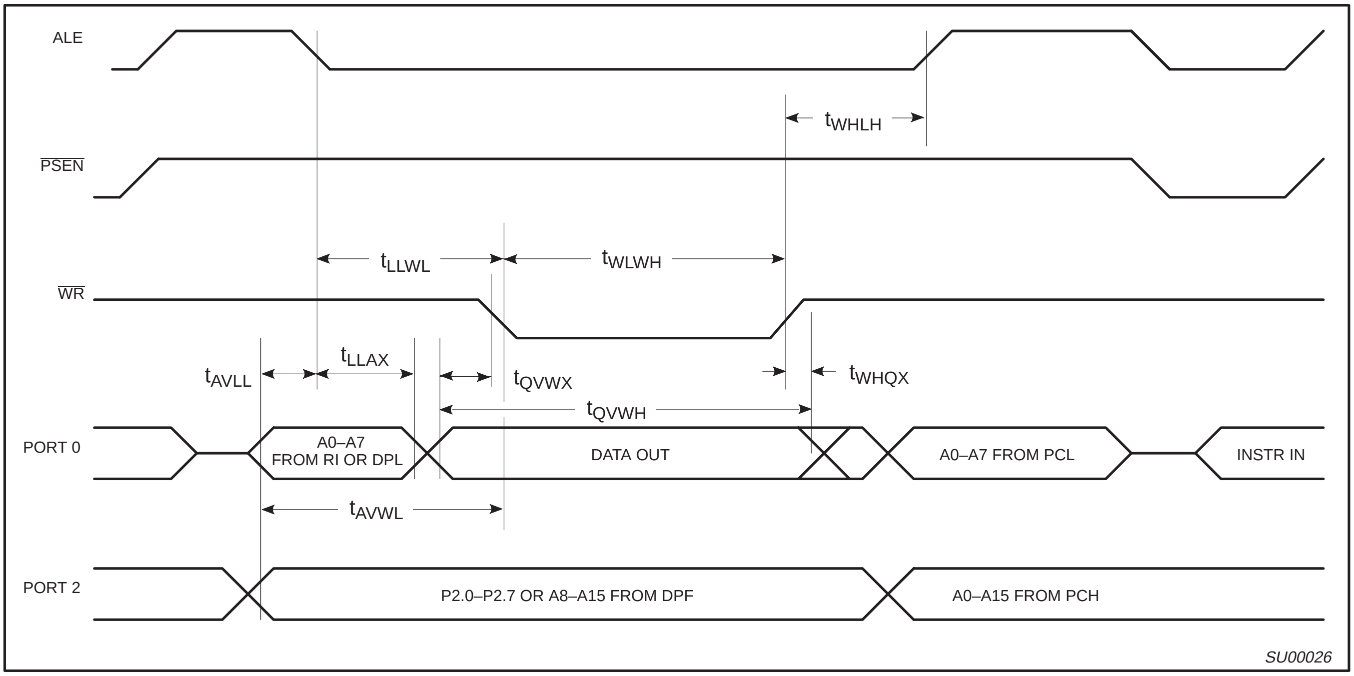


Figure 11. External Data Memory Write Cycle

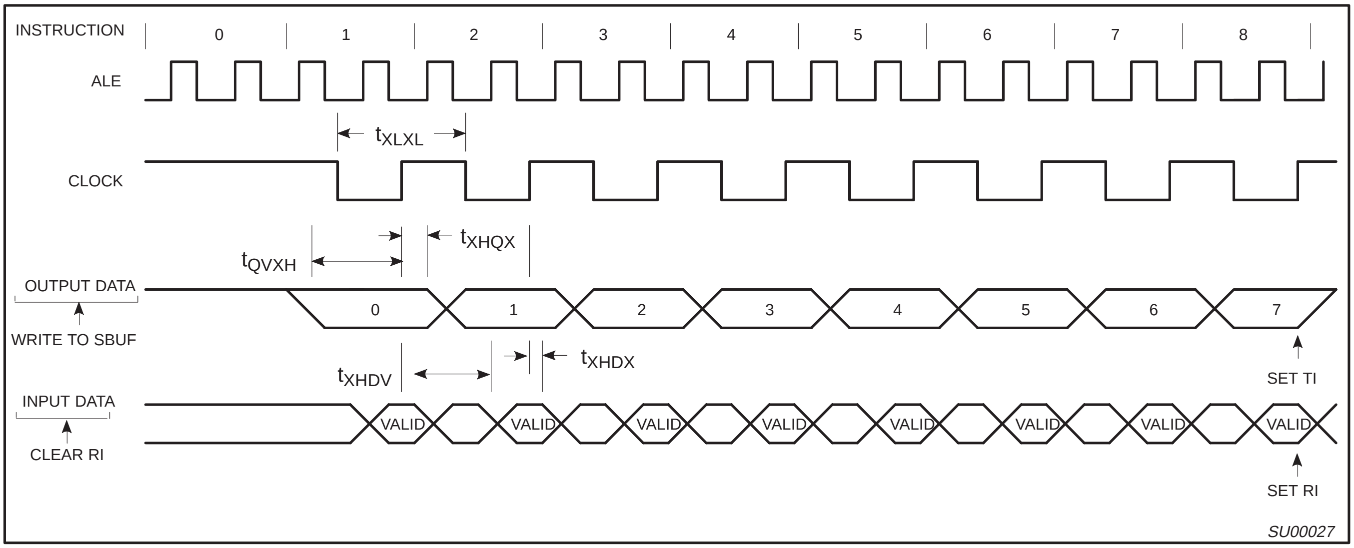


Figure 12. Shift Register Mode Timing

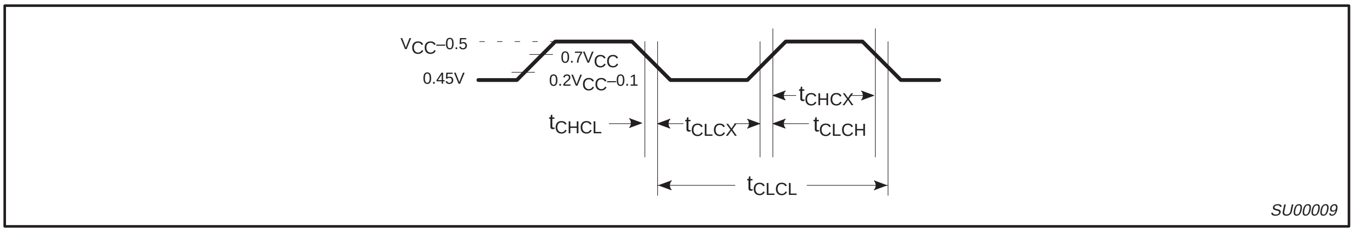
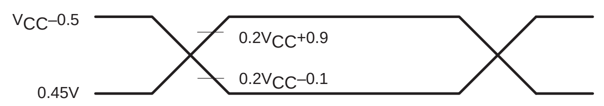


Figure 13. External Clock Drive



NOTE:
AC inputs during testing are driven at V_{CC} –0.5 for a logic '1' and 0.45V for a logic '0'. Timing measurements are made at V_{IH} min for a logic '1' and V_{IL} max for a logic '0'.

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Figure 14. AC Testing Input/Output

NOTE:
For timing purposes, a port is no longer floating when a 100mV change from load voltage occurs, and begins to float when a 100mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OH}/I_{OL} \geq \pm$20mA.

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Figure 15. Float Waveform

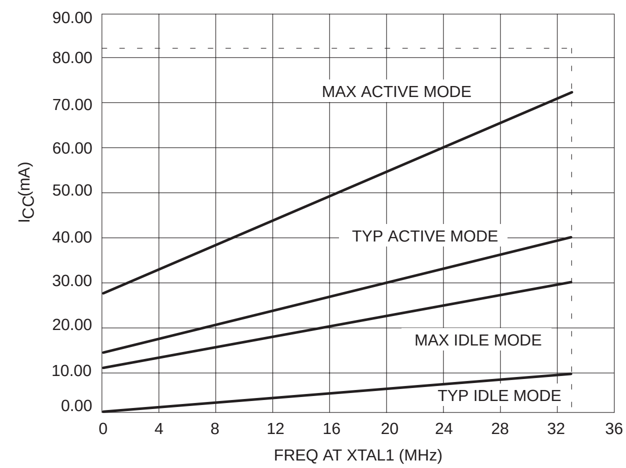

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Figure 16. I_{CC} vs. FREQ Valid only within frequency specifications of the device under test

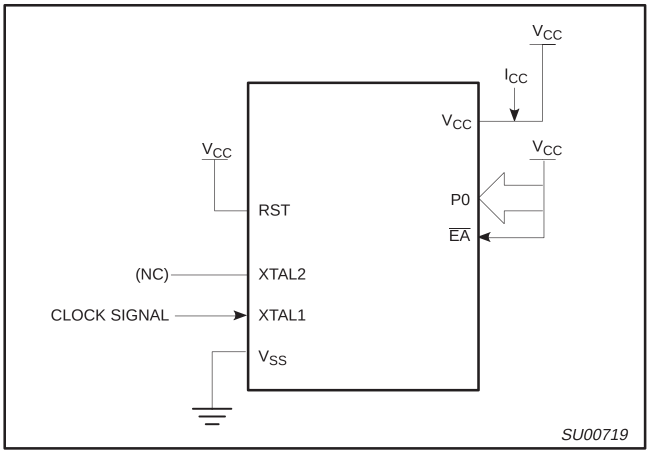


Figure 17. I_{CC} Test Condition, Active Mode
All other pins are disconnected

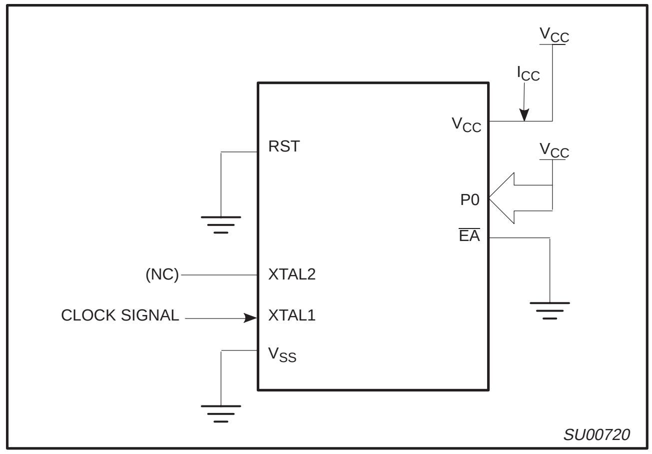


Figure 18. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

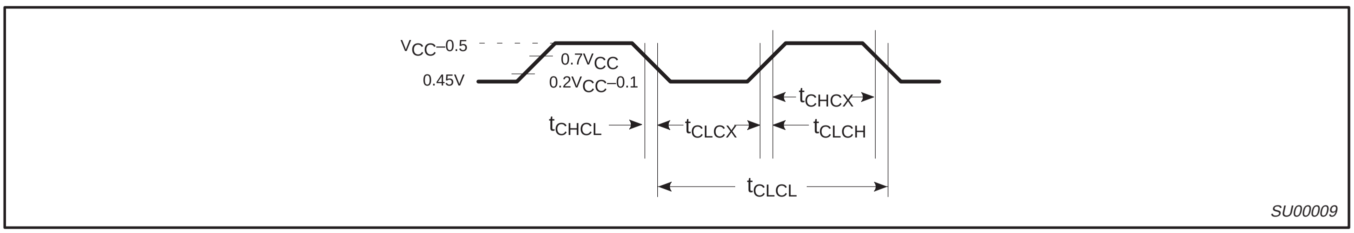


Figure 19. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

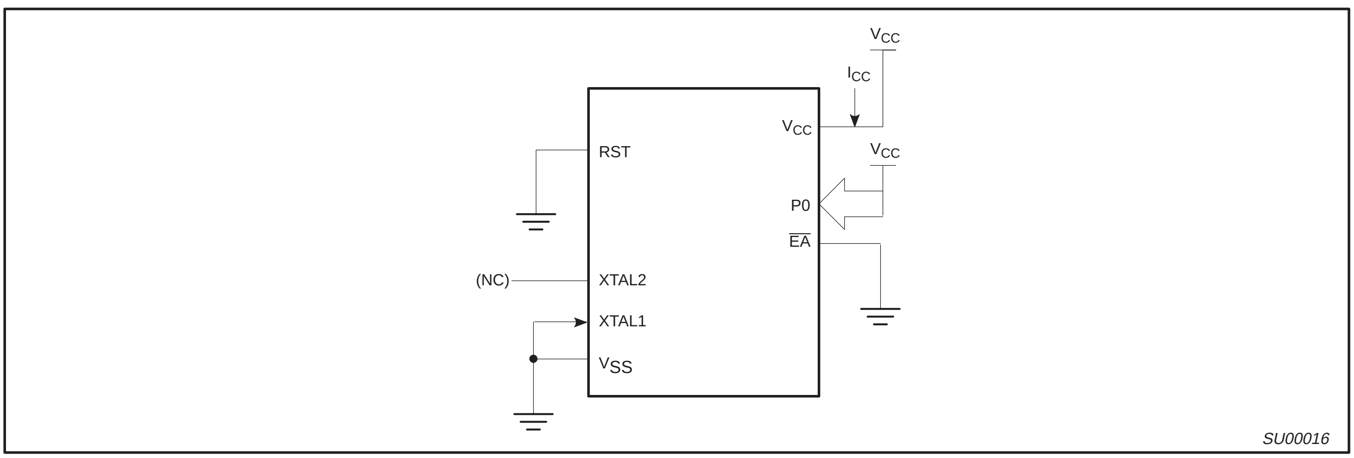


Figure 20. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected. V_{CC} = 2V to 5.5V

FLASH EPROM PROGRAM MEMORY

FEATURES

- 8K (89C535), 16K (89C536), 64K (89C538) or electrically erasable internal program.
- Up to 64 Kilobyte external program memory if the internal program memory is switched off ($\overline{EA}$ = 0)..
- Programming and erasing voltage 12V ±5%
- Command register architecture
  - Byte Programming (10 us typical)
  - Auto chip erase 5 seconds typical (including preprogramming time)
- Auto Erase and auto program
  - $\overline{DATA}$ polling
  - Toggle bit
- 100 minimum erase/program cycles
- Advanced CMOS FLASH EPROM memory technology

GENERAL DESCRIPTION

The 89C535/536/538 FLASH EPROM memory augments EPROM functionality with In–circuit electrical erasure and programming. The 89C535/536/538 uses a command register to manage this functionality.

The FLASH EPROM reliably stores memory contents even after 100 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The 89C535/536/538 uses a 12.0V ±5%V_{PP} supply to perform the Auto Program/Erase algorithms.

Automatic Programming

The 89C535/536/538 is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical room temperature chip programming time of the 89C535/536/538 is less than 5 seconds.

Automatic Chip Erase

The device may be erased using the automatic Erase algorithm. The automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device.

Automatic Programming Algorithm

The 89C535/536/538 automatic Programming algorithm requires the user to only write a program set–up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify, and counts the number of sequences. A status bit similar to $\overline{DATA}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC ERASE ALGORITHM

The 89C535/536/538 Automatic Erase algorithm requires the user to only write an erase set–up command and erase command. The device will automatically pre–program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify, and counts the number of sequences. A status bit similar to $\overline{DATA}$ polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the erase operation.

Commands are written to the command register. Register contents serve as inputs to an internal state–machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the 89C535/536/538 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin through the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

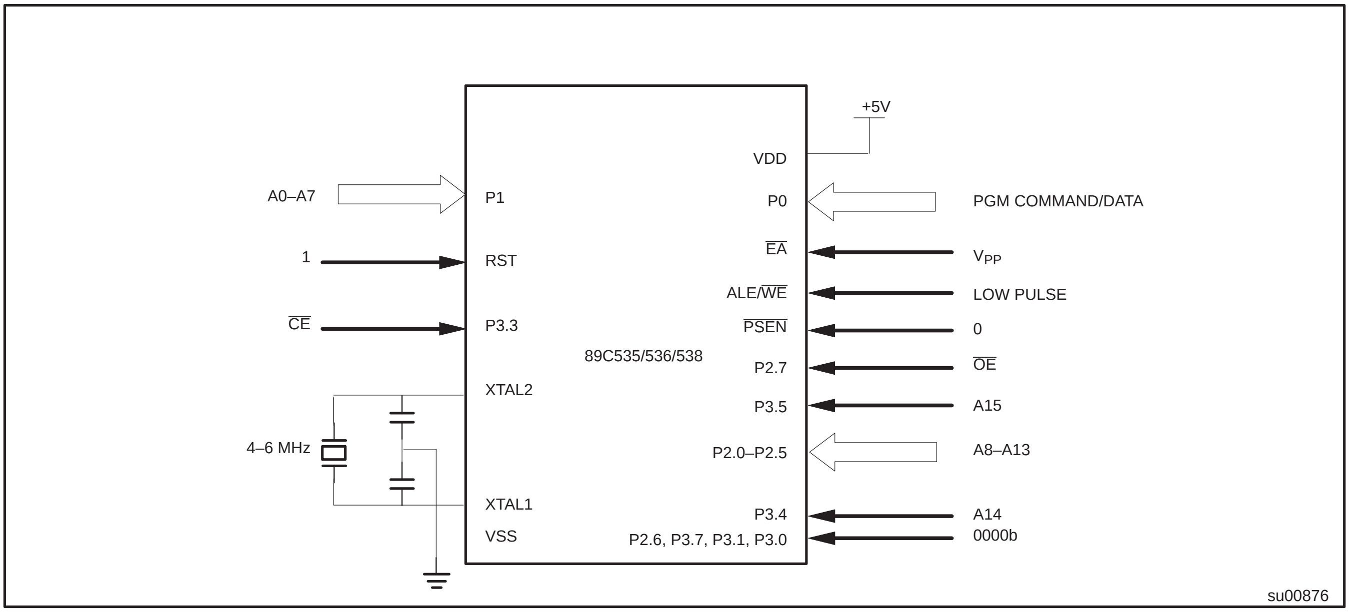


Figure 21. Erase/Programming/Verification

Table 8. Pin Description

PIN NAME	SYMBOL	FUNCTION
P1.0–P1.7 P2.0–P2.5, P3.4, P3.5	A0–A7 A8–A13, A14–A15	Input Low Order Address Bits Input High Order Address Bits
P0.0–P0.7	Q0–Q7	Data Input/Output
P3.3	$\overline{CE}$	Chip Enable Input
P2.7	$\overline{OE}$	Output Enable Input
ALE/$\overline{WE}$	$\overline{WE}$	Write Enable Pin
$\overline{EA}$	V_{PP}	Program Supply Voltage
P2.6, P3.7, P3.1, P3.0	FTEST3–FTEST0	Flash Test Mode Selection
V_{CC}	V_{CC}	Power Supply Voltage (+5V)
GND	GND	Ground Pin

Table 9. Command Definitions

COMMAND	BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Setup auto erase/auto erase (chip)	2	Write	X	30H	Write	X	30H
Setup auto program/program	2	Write	X	40H	Write	PA	PD
Reset	2	Write	X	FFH	Write	X	FFH

Note:
- PA = Address of memory location to be programmed
- PD = Data to be programmed at location

Command Definitions

When low voltage is applied to the V_{PP} pin, the contents of the command register default to 00H. Placing high voltage on the V_{PP} pin enables read/write operations. Device operations are selected by writing specific data patterns into the command register. Table 2 defines these 89C535/536/538 register commands. Table 3 defines the bus operations of 89C535/536/538.

Table 10.

OPERATION		V_{PP}(1)	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	D00–D07
READ/WRITE	Read(2)	V_{PPH}	V_{IL}	V_{IL}	V_{IH}	DATA OUT(3)
	Standby(4)	V_{PPH}	V_{IH}	X	X	Tri–State
	Write	V_{PPH}	V_{IL}	V_{IH}	V_{IL}	Data In(5)

NOTES:
1. V_{PPH} is the programming voltage specified for the device.
2. Read operation withVPP = V_{PPH} may access array data (if write command is preceded) or silicon ID codes.
3. With V_{PP} at high voltage, the standby current equals I_{CC}+I_{PP} (standby).
4. Refer to Table 38 for valid Data–In during a write operation.
5. X can be V_{IL} or V_{IH}.

Set–Up Automatic Chip Erase/Erase Commands

The automatic chip erase does not require the device to be entirely pre–programmed prior to executing the Automatic set–up erase command and automatic chip erase command. Upon executing the Automatic chip erase command, the device automatically will program and verify the entire memory for an all–zero data pattern. When the device is automatically verified to contain an all–zero pattern, a self–timed chip erase and verify begins. The erase and verify operations are complete when the data on DQ7 is"1" at which time the device returns to the standby mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Automatic set–up erase command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Automatic set–up erase is performed by writing 30H to the command register.

To command automatic chip erase, the command 30H must be written again to the command register. The automatic chip erase begins on the rising edge of the WE and terminates when the data on DQ7 is "1 " and the data on DQ6 stops toggling for two consecutive read cycles, at which time the device returns to the standby mode.

Set–Up Automatic Program/Program Commands

The Automatic Set–up Program is a command–only operation that stages the devices for automatic programming. Automatic Set–up Program is performed by writing 40H to the command register.

Once the Automatic Set–up Program operation is performed, the next WE pulse causes a transition to an active programming operation. Addresses are internally latched on the falling edge of the WE pulse. Data is internally latched on the rising edge of the WE pulse. The rising edge of WE also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data read on DQ6 stops toggling for two consecutive read cycles and the data on DQ7 and DQ6 are equivalent to data written to these two bits at which time the device returns to the Read mode (no program verify command is required; but data can be read out if OE is active low).

Reset Command

A reset command is provided as a means to safely abort the erase– or program–command sequences. Following either set–up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. Should program–fail or erase–fail happen, two consecutive writes of FFH will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

Write Operation Status

Toggle Bit–DQ6

The 89C535/536/538 features a "Toggle Bit" as a method to indicate to the host system that the Auto Program/Erase algorithms are either in progress or completed.

While the Automatic Program or Erase algorithm is in progress, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Automatic Program or Erase algorithm is completed, DQ6 will stop toggling and valid data will be read. The toggle bit is valid after the rising edge of the second WE pulse of the two write pulse sequences.

Data Polling–D07

The 89C535/536/538 also features DATA Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation an attempt to read the device will produce the complement data of the data last written to DQ7. Upon completion of the Automatic Program algorithm an attempt to read the device will produce the true data last written to DQ7. The Data Polling feature is valid after the rising edge of the second WE pulse of the two write pulse sequences.

While the Automatic Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The DATA Polling feature is valid after the rising edge of the second WE pulse of two writes pulse sequences.

The DATA Polling feature is active during Automatic Program/Erase algorithms.

Write Operation

The data to be programmed into Flash should be inverted when programming. In other words to program the value '00', 'FF' should be applied to port P0.

System Considerations

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and GND, and between V_{PP} and GND to minimize transient effects.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
C_{IN}	V_{PPH}			14	PF	VI_N = 0V
C_{OUT}	V_{PPH}			16	pF	V_{OUT} = 0V

Command programming/Data programming/Erase Operation

DC CHARACTERISTICS

T_{amb} = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{PP} = 12.0V ± 5%

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			10	µA
I_{SB1}	Standby V_{CC} Current	$\overline{CE}$ = VI_H			1	mA
I_{SB2}		$\overline{CE}$ = V_{CC} ± 0.3 V		1	100	µA
I_{CC1} (Read)	Operating V_{CC} Current	I_{OUT} = 0 mA, f=1 MHz			30	mA
I_{CC2}		I_{OUT} = 0 mA, F=11MHz			50	mA
I_{CC3} (Program)		In Programming			50	mA
I_{CC4} (Erase)		In Erase			50	mA
I_{CC5} (Program Verify)		In Program Verify			50	mA
I_{CC6} (Erase Verify)		In erase Verify			50	mA
I_{PP1} (Read)	V_{PP} Current	V_{PP}=12.6 V			100	µA
I_{PP2} (Program)		In Programming			50	mA
I_{PP3} (Erase)		In Erase			50	mA
I_{PP4} (Program Verify)		In Program Verify			50	mA
I_{PP5} (Erase Verify)		In Erase Verify			50	mA
V_{IL}	Input Voltage		–0.5 (Note 5)		$0.2V_{PP}$ – 0.3	V
V_{IH}			2.4		V_{CC}+0.3V (Note 6)	V
V_{OL}	Output Voltage Low	I_{OL}=2.1mA			0.45	V
V_{OH}	Output Voltage High	I_{OH}=400uA	2.4			V

NOTES:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 14V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12V.
4. Do not alter V_{PP} from V_{IL} to 12V or 12V to V_{IL} when $\overline{CE}$=V_{IL}
5. V_{IL} min. = –0.5V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.
7. All currents are in RMS unless otherwise noted. (Sampled, not 100% tested.).

AC CHARACTERISTICS

T_{amb} = 0°C to 70°C, V_{CC} = 5V ± 10%, V_{PP} = 12V ± 5%

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
τ_{VPS}	V_{PP} setup time		100		ns
τ_{OES}	OE setup time		100		ns
τ_{CWC}	Command programming cycles		150		ns
τ_{CEP}	WE programming pulse width		60		ns
τ_{EPH1}	WE programming pulse width High		20		ns
τ_{CEPH2}	WE programming pulse width High		100		ns
τ_{AS}	Address setup time		0		ns
τ_{AH1}	Address hold time for DATA Polling		0		ns
τ_{DS}	DATA setup time		50		ns
τ_{DH}	DATA hold time		10		ns
τ_{CESP}	CE setup time before DATA polling/toggle bit		100		ns
τ_{CES}	CE setup time		0		ns
τ_{CESC}	CE setup time before command write		100		ns
τ_{VPH}	V_{PP} hold time		100		ns
τ_{DF}	Output disable time (Note 2)			35	ns
τ_{DPA}	DATA polling/toggle bit access time			150	ns
τ_{AETC}	Total erase time in auto chip erase			5(TYP)	s
τ_{AVT}	Total programming time in auto verify		15	300	μs

NOTES:
1. $\overline{CE}$ and $\overline{OE}$ must be fixed high during V_{PP} transition from 5V to 12V or from 12V to 5V.
2. τ_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Timing Waveform

Automatic Programming

One byte of data is programmed. Verifying in fast algorithm and additional programming by external control are not required because these operations are executed automatically by an internal control circuit. Programming completion can be verified by $\overline{\text{DATA}}$ polling and toggle bit checking after automatic verify starts. Device outputs $\overline{\text{DATA}}$ during programming and DATA after programming on Q7. Q0 to Q5(Q6 is for toggle bit; see toggle bit, $\overline{\text{DATA}}$ polling, timing waveform) are in high impedance.

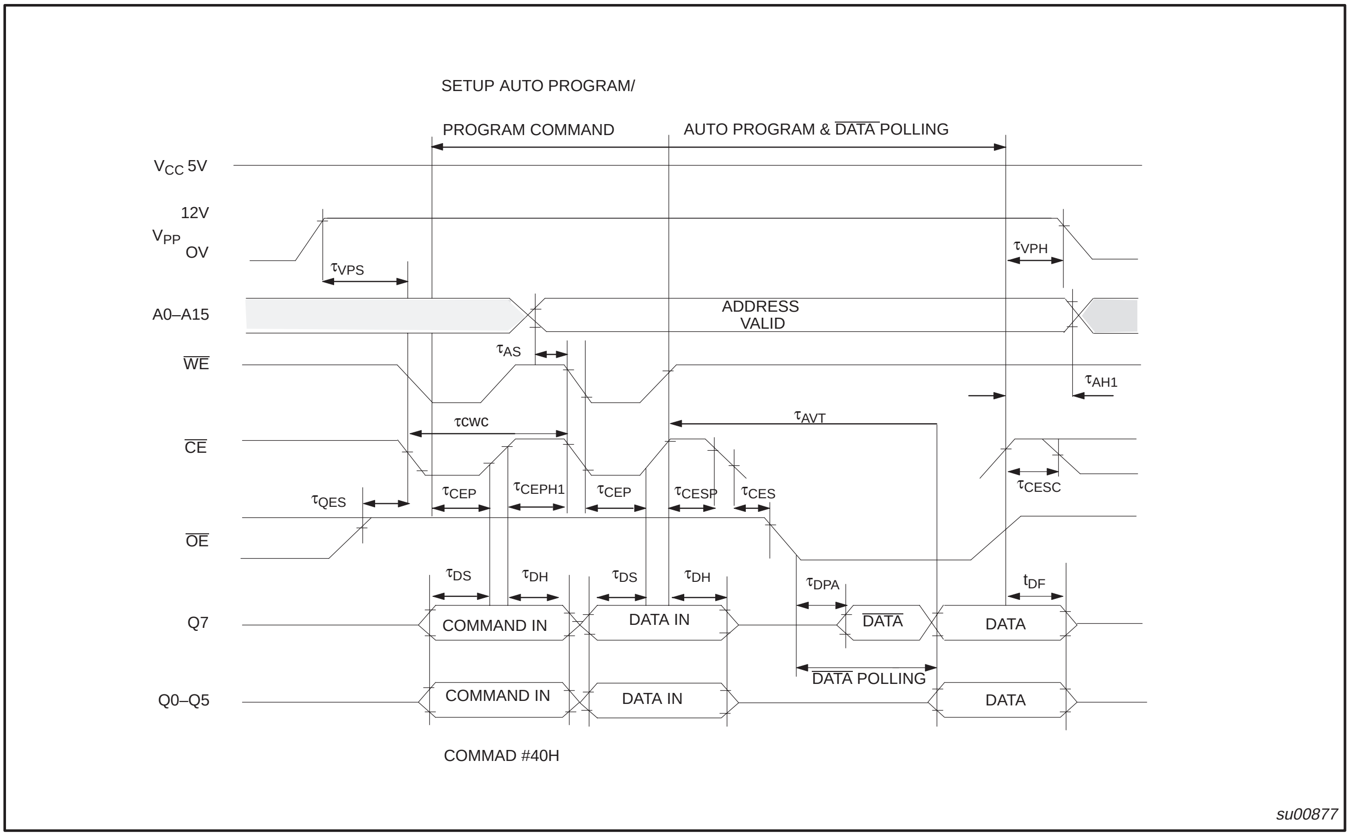


Figure 22. Automatic Programming Timing Waveform

AUTOMATIC CHIP ERASE

All data in the FLASH memory is erased. External erase verification is not required. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7, Q0 to Q5 (Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform) are in high impedance.

RESET

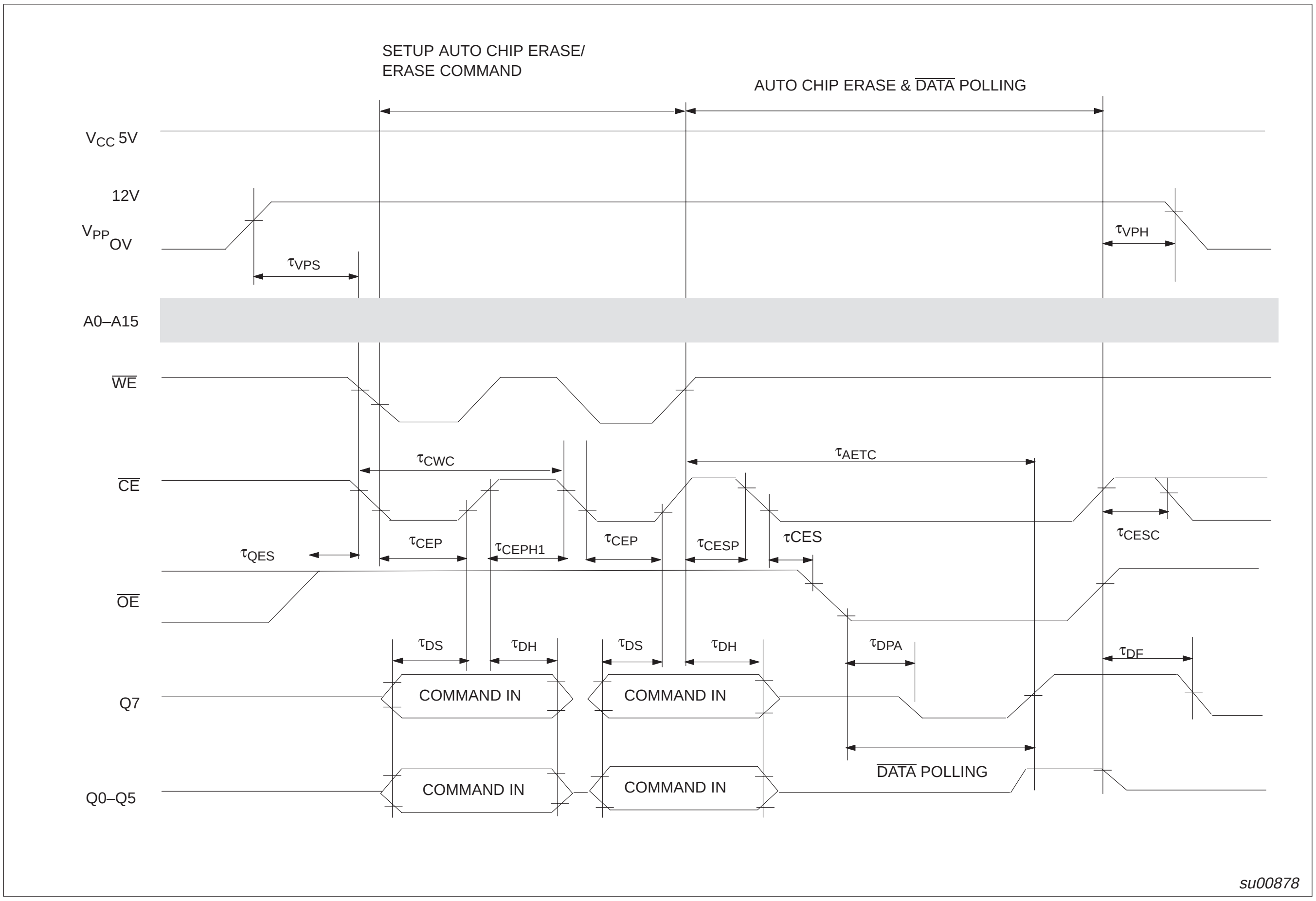


Figure 23. Automatic Chip Erase Timing Waveform

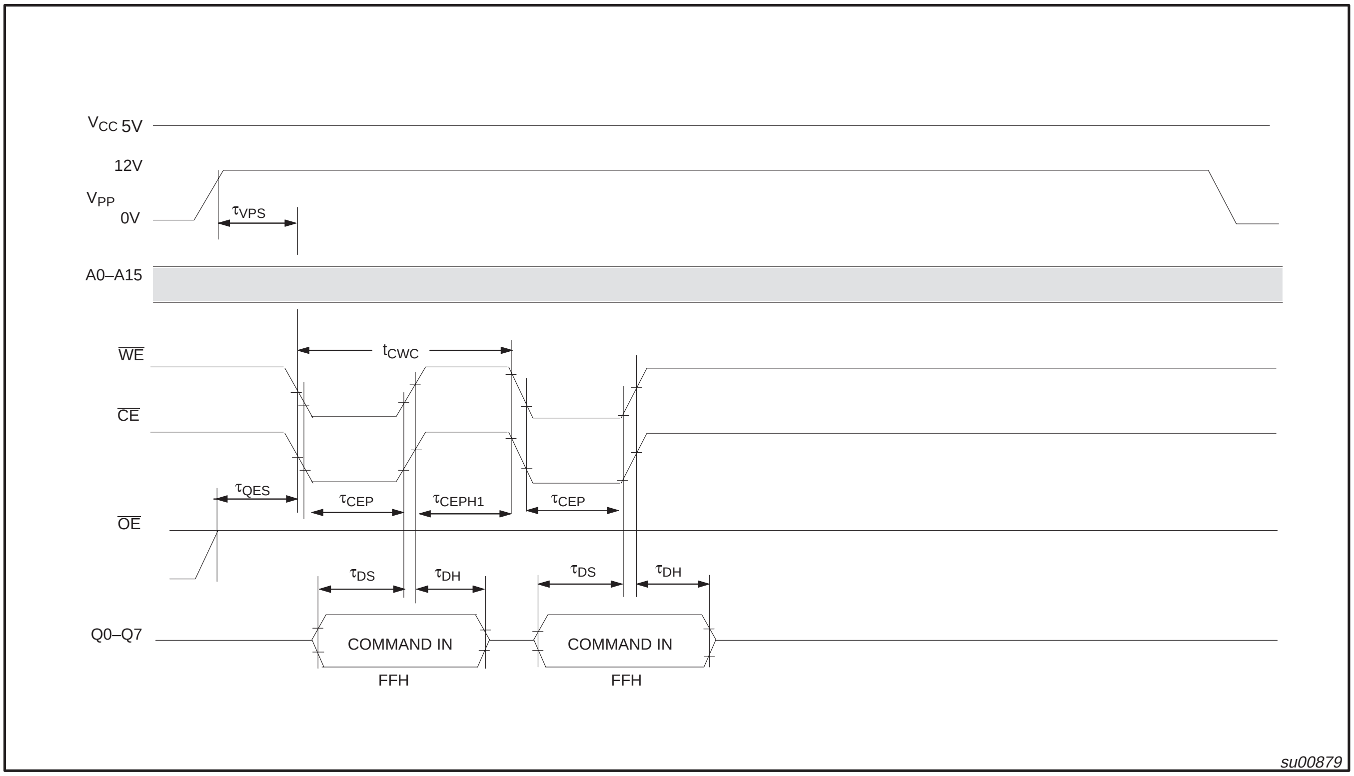


Figure 24. Reset Timing Waveform

Toggle Bit, Data Polling

Toggle bit appears in Q6, when program/erase is operating. DATA polling appears in Q7 during programming or erase.

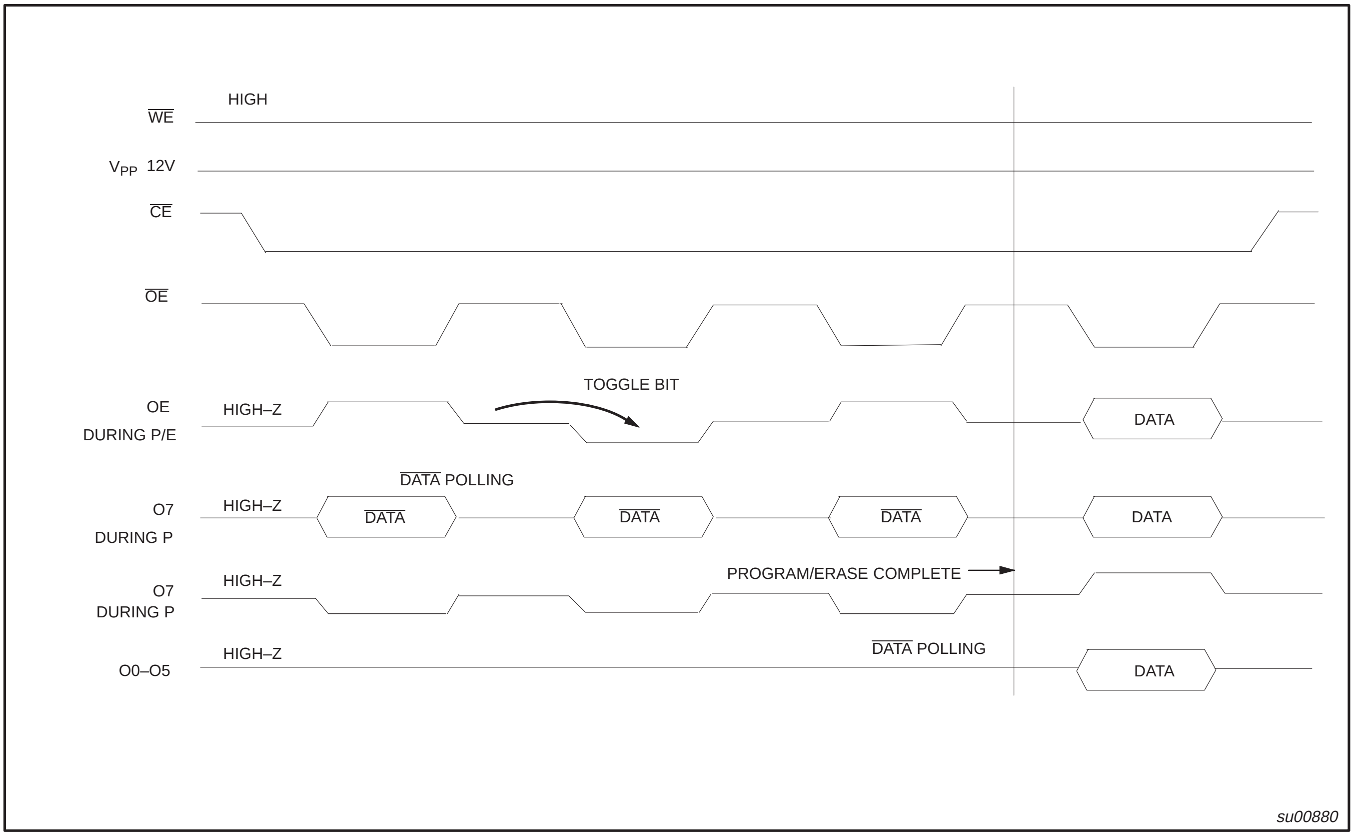
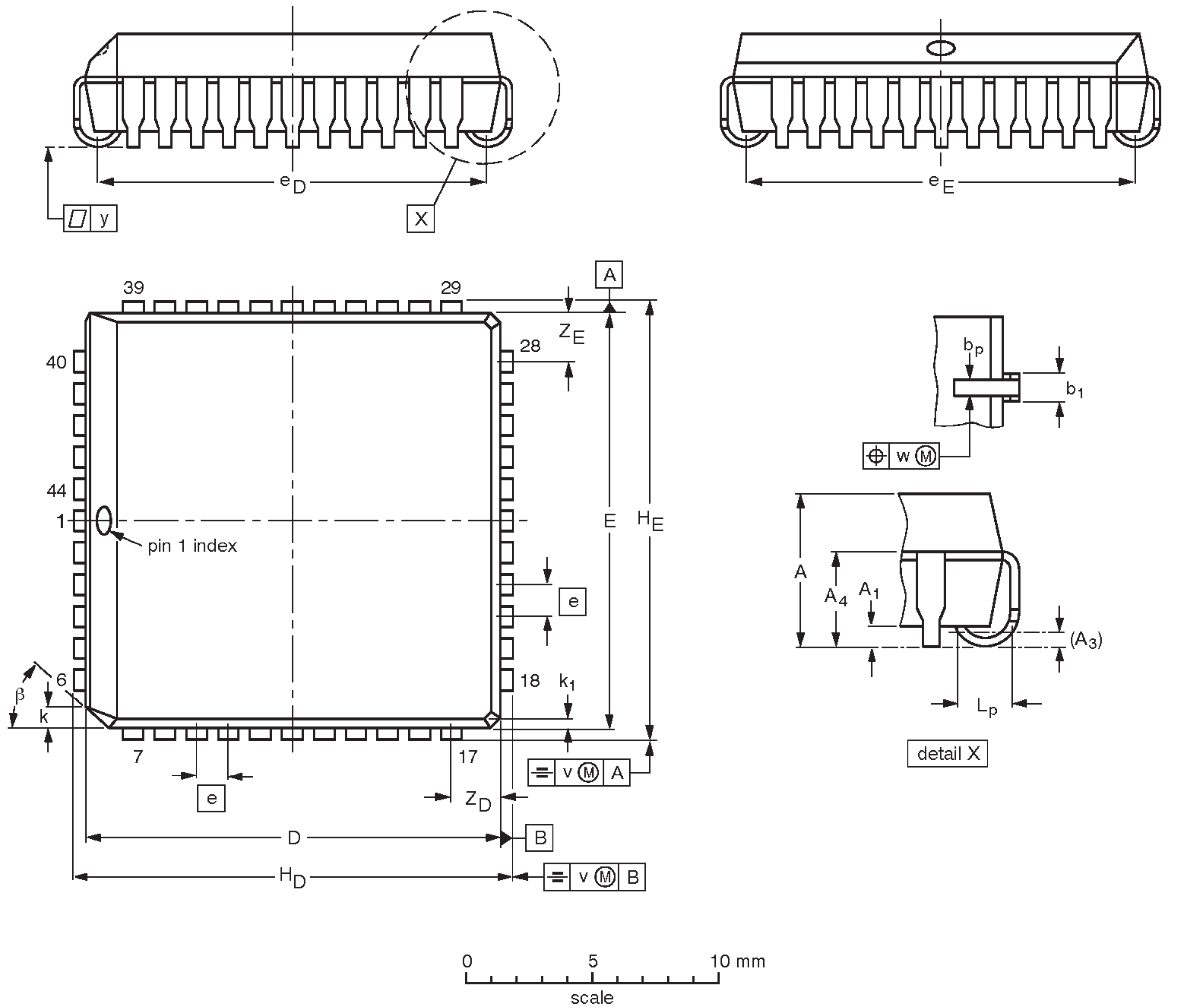


Figure 25. Toggle Bit, Data Polling Timing Waveform

PLCC44: plastic leaded chip carrier; 44 leads SOT187-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

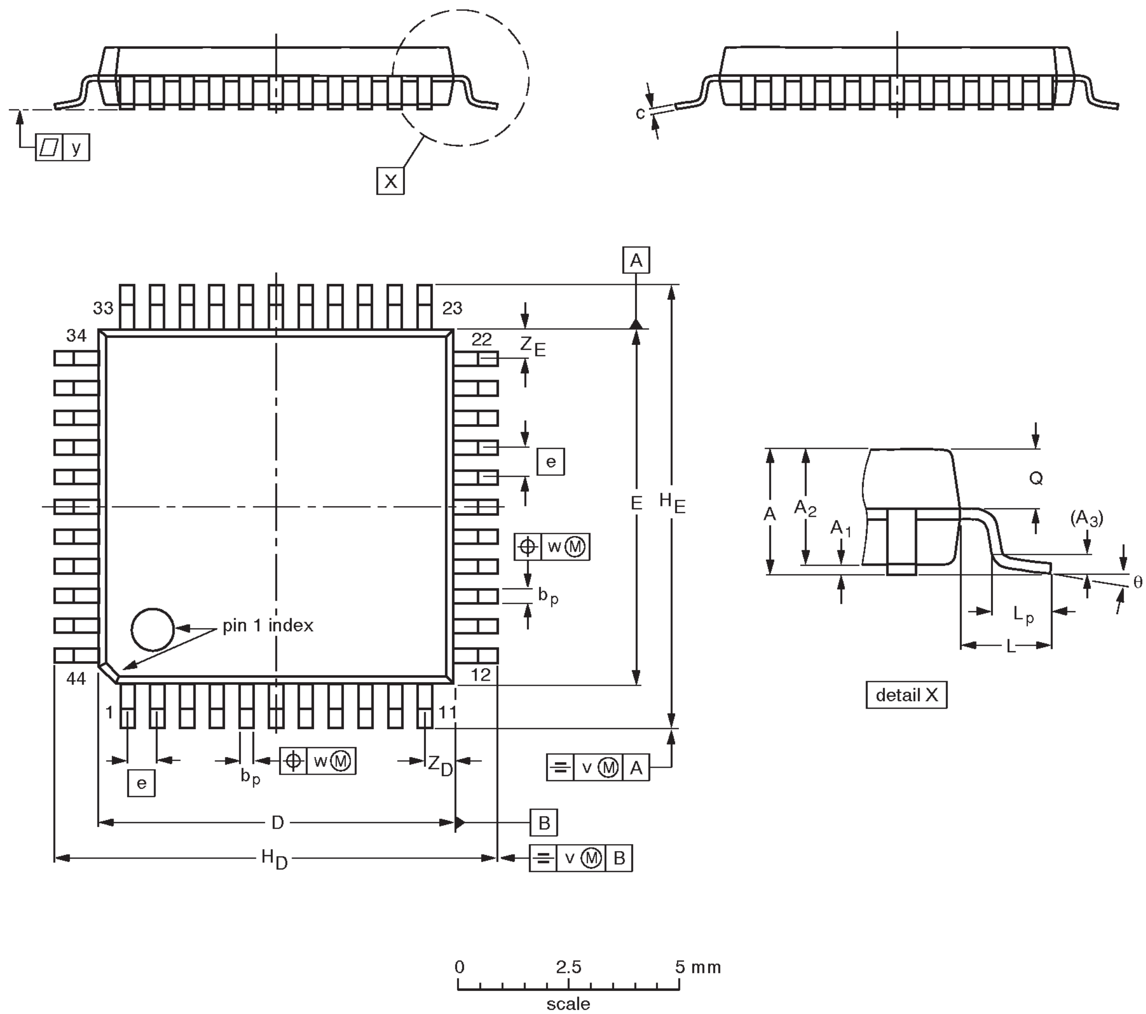
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	16.66 16.51	16.66 16.51	1.27	16.00 14.99	16.00 14.99	17.65 17.40	17.65 17.40	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45°
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.656 0.650	0.656 0.650	0.05	0.630 0.590	0.630 0.590	0.695 0.685	0.695 0.685	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT187-2	112E10	MO-047AC				~~92-11-17~~ 95-02-25

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~92-11-17~~ 95-02-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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