## DISCRETE SEMICONDUCTORS

# DATA SHEET

# **BLF545**UHF push-pull power MOS transistor

**Product specification** 





### **UHF push-pull power MOS transistor**

**BLF545** 

### **FEATURES**

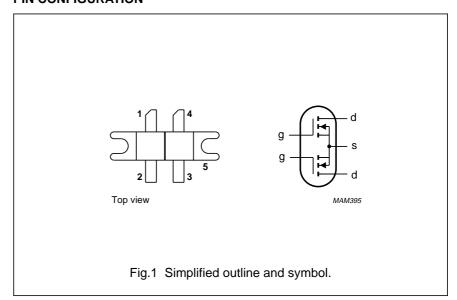
- · High power gain
- · Easy power control
- · Good thermal stability
- Gold metallization ensures excellent reliability
- Designed for broadband operation.

### **DESCRIPTION**

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor designed for communications transmitter applications in the UHF frequency range.

The transistor is encapsulated in a 4-lead, SOT268 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

### PIN CONFIGURATION



### **CAUTION**

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

### **PINNING - SOT268**

PIN	DESCRIPTION
1	drain 1
2	gate 1
3	gate 2
4	drain 2
5	source

### **WARNING**

### Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

### QUICK REFERENCE DATA

RF performance at T<sub>h</sub> = 25 °C in a push-pull common source circuit.

MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>P</sub> (dB)	η <sub>D</sub> (%)
CW, class-B	500	28	40	> 11	> 50

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### **LIMITING VALUES**

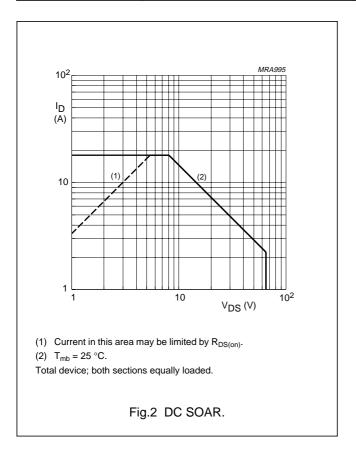
In accordance with the Absolute Maximum System (IEC 134).

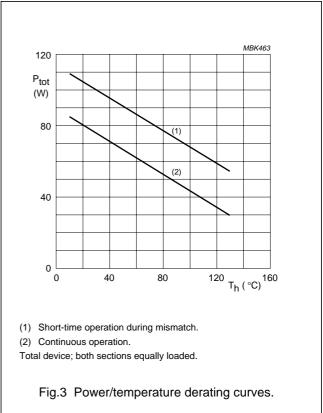
Per transistor section unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		_	65	V
±V <sub>GS</sub>	gate-source voltage		_	20	V
I <sub>D</sub>	DC drain current		_	3.5	Α
P <sub>tot</sub>	total power dissipation	up to T <sub>mb</sub> = 25 °C; total device; both sections equally loaded	_	92	W
T <sub>stg</sub>	storage temperature		-65	150	°C
Tj	junction temperature		_	200	°C

### THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
R <sub>th j-mb</sub>	thermal resistance from junction to mounting base	total device; both sections equally loaded	1.9 K/W
R <sub>th mb-h</sub>	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.25 K/W





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### **CHARACTERISTICS** (per section)

 $T_j = 25$  °C unless otherwise specified.

SYMBOL	PARAMETER	PARAMETER CONDITIONS		TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	V <sub>GS</sub> = 0; I <sub>D</sub> = 10 mA	65	_	_	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>GS</sub> = 0; V <sub>DS</sub> = 28 V	_	_	1	mA
$I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20 \text{ V}; V_{DS} = 0$	-	_	1	μΑ
V <sub>GS(th)</sub>	gate-source threshold voltage	$I_D = 40 \text{ mA}; V_{DS} = 10 \text{ V}$	1	_	4	V
9 <sub>fs</sub>	forward transconductance	I <sub>D</sub> = 1.2 A; V <sub>DS</sub> = 10 V	600	900	_	mS
R <sub>DS(on)</sub>	drain-source on-state resistance	I <sub>D</sub> = 1.2 A; V <sub>GS</sub> = 10 V	-	0.85	1.25	Ω
I <sub>DSX</sub>	on-state drain current	V <sub>GS</sub> = 15 V; V <sub>DS</sub> = 10 V	-	4.8	_	Α
C <sub>is</sub>	input capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 28 V; f = 1 MHz	-	32	_	pF
C <sub>os</sub>	output capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 28 V; f = 1 MHz	-	24	_	pF
C <sub>rs</sub>	feedback capacitance	V <sub>GS</sub> = 0; V <sub>DS</sub> = 28 V; f = 1 MHz	-	6.4	_	pF

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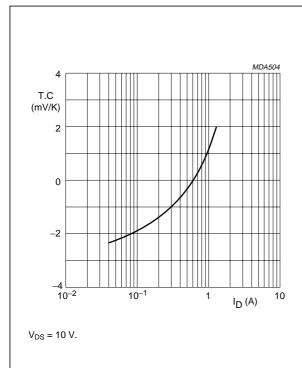


Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.

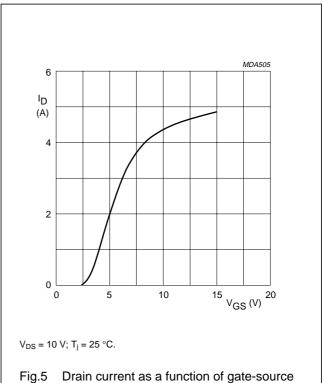


Fig.5 Drain current as a function of gate-source voltage, typical values per section.

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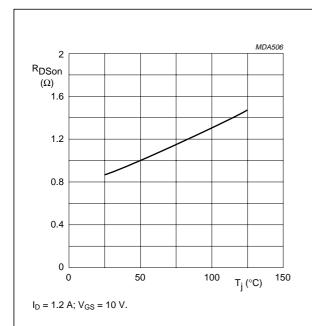


Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.

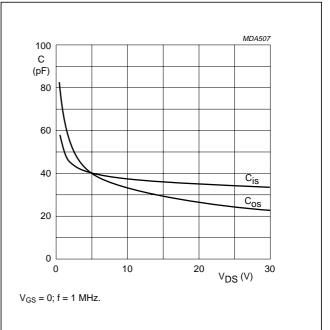
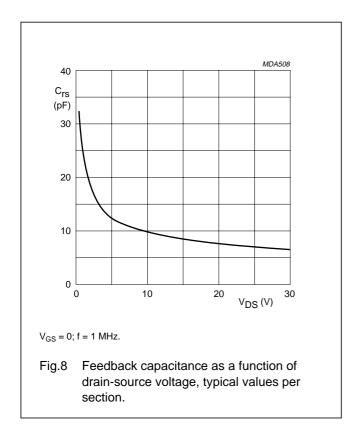


Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



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### **APPLICATION INFORMATION FOR CLASS-B OPERATION**

 $T_h$  = 25 °C;  $R_{th\ mb-h}$  = 0.25 K/W, unless otherwise specified. RF performance in a common source, class-B, push-pull circuit.

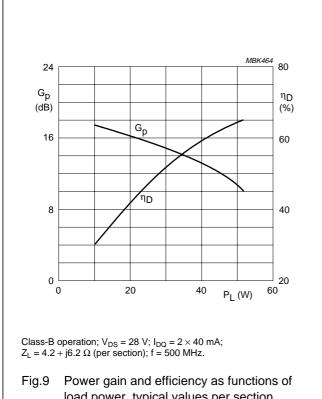
MODE OF OPERATION	f (MHz)	V <sub>DS</sub> (V)	I <sub>DQ</sub> (mA)	P <sub>L</sub> (W)	G <sub>P</sub> (dB)	η <sub>D</sub> (%)
CW, class-B	500	28	2 × 40	40	> 11 typ. 13	> 50 typ. 60

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### Ruggedness in class-B operation

The BLF545 is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions:

 $V_{DS} = 28 \text{ V}$ ; f = 500 MHz at rated output power.



load power, typical values per section.

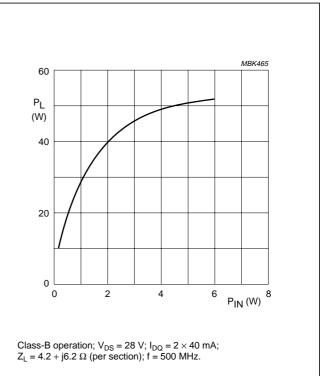
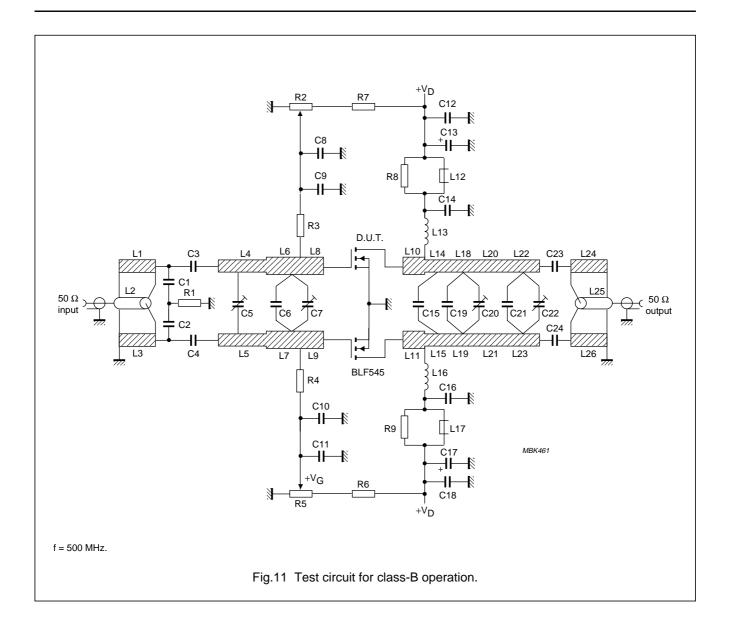


Fig.10 Load power as a function of input power, typical values per section.

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### List of components (class-B test circuit)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor (note 1)	5.1 pF		
C3, C4	multilayer ceramic chip capacitor (note 1)	16 pF		
C5, C7, C20, C22	film dielectric trimmer	1.8 to 10 pF		2222 809 05002
C6	multilayer ceramic chip capacitor (note 1)	22 pF		
C8, C11, C12, C18	multilayer ceramic chip capacitor	100 nF		2222 852 47104
C9, C10, C14, C16	multilayer ceramic chip capacitor (note 1)	390 pF		
C13, C17	electrolytic capacitor	10 μF, 63 V		
C15	multilayer ceramic chip capacitor (note 1)	18 pF		
C19	multilayer ceramic chip capacitor (note 1)	13 pF		
C21	multilayer ceramic chip capacitor (note 1)	6.2 pF		
C23, C24	multilayer ceramic chip capacitor (note 1)	10 pF		
L1, L3, L24, L26	stripline (note 2)	50 Ω	56 × 2.4 mm	
L2, L25	semi-rigid cable (note 3)	50 Ω	ext. dia. 2.2 mm ext. conductor length 56 mm	
L4, L5	stripline (note 2)	56 Ω	13.4 × 2 mm	
L6, L7	stripline (notes 2 and 4)	56 Ω	9.6 × 2 mm	
L8, L9	stripline (note 2)	42 Ω	9 × 3 mm	
L10, L11	stripline (note 2)	42 Ω	6 × 3 mm	
L12, L17	grade 3B Ferroxcube RF choke			4312 020 36642
L13, L16	4 turns enamelled 1.2 mm copper wire	62 nH	length 7.6 mm int. dia. 5 mm leads 2 × 5 mm	
L14, L15	stripline (note 2)	56 Ω	8 × 2 mm	
L18, L19	stripline (note 2)	56 Ω	13 × 2 mm	
L20, L21	stripline (note 2)	56 Ω	18 × 2 mm	
L22, L23	stripline (note 2)	56 Ω	14 × 2 mm	
R1	0.4 W metal film resistor	5.11 Ω		2322 151 75118
R2, R5	10 turns cermet potentiometer	50 kΩ		
R3, R4	0.4 W metal film resistor	10 kΩ		2322 151 71003
R6, R7	0.4 W metal film resistor	205 kΩ		2322 151 72054
R8, R9	1 W metal film resistor	10 Ω		2322 151 71009

### Notes

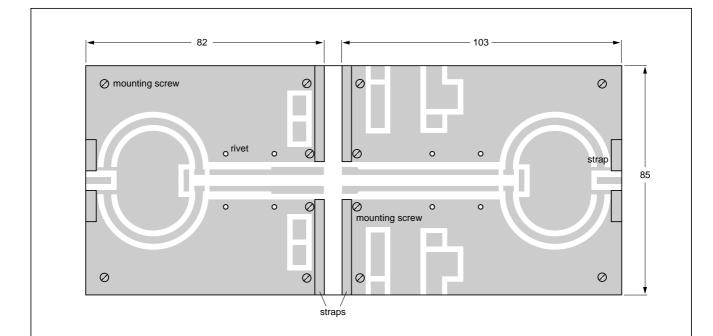
1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.

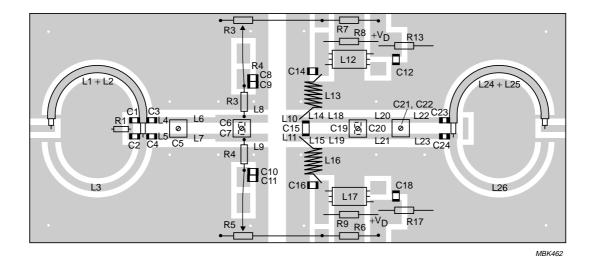
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2. The striplines are on a double copper-clad printed circuit board, with glass microfibre reinforced PTFE ( $\epsilon_r$  = 2.2); thickness 1/32 inch.

- 3. Semi-rigid cables L2 and L25 are soldered on to striplines L1 and L26.
- 4. Striplines L6 and L7 are used in series with a 42  $\Omega$  stripline (11  $\times$  3 mm).





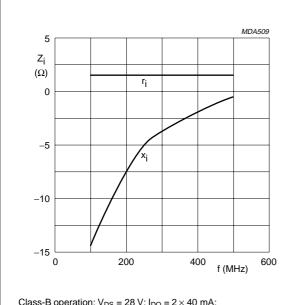
The circuit and components are situated on one side of the printed circuit board, the other side being fully metallized, to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Dimensions in mm.

Fig.12 Component layout for 500 MHz class-B test circuit.

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Class-B operation;  $V_{DS}$  = 28 V;  $I_{DQ}$  = 2 × 40 mA;  $P_L$  = 40 W.

Fig.13 Input impedance as a function of frequency (series components), typical values per section.

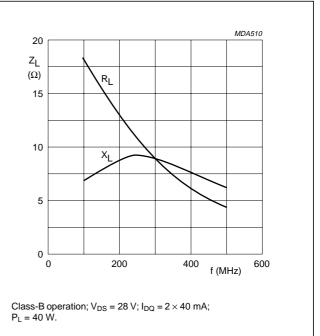


Fig.14 Load impedance as a function of frequency (series components), typical values per section.

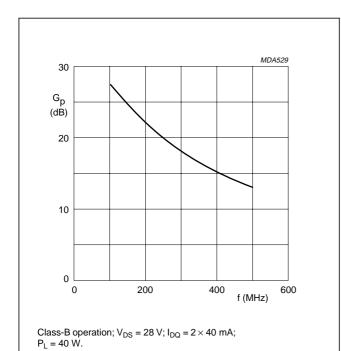


Fig.15 Power gain as a function of frequency, typical values per section.

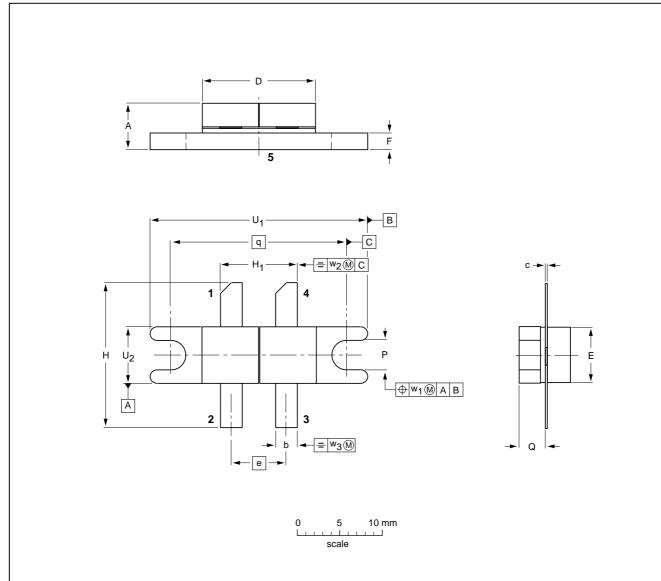
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### **PACKAGE OUTLINE**

Flanged double-ended ceramic package; 2 mounting holes; 4 leads

SOT268A



### DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

ι	JNIT	Α	b	С	D	E	е	F	н	Н <sub>1</sub>	р	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>	w <sub>3</sub>
	mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.51	1.02	0.26
ir		0.193 0.165	0.065 0.055	0.005 0.003		0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.02	0.04	0.01

OUTLINE		REFER	EUROPEAN ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT268A						97-06-28

Product specification Philips Semiconductors

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### **DEFINITIONS**

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

### **Application information**

Where application information is given, it is advisory and does not form part of the specification.

### LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.