

DATA SHEET

BSP090

P-channel enhancement mode
vertical D-MOS transistor

Product specification
Supersedes data of 1997 Jan 20
File under Discrete Semiconductors, SC07

1997 Mar 13

P-channel enhancement mode vertical D-MOS transistor

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FEATURES

- High speed switching
- No secondary breakdown
- Very low on-state resistance.

APPLICATIONS

- Motor and actuator drivers
- Power management
- Synchronized rectification.

DESCRIPTION

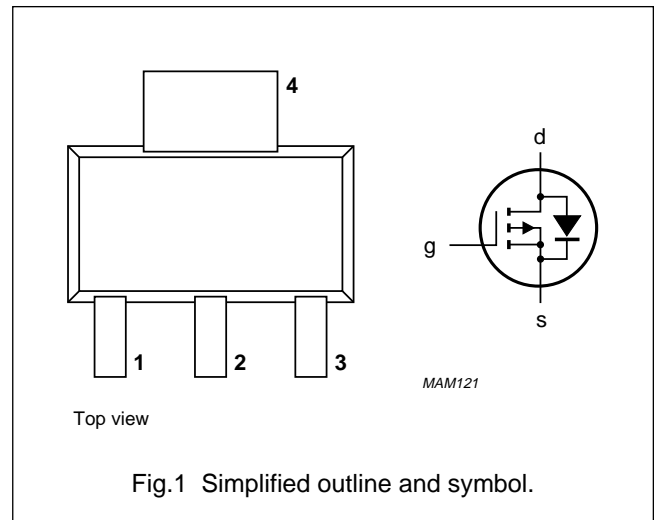
P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION

The device is supplied in an antistatic package.
The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		-	-30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	-	-1.3	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	-1	-2.8	V
I_D	drain current (DC)	$T_s = 100$ °C	-	-5.7	A
R_{DSon}	drain-source on-state resistance	$I_D = -2.8$ A; $V_{GS} = -10$ V	-	0.09	Ω
P_{tot}	total power dissipation	$T_s = 100$ °C	-	5	W

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_s = 100\text{ }^\circ\text{C}$; note 1	–	–5.7	A
I_{DM}	peak drain current	note 2	–	–22	A
P_{tot}	total power dissipation	$T_s = 100\text{ }^\circ\text{C}$	–	5	W
		$T_{amb} = 25\text{ }^\circ\text{C}$; note 3	–	3.3	W
		$T_{amb} = 25\text{ }^\circ\text{C}$; note 4	–	1.25	W
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	operating junction temperature		–65	+150	$^\circ\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_s = 100\text{ }^\circ\text{C}$	–	–3.8	A
I_{SM}	peak pulsed source current	note 2	–	–15	A

Notes

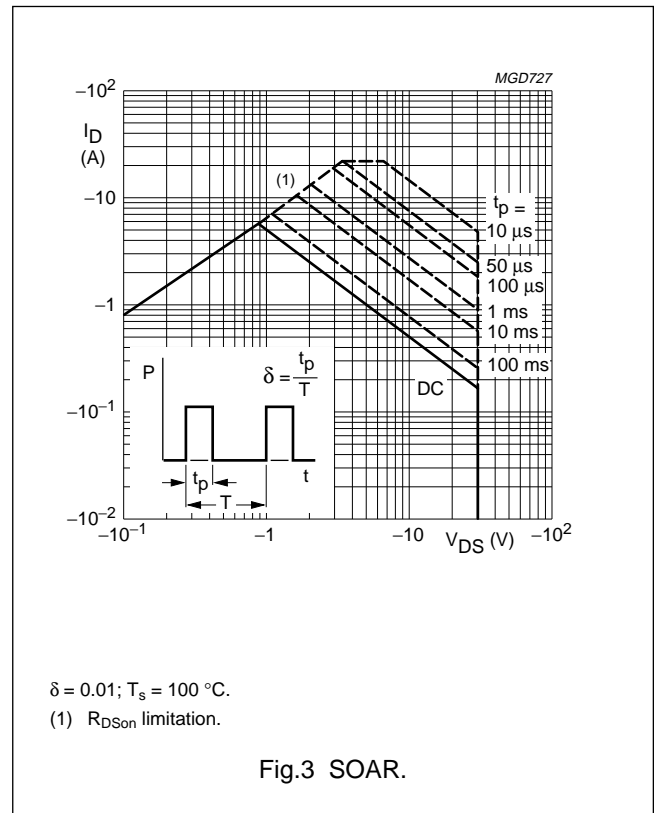
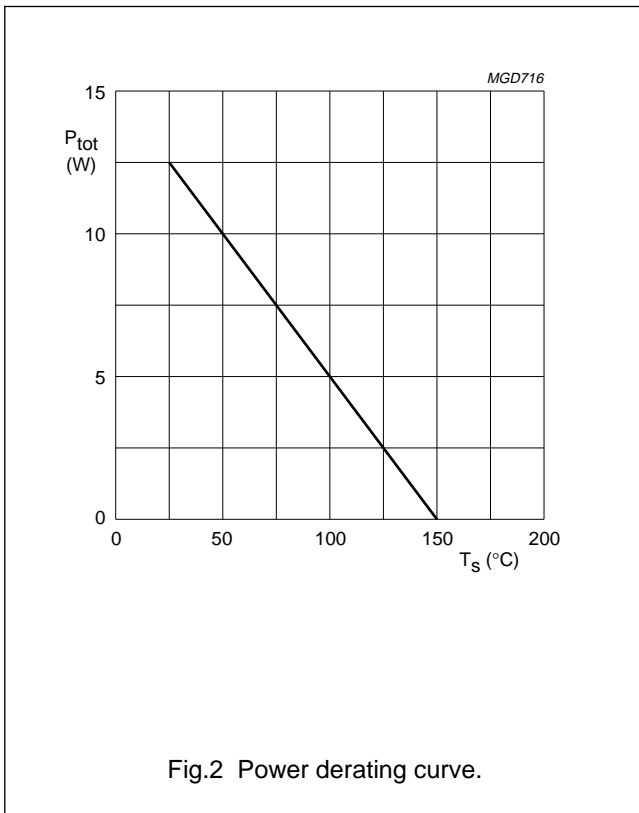
- T_s is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Device mounted on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
- Device mounted on a printed-circuit board with a $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	10	K/W

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CHARACTERISTICS $T_j = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-30	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-1	–	-2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24\ \text{V}$	–	–	-500	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}; I_D = -1.4\ \text{A}$	–	–	0.15	Ω
		$V_{GS} = -10\ \text{V}; I_D = -2.8\ \text{A}$	–	–	0.09	Ω
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	800	–	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	400	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	100	–	pF
Q_g	total gate charge	$V_{GS} = -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -2.8\ \text{A}; T_{amb} = 25\text{ °C}$	–	21	–	nC
Q_{gs}	gate-source charge	$V_{GS} = -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -2.8\ \text{A}; T_{amb} = 25\text{ °C}$	–	2.5	–	nC
Q_{gd}	gate-drain charge	$V_{GS} = -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -2.8\ \text{A}; T_{amb} = 25\text{ °C}$	–	6	–	nC
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	6	–	ns
t_r	rise time	$V_{GS} = 0\ \text{to}\ -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	6	–	ns
t_{on}	turn-on switching time	$V_{GS} = 0\ \text{to}\ -10\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	12	25	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = -10\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	55	–	ns
t_f	fall time	$V_{GS} = -10\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	40	–	ns
t_{off}	turn-off switching time	$V_{GS} = -10\ \text{to}\ 0\ \text{V}; V_{DD} = -15\ \text{V};$ $I_D = -1\ \text{A}; R_L = 15\ \Omega; R_{gen} = 6\ \Omega$	–	95	190	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0; I_S = -1.25\ \text{A}$	–	–	-1.3	V
t_{rr}	reverse recovery time	$I_S = -1.25\ \text{A}; di/dt = 100\ \text{A}/\mu\text{s}$	–	70	–	ns

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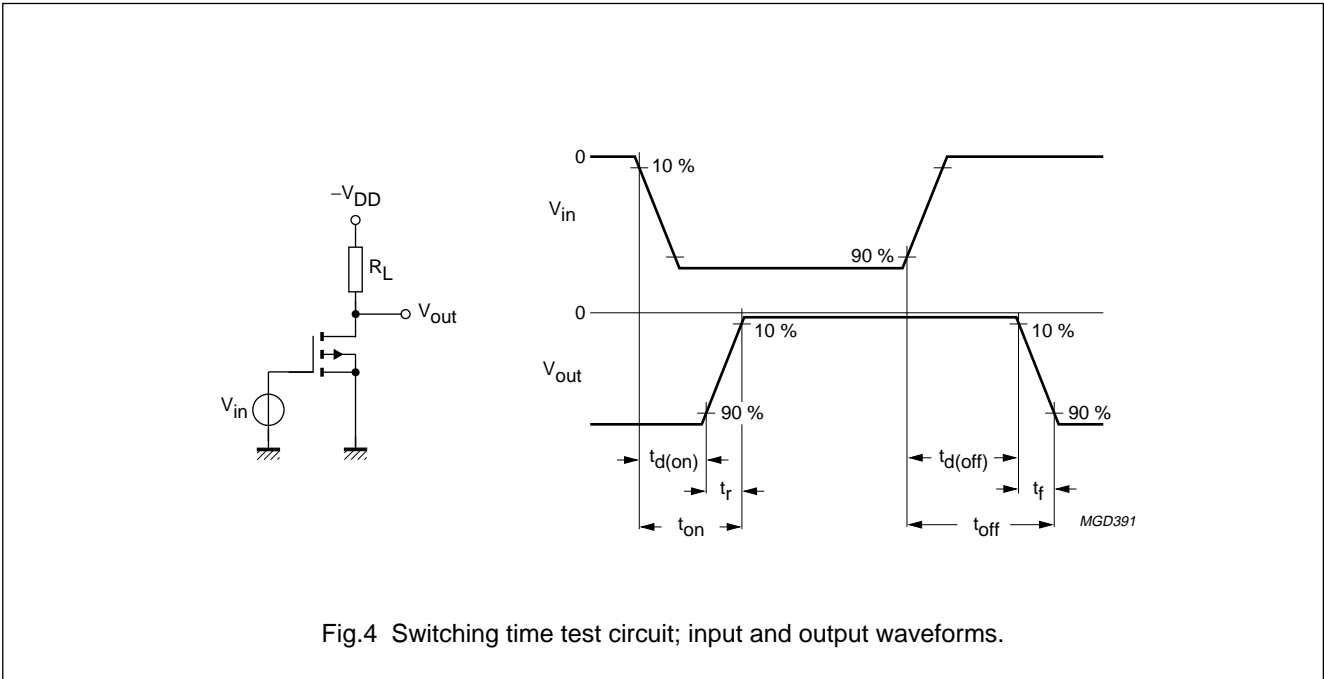


Fig.4 Switching time test circuit; input and output waveforms.

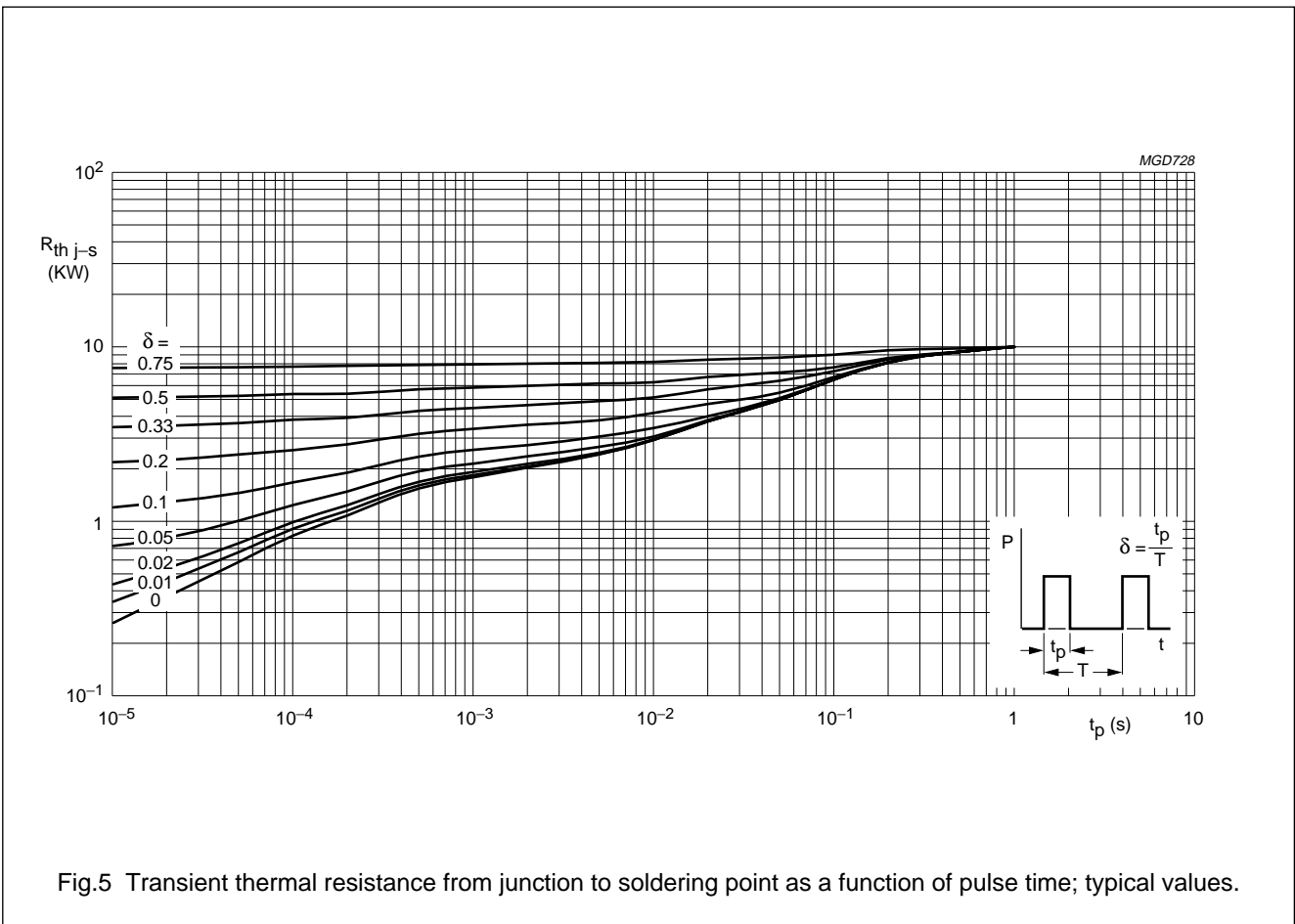
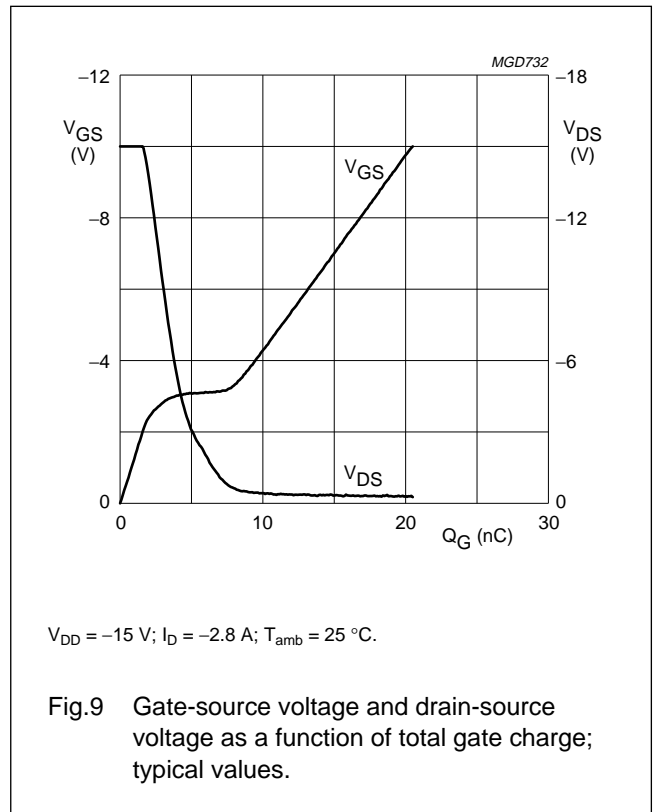
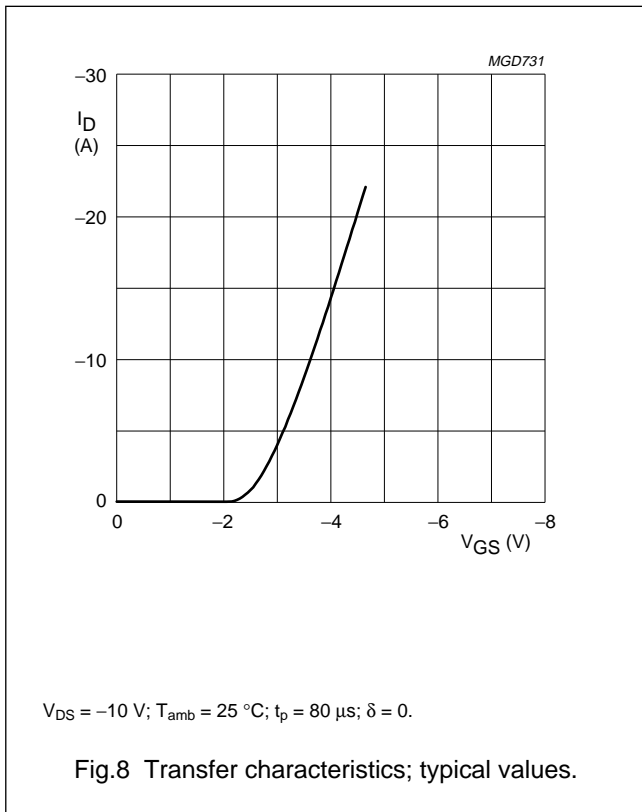
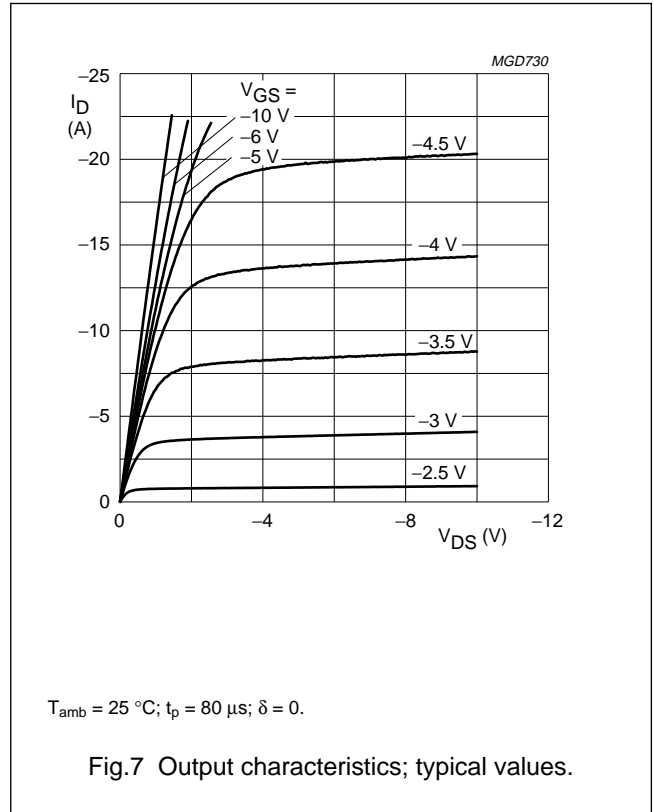
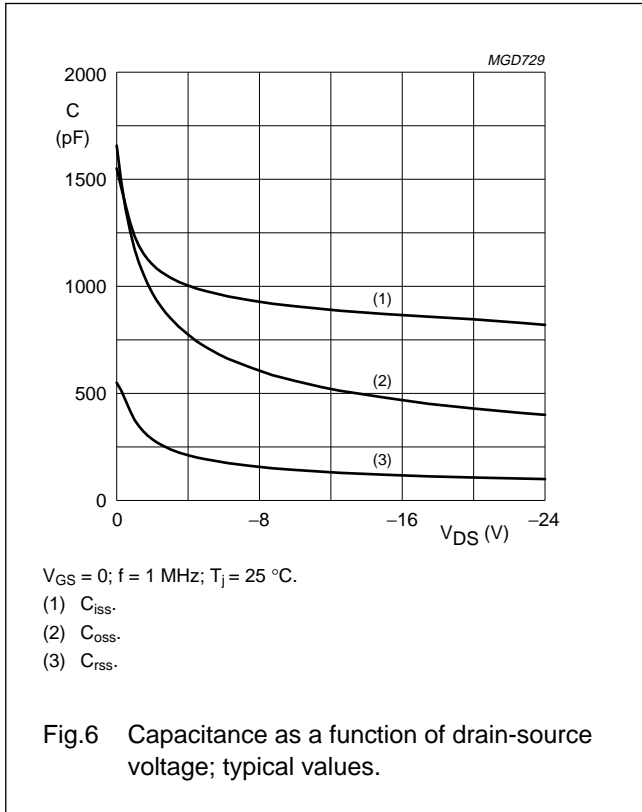


Fig.5 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

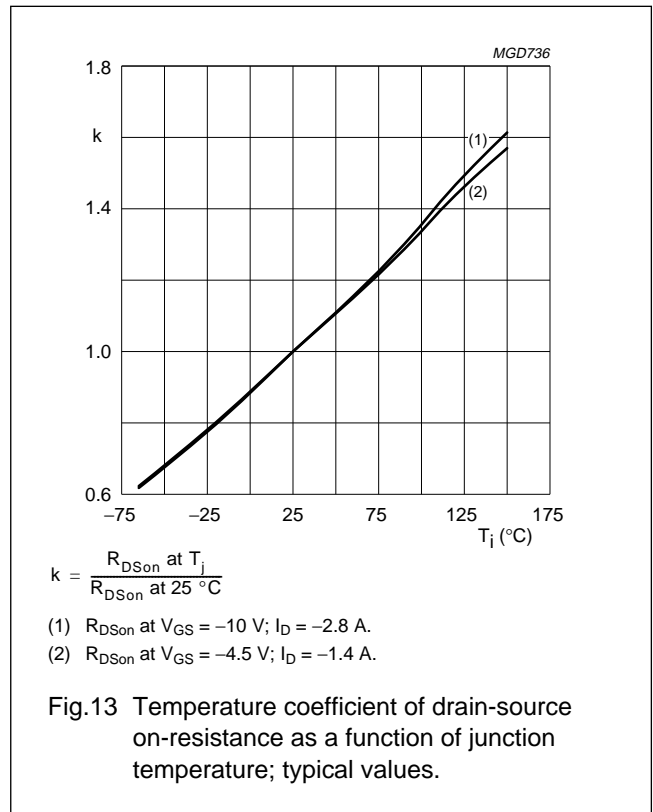
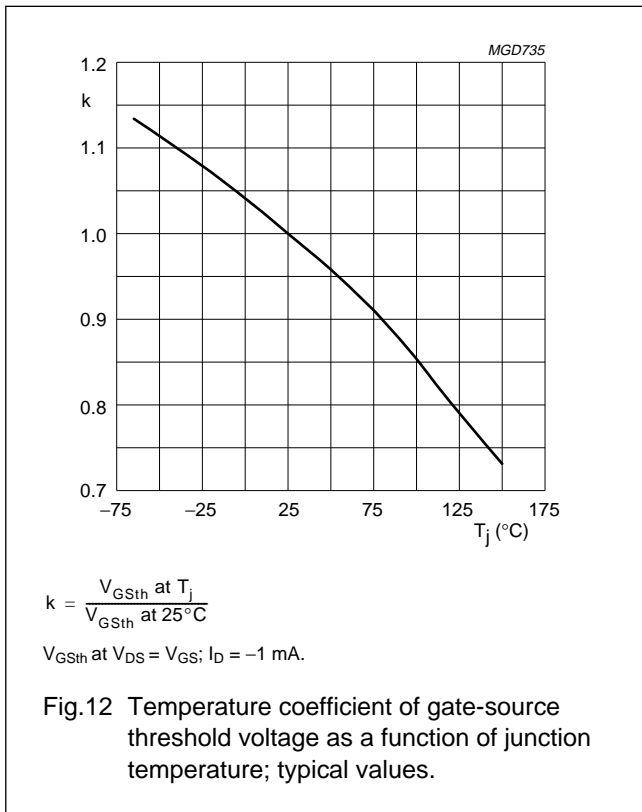
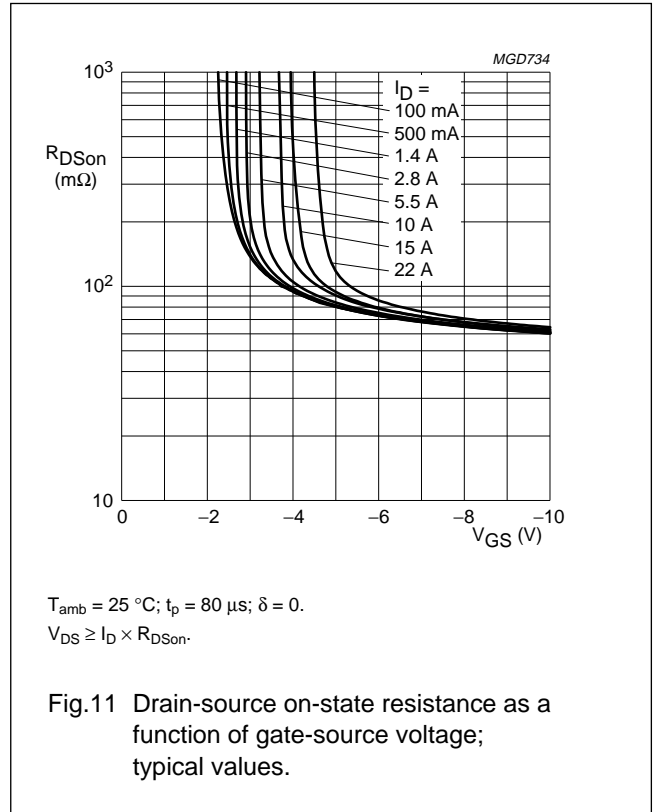
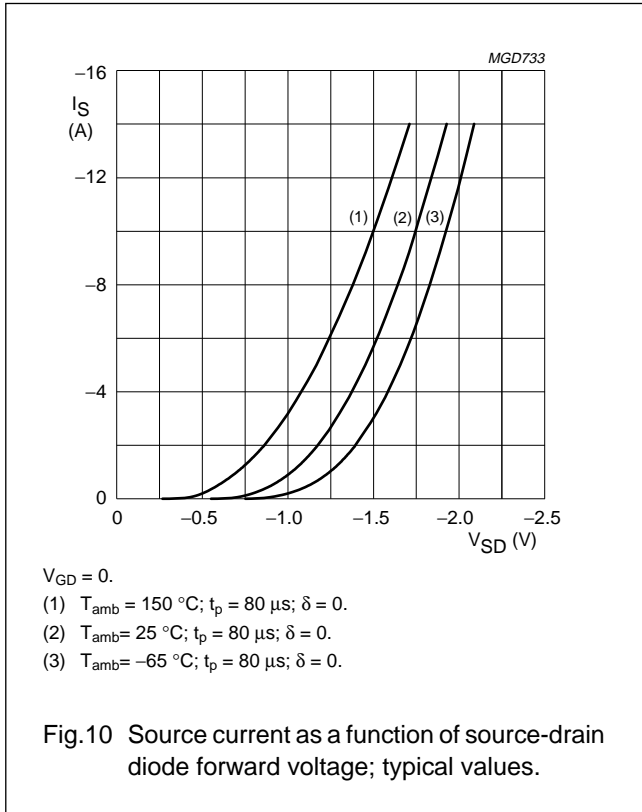
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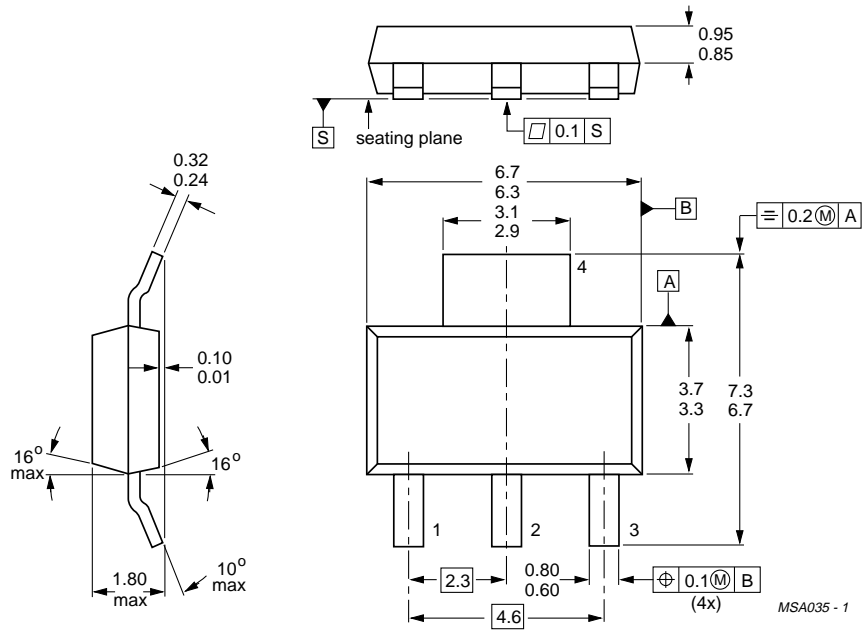
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PACKAGE OUTLINE



Dimensions in mm.

Fig.14 SOT223.

P-channel enhancement mode vertical D-MOS transistor

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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