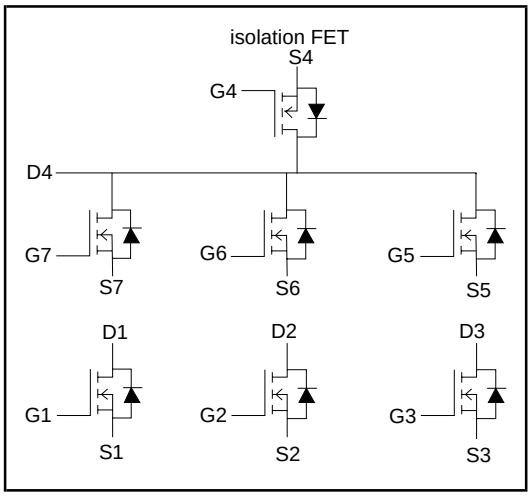
N-channel enhancement mode TrenchMOS transistor array

PHN70308

FEATURES

- 30 mΩ isolation transistor
- 80 mΩ spindle transistors
- TrenchMOS technology
- Logic level compatible
- Surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DS} = 25 V

I_D = 5 A

$R_{DS(ON)} \leq$ 30 mΩ

(V_{GS} = 10 V; isolation FET)

$R_{DS(ON)} \leq$ 80 mΩ

(V_{GS} = 10 V; spindle FETs)

GENERAL DESCRIPTION

This product is used to drive high performance, three phase brushless d.c. motors in computer disk drives.

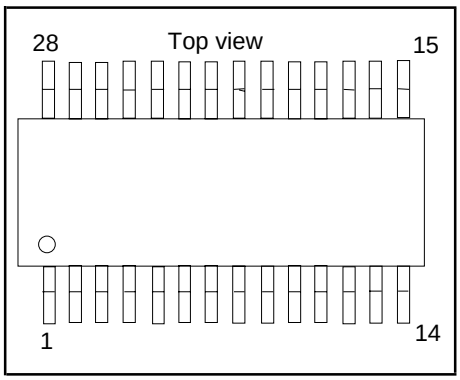
The PHN70308 contains seven, n-channel enhancement mode trenchMOS transistors in a surface mounting plastic package. Six of the transistors can be configured as a three phase bridge to drive the spindle of a disk drive motor. The remaining transistor delivers power to the three phase bridge during normal operation. In the event of a power failure occurring whilst the motor is still spinning, this transistor isolates the computer power supply from the back emf generated by the motor.

The PHN70308 is supplied in the surface mounting SOT341-1 (SSOP28) package.

PINNING

PIN	DESCRIPTION	PIN	DESCRIPTION
1,3	drain 1	16,17	source 4
2	source 1	18	gate 4
4	gate 1	20	gate 5
5,7	drain 2	21	source 5
6	source 2	23	gate 6
8	gate 2	24	source 6
9,11	drain 3	26	gate 7
10	source 3	27	source 7
12	gate 3	13-15,19,22,25,28	drain 4

SOT341-1 (SSOP28)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	T_j = 25 ˚C to 150˚C	-	25	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Peak drain current per device	T_{sp} = 50 ˚C[1]			
	(continuous operation)	spindle FETs; δ = 33.3%	-	5	A
		Isolation FET (dc)	-	5	A
I_{DM}	Peak current per device (pulse	spindle FETs	-	20	A
	peak value)	isolation FET	-	20	A
P_{tot}	Power dissipation per device[2]	T_{sp} = 50 ˚C			
		spindle FETs; δ = 33.3%	-	1.13	W
		isolation FET (dc)	-	1.275	W
P_{tot}	Total power dissipation in normal operation[2]	T_{sp} = 50 ˚C spindle FETs; δ = 33.3% isolation FET (dc)	-	8	W
T_{stg}, T_j	Storage & operating temperature		- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}sp}$	Thermal resistance junction to	isolation FET	20	-	K/W
	solder point	spindle FET	43	-	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	device soldered to FR4 board, minimum footprint.			
		isolation FET	85	-	K/W
		spindle FET	100	-	K/W

1 T_{sp} is the temperature at the soldering point of the drain leads.

2 In normal operation, the isolation FET conducts continuously whilst each of the spindle FETs conducts for 33.3% of the time. The dissipation in the isolation transistor is given by:-

$$P_{isolation} = I^2 x R_{DS(ON)(isolation FET)}$$

The dissipation in each of the spindle transistors is given by:-

$$P_{spindle} = 0.333 x I^2 x R_{DS(ON)(spindle FET)}$$

The total dissipation under these conditions is given by:-

$$P_{tot} = P_{isolation} + 6 x P_{spindle}$$

With the motor being driven at 5 A and assuming T_j = 150˚C, the total dissipation is:-

$$P_{tot} = 25 x 0.03 x 1.7 + 0.333 x 25 x 0.08 x 1.7 x 6 = 8 W$$

Switching losses are assumed to be negligible.

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 10 μA	25	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4 A				
		spindle FET	-	60	80	mΩ
		isolation FET	-	27	30	mΩ
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 2 A				
		spindle FET	-	95	150	mΩ
		isolation FET	-	38	60	mΩ
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4 A; T_j = 150˚C				
		spindle FET	-	102	136	mΩ
		isolation FET	-	46	51	mΩ
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 20 V; V_{GS} = 0 V;	-	10	100	nA
		T_j = 150˚C	-	0.1	0.5	mA
$Q_{g(tot)}$	Total gate charge	I_D = 1 A; V_{DD} = 20 V; V_{GS} = 10 V				
		spindle FET	-	5.4	-	nC
		isolation FET	-	17.6	-	nC
Q_{gs}	Gate-source charge	spindle FET	-	0.4	-	nC
		isolation FET	-	1.4	-	nC
Q_{gd}	Gate-drain (Miller) charge	spindle FET	-	1.6	-	nC
		isolation FET	-	5.7	-	nC
t_{on}	Turn-on time	V_{DD} = 20 V; I_D = 1 A; V_{GS} = 10 V; R_G = 6 Ω; resistive load				
		spindle FET	-	5.5	10	ns
		isolation FET	-	11	20	ns
t_{off}	Turn-off time	spindle FET	-	16	25	ns
		isolation FET	-	45	60	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz				
		spindle FET	-	180	-	pF
		isolation FET	-	546	-	pF
C_{oss}	Output capacitance	spindle FET	-	70	-	pF
		isolation FET	-	311	-	pF
C_{rss}	Feedback capacitance	spindle FET	-	36	-	pF
		isolation FET	-	133	-	pF

SOURCE-DRAIN DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_F	Continuous forward diode current	T_{sp} = 50 ˚C				
		spindle FET; δ = 33.3%	-	-	5	A
		isolation FET	-	-	5	A
I_{FRM}	Repetitive peak forward diode current	spindle FET	-	-	20	A
		isolation FET	-	-	20	A
V_F	Diode forward voltage	I_F = 1.25 A; V_{GS} = 0 V				
		spindle FET	-	0.8	1	V
		isolation FET	-	0.8	1	V
t_{rr}	Reverse recovery time	I_F = 1.25 A; -dI_F/dt = 100 A/µs; V_{DS} = 25 V				
		spindle FET	-	20	-	ns
		isolation FET	-	25	-	ns

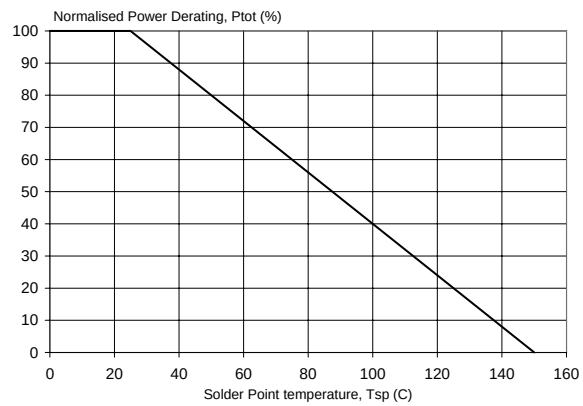


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{sp})

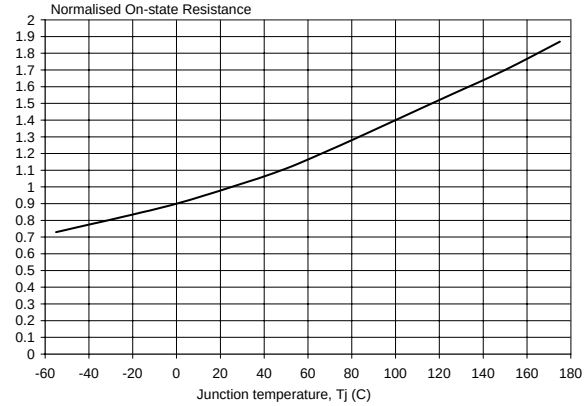


Fig.3. Normalised drain-source on-state resistance.
$R_{DS(ON)}$/$R_{DS(ON)25\ ˚C}$ = f(T_j)

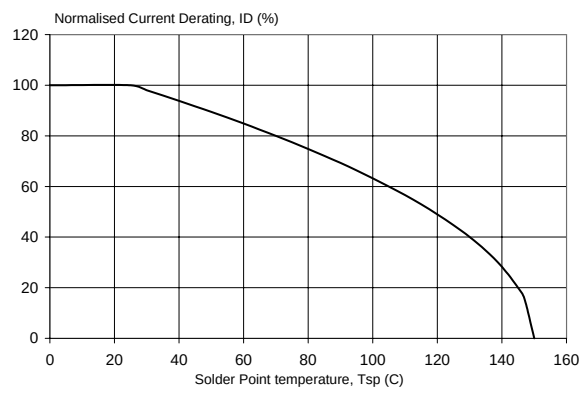


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{sp}); conditions: V_{GS} ≥ 10 V

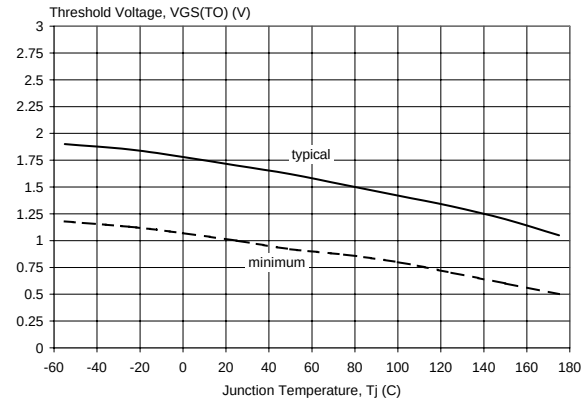


Fig.4. Gate threshold voltage.
$V_{GS(TO)}$ = f(T_j); conditions: I_D = 1 mA; V_{DS} = V_{GS}

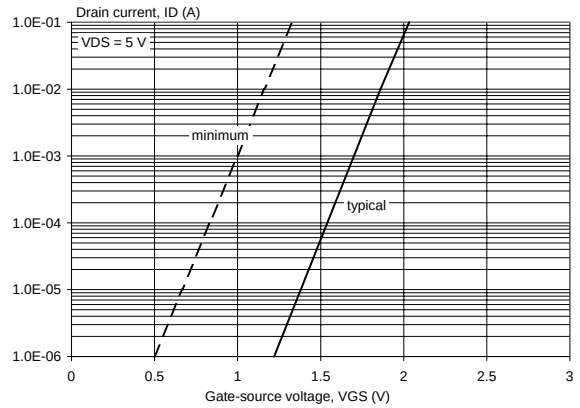


Fig.5. Sub-threshold drain current. $I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C

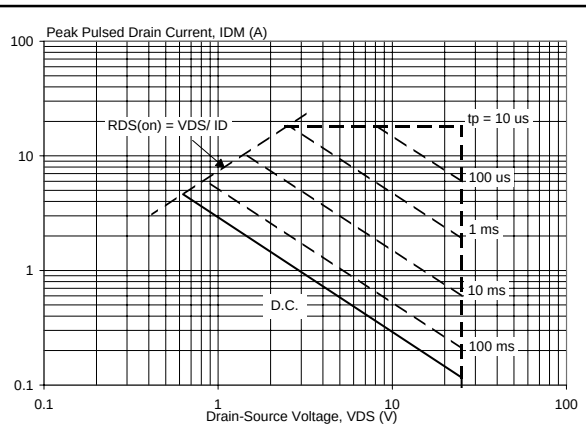


Fig.6. Safe operating area (spindle FET) $T_{sp} = 25$˚C I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

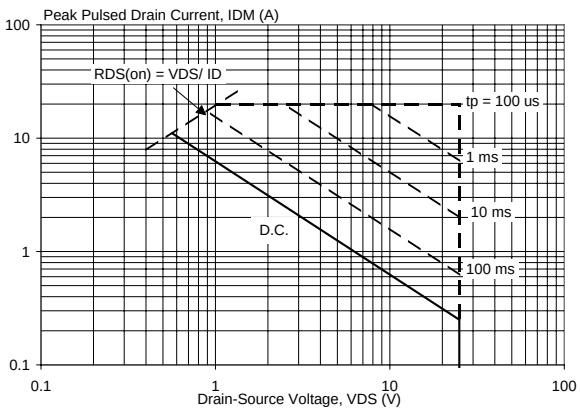


Fig.7. Safe operating area (isolation FET) $T_{sp} = 25$˚C I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

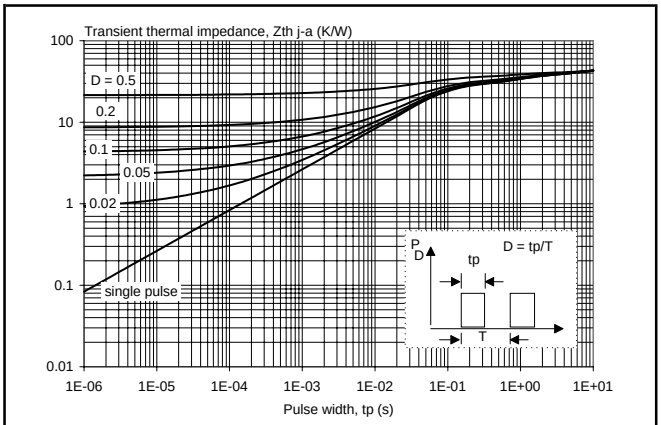


Fig.8. Transient thermal impedance (spindle FET). $Z_{th\ j\text{-}sp} = f(t)$; parameter $D = t_p/T$

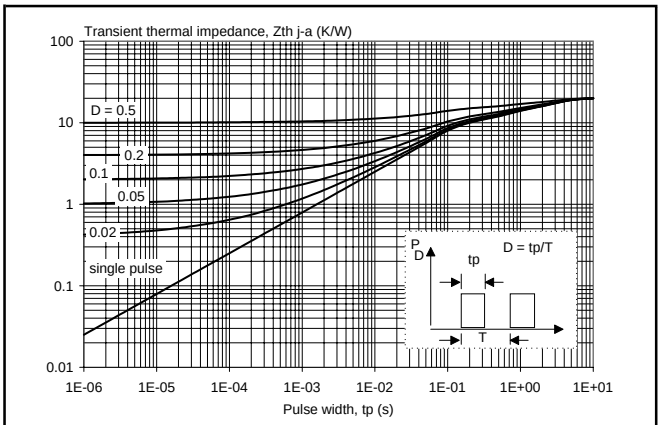


Fig.9. Transient thermal impedance (isolation FET). $Z_{th\ j\text{-}sp} = f(t)$; parameter $D = t_p/T$

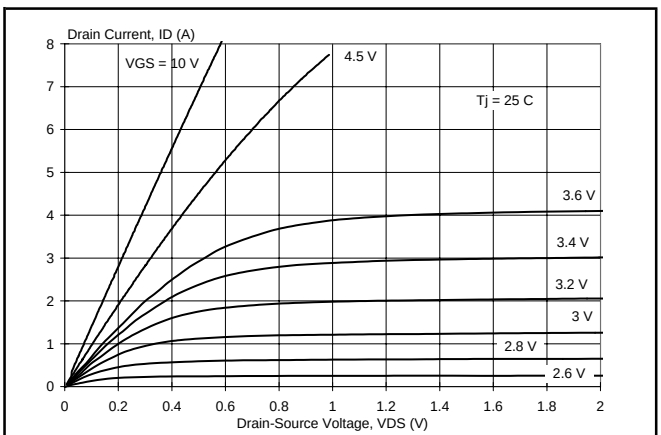


Fig.10. Typical output characteristics (spindle FET) $T_j = 25$ ˚C; $I_D = f(V_{DS})$; parameter V_{GS}

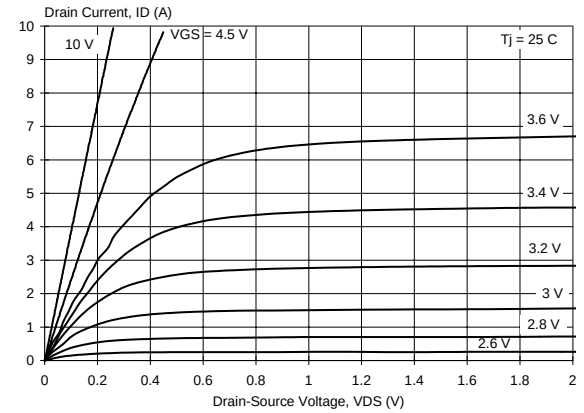


Fig.11. Typical output characteristics (isolation FET) T_j = 25 ˚C; $I_D = f(V_{DS})$; parameter V_{GS}

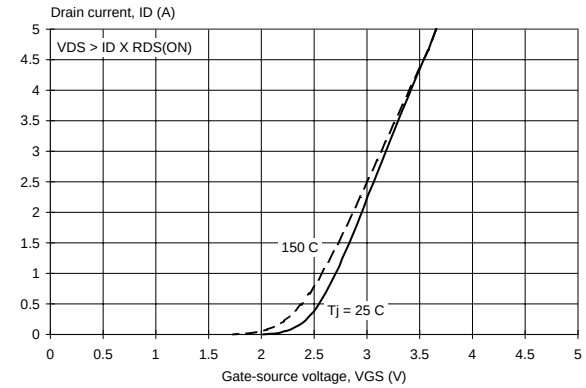


Fig.14. Typical transfer characteristics (spindle FET) $I_D = f(V_{GS})$

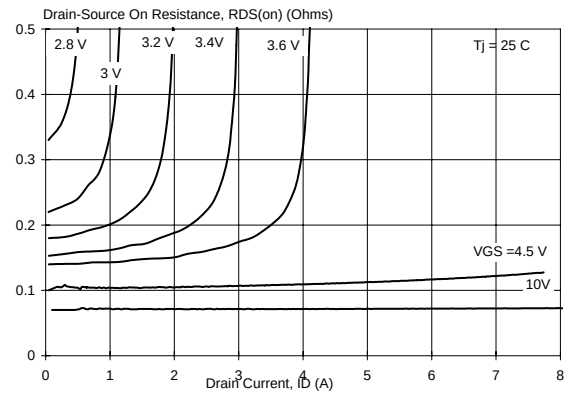


Fig.12. Typical on-state resistance (spindle FET) T_j = 25 ˚C; $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

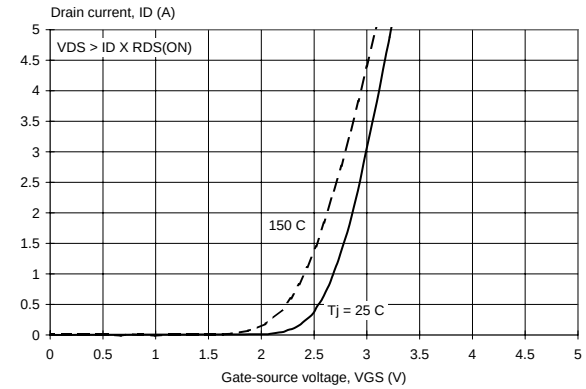


Fig.15. Typical transfer characteristics (isolation FET); $I_D = f(V_{GS})$

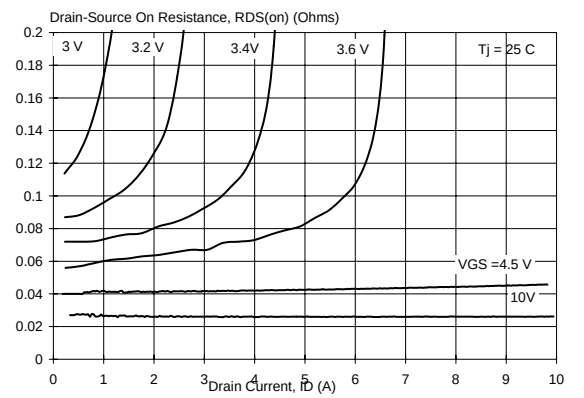


Fig.13. Typical on-state resistance (isolation FET) T_j = 25 ˚C; $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

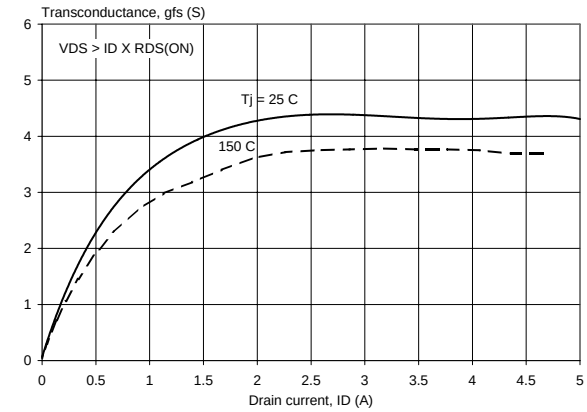


Fig.16. Typical transconductance (spindle FET) T_j = 25 ˚C; $g_{fs} = f(I_D)$

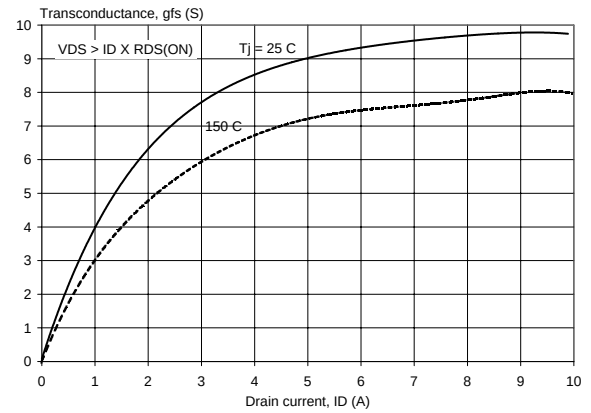


Fig.17. Typical transconductance (isolation FET) T_j = 25 ˚C; $g_{fs} = f(I_D)$

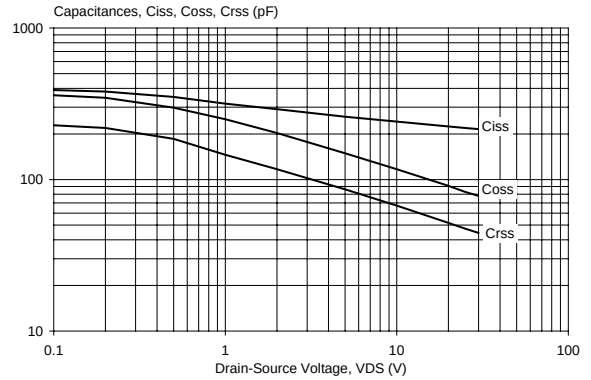


Fig.18. Typical capacitances (spindle FET) C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

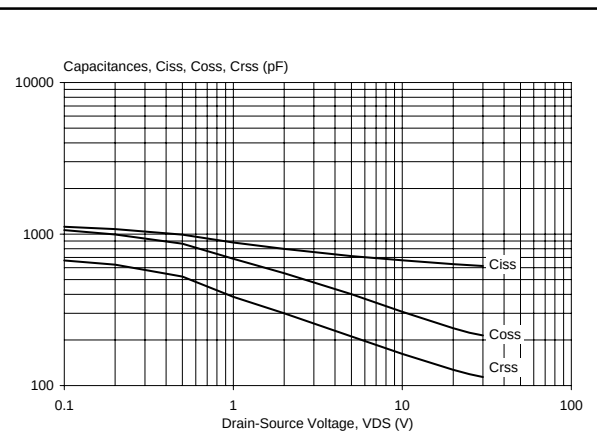


Fig.19. Typical capacitances (isolation FET) C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

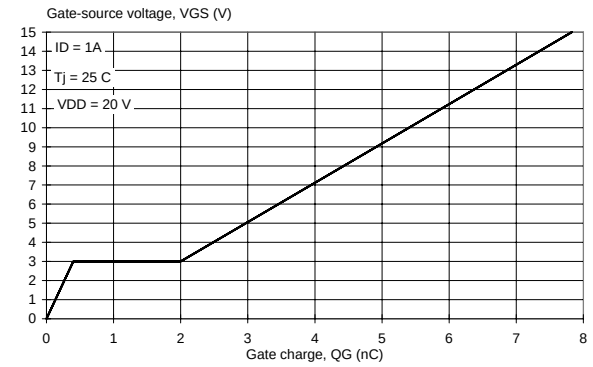


Fig.20. Typical turn-on gate-charge characteristics (spindle FET); $V_{GS} = f(Q_G)$

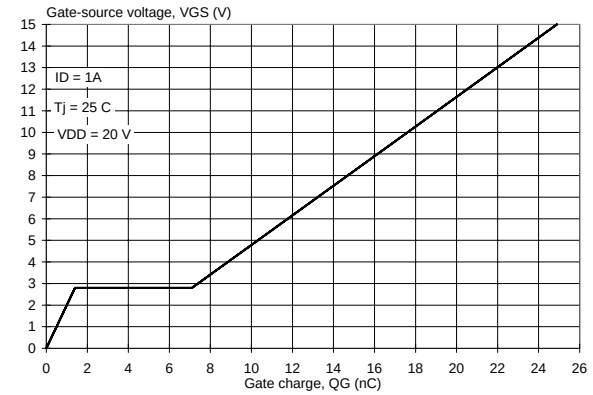


Fig.21. Typical turn-on gate-charge characteristics (isolation FET); $V_{GS} = f(Q_G)$

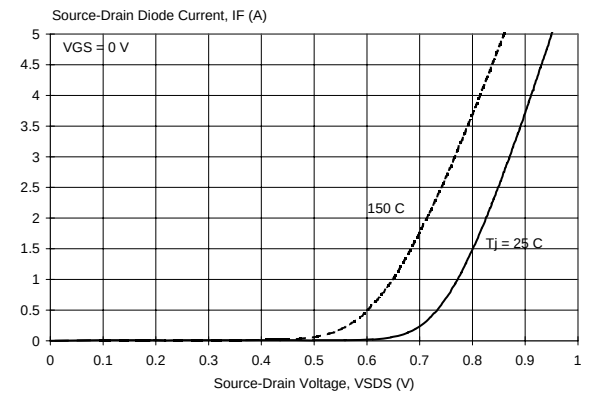


Fig.22. Typical reverse diode current (spindle FET) $I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

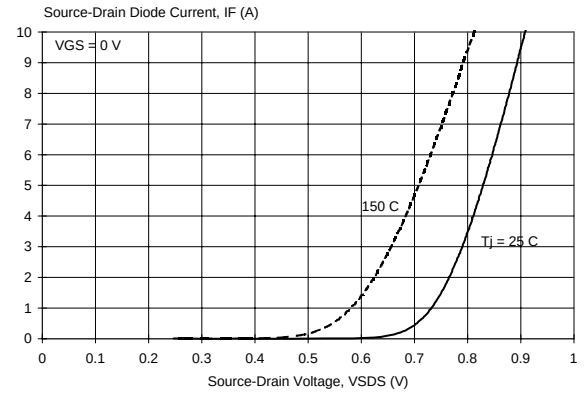
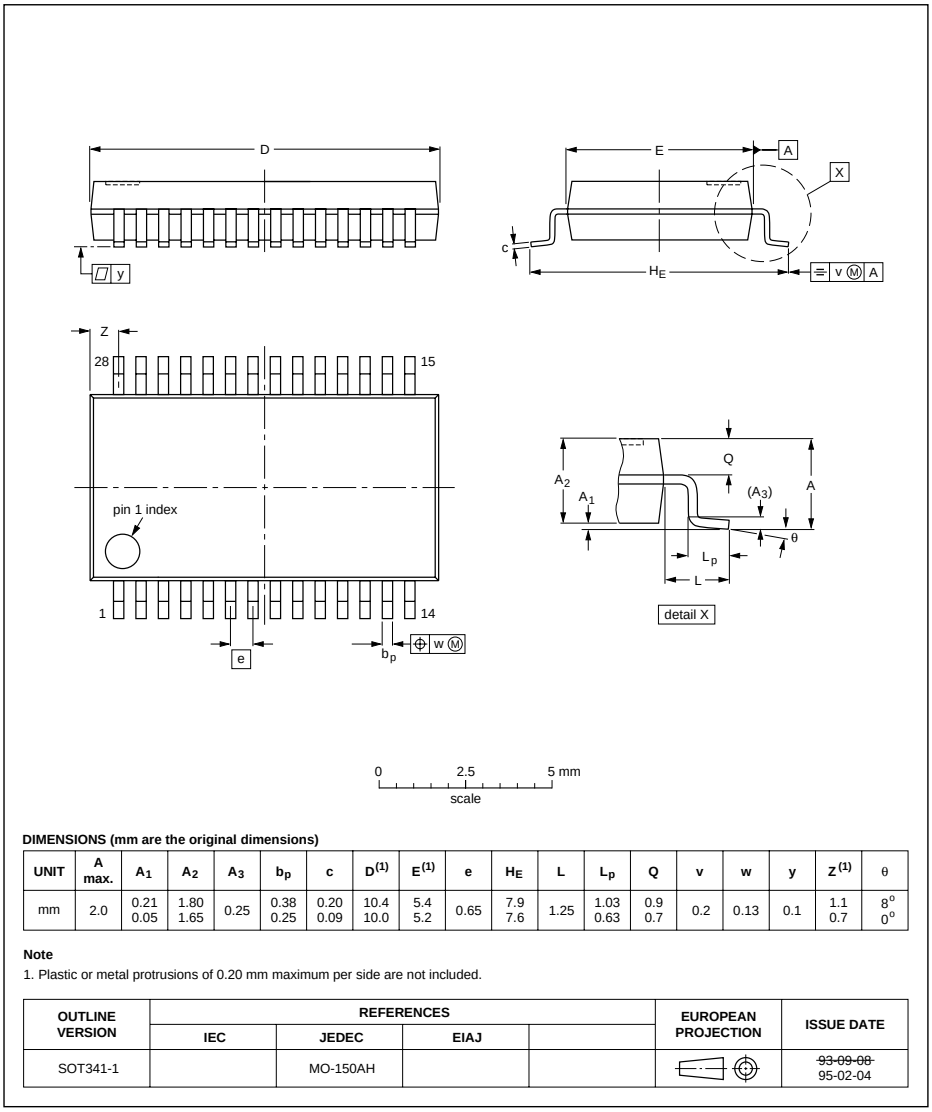


Fig.23. Typical reverse diode current (isolation FET) $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Fig.24. SOT341-1 (SSOP28) surface mounting package.

Notes

1. This product is supplied in anti-static packaging. The leads must be protected against static discharge during transport or handling.
2. Refer to Integrated Circuit Packages, Data Handbook IC26.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.