

PowerMOS transistor Logic level FET

PHP3N20L

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope featuring high avalanche energy capability, stable blocking voltage, fast switching and high thermal cycling performance with low thermal resistance. Intended for use in Switched Mode Power Supplies (SMPS), motor control circuits and general purpose switching applications.

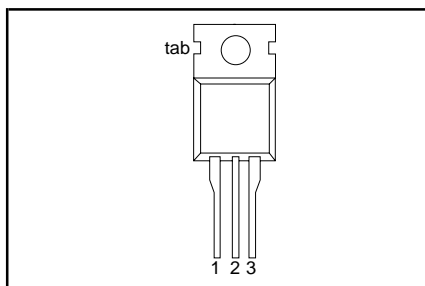
QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|--------------|----------------------------------|------|----------|
| V_{DS} | Drain-source voltage | 200 | V |
| I_D | Drain current (DC) | 3.5 | A |
| P_{tot} | Total power dissipation | 50 | W |
| $R_{DS(ON)}$ | Drain-source on-state resistance | 1.5 | Ω |

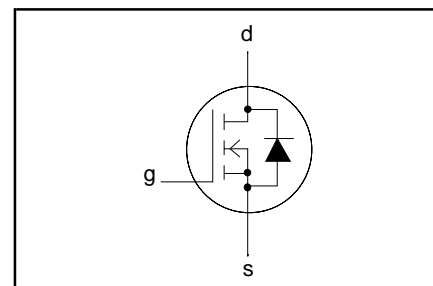
PINNING - TO220AB

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | gate |
| 2 | drain |
| 3 | source |
| tab | drain |

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|------------------------------|--|---|------|----------|------------------|
| I_D | Continuous drain current | $T_{mb} = 25\text{ }^\circ\text{C}; V_{GS} = 10\text{ V}$ $T_{mb} = 100\text{ }^\circ\text{C}; V_{GS} = 10\text{ V}$ | - | 3.5 | A |
| I_{DM} | Pulsed drain current | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 14 | A |
| P_D | Total dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ | - | 50 | W |
| $\Delta P_D / \Delta T_{mb}$ | Linear derating factor | $T_{mb} > 25\text{ }^\circ\text{C}$ | - | 0.33 | W/K |
| V_{GS} | Gate-source voltage | | - | ± 15 | V |
| V_{GSM} | Non-repetitive gate-source voltage | $t_p \leq 50\text{ }\mu\text{s}$ | - | ± 20 | V |
| E_{AS} | Single pulse avalanche energy | $V_{DD} \leq 50\text{ V};$ starting $T_j = 25\text{ }^\circ\text{C}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}$ | - | 25 | mJ |
| I_{AS} | Peak avalanche current | $V_{DD} \leq 50\text{ V};$ starting $T_j = 25\text{ }^\circ\text{C}; R_{GS} = 50\text{ }\Omega;$ $V_{GS} = 5\text{ V}$ | - | 3.5 | A |
| T_j, T_{stg} | Operating junction and storage temperature range | | -55 | 175 | $^\circ\text{C}$ |

THERMAL RESISTANCES

| SYMBOL | PARAMETER | CONDITIONS | TYP. | MAX. | UNIT |
|----------------|--|------------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance junction to mounting base | | - | 3 | K/W |
| $R_{th\ j-a}$ | Thermal resistance junction to ambient | | 60 | - | K/W |

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ELECTRICAL CHARACTERISTICS
 $T_j = 25\text{ °C}$ unless otherwise specified

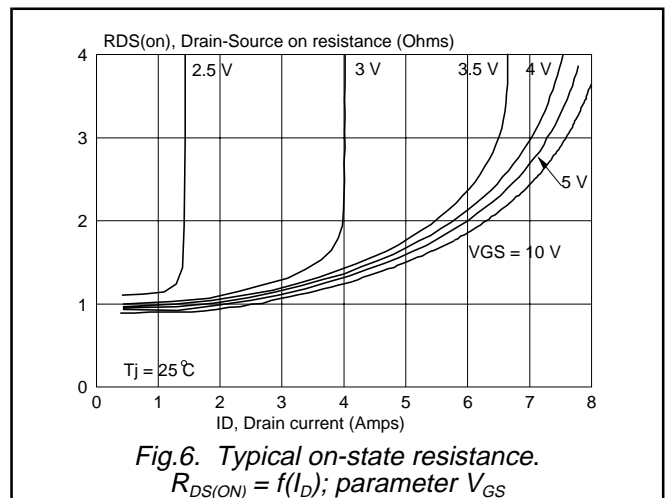
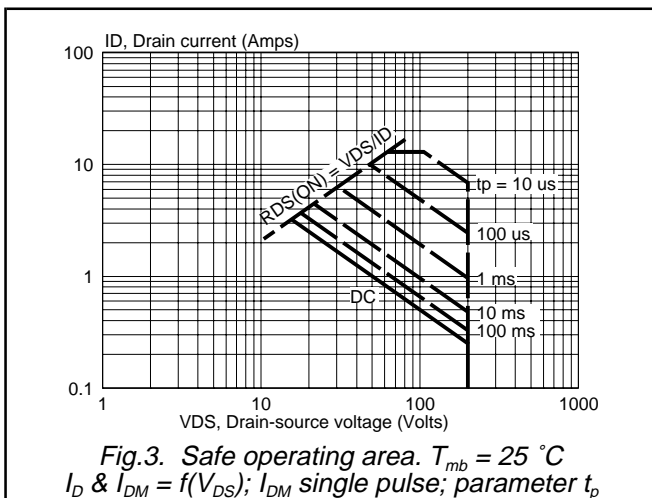
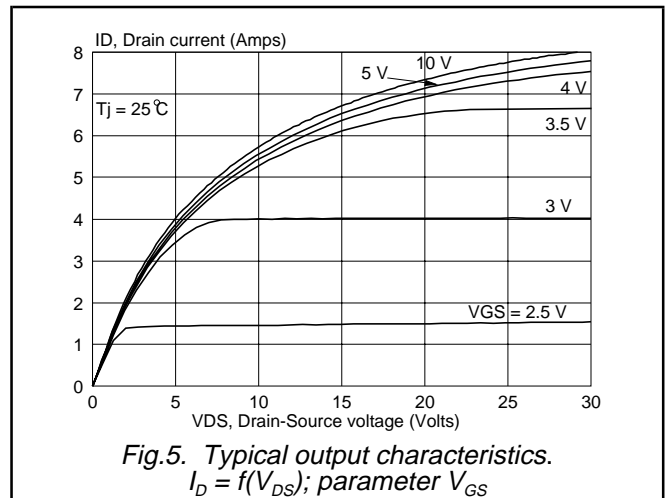
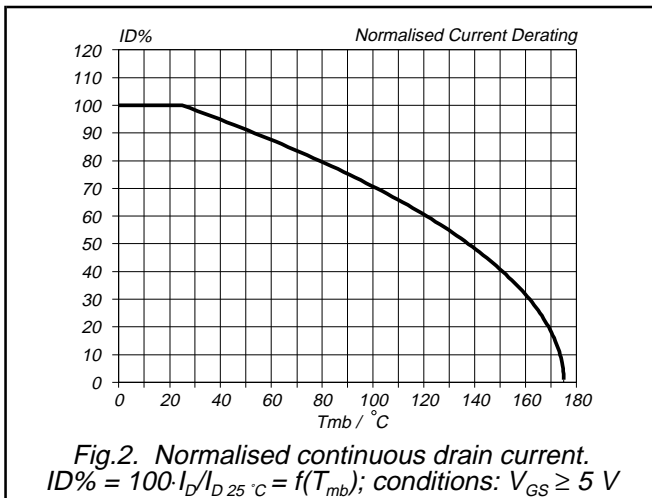
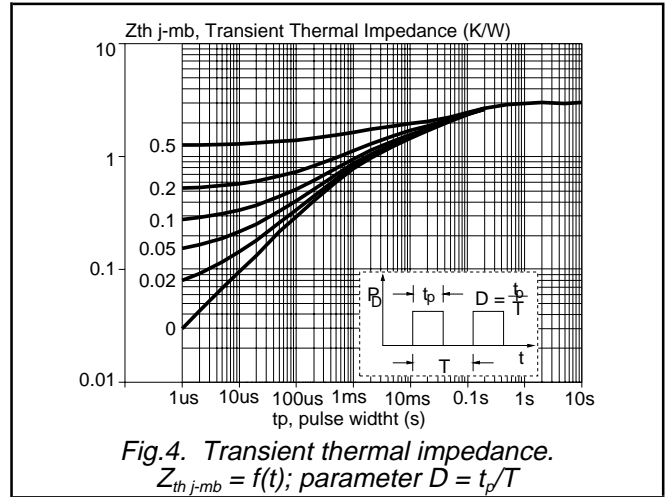
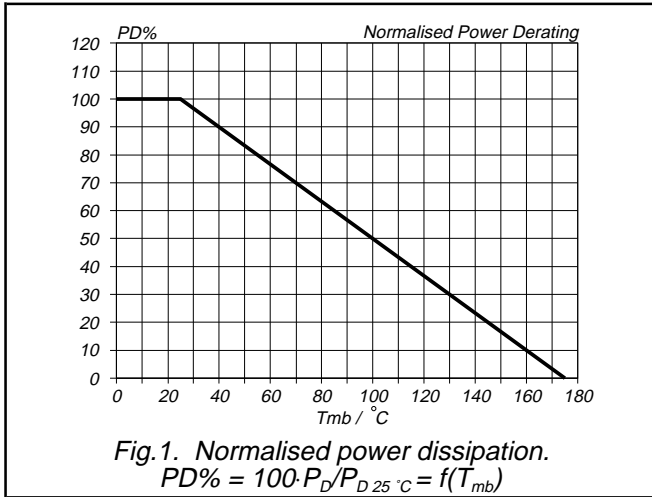
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|--|--|------|------|------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$ | 200 | - | - | V |
| $\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$ | Drain-source breakdown voltage temperature coefficient | $V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$ | - | 0.25 | - | V/K |
| $R_{DS(ON)}$ | Drain-source on resistance | $V_{GS} = 5\text{ V}; I_D = 2\text{ A}$ | - | 0.77 | 1.5 | Ω |
| $V_{GS(TO)}$ | Gate threshold voltage | $V_{DS} = V_{GS}; I_D = 0.25\text{ mA}$ | 1.0 | 1.5 | 2.0 | V |
| g_{fs} | Forward transconductance | $V_{DS} = 50\text{ V}; I_D = 2\text{ A}$ | 0.8 | 3.0 | - | S |
| I_{DSS} | Drain-source leakage current | $V_{DS} = 200\text{ V}; V_{GS} = 0\text{ V}$ | - | 0.1 | 25 | μA |
| I_{GSS} | Gate-source leakage current | $V_{DS} = 160\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$ $V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$ | - | 1 | 250 | μA |
| | | | - | 10 | 100 | nA |
| $Q_{g(tot)}$ | Total gate charge | $I_D = 3.3\text{ A}; V_{DD} = 160\text{ V}; V_{GS} = 5\text{ V}$ | - | 7.5 | 9 | nC |
| Q_{gs} | Gate-source charge | | - | 1 | 3 | nC |
| Q_{gd} | Gate-drain (Miller) charge | | - | 4 | 6 | nC |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 100\text{ V}; I_D = 3.3\text{ A};$ | - | 8 | - | ns |
| t_r | Turn-on rise time | $R_G = 24\ \Omega; R_D = 30\ \Omega$ | - | 33 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 40 | - | ns |
| t_f | Turn-off fall time | | - | 36 | - | ns |
| L_d | Internal drain inductance | Measured from contact screw on tab to centre of die | - | 3.5 | - | nH |
| L_d | Internal drain inductance | Measured from drain lead 6 mm from package to centre of die | - | 4.5 | - | nH |
| L_s | Internal source inductance | Measured from source lead 6 mm from package to source bond pad | - | 7.5 | - | nH |
| C_{iss} | Input capacitance | $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$ | - | 270 | - | pF |
| C_{oss} | Output capacitance | | - | 48 | - | pF |
| C_{rss} | Feedback capacitance | | - | 17 | - | pF |

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS
 $T_j = 25\text{ °C}$ unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|----------|--|--|------|------|------|---------------|
| I_S | Continuous source current (body diode) | $T_{mb} = 25\text{ °C}$ | - | - | 3.5 | A |
| I_{SM} | Pulsed source current (body diode) | $T_{mb} = 25\text{ °C}$ | - | - | 14 | A |
| V_{SD} | Diode forward voltage | $I_S = 3.3\text{ A}; V_{GS} = 0\text{ V}$ | - | - | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_S = 3.3\text{ A}; V_{GS} = 0\text{ V};$ $di/dt = 100\text{ A}/\mu\text{s}$ | - | 90 | - | ns |
| Q_{rr} | Reverse recovery charge | | - | 0.5 | - | μC |

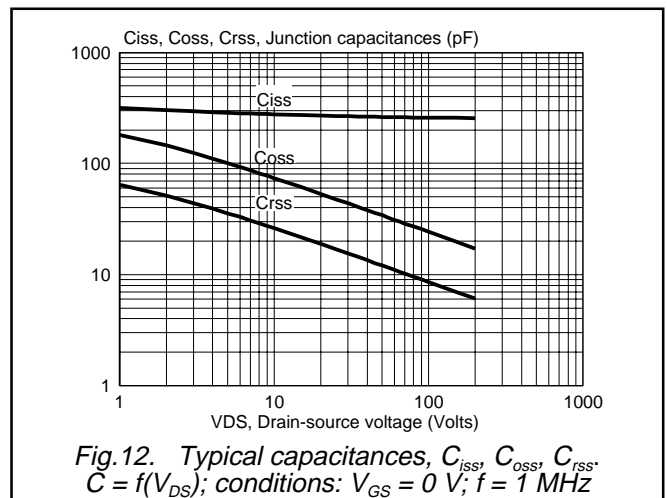
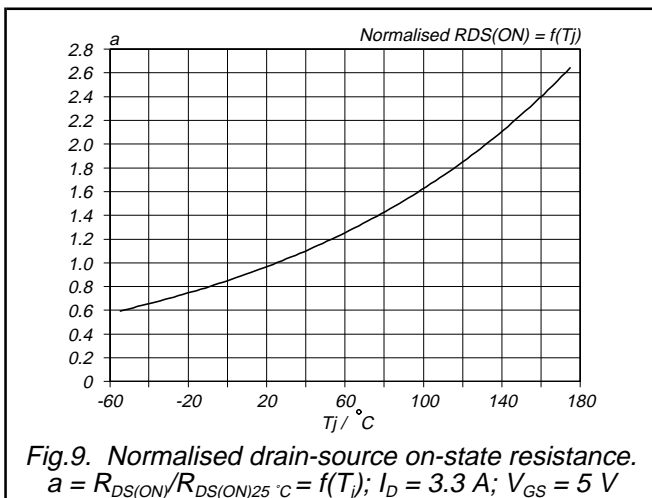
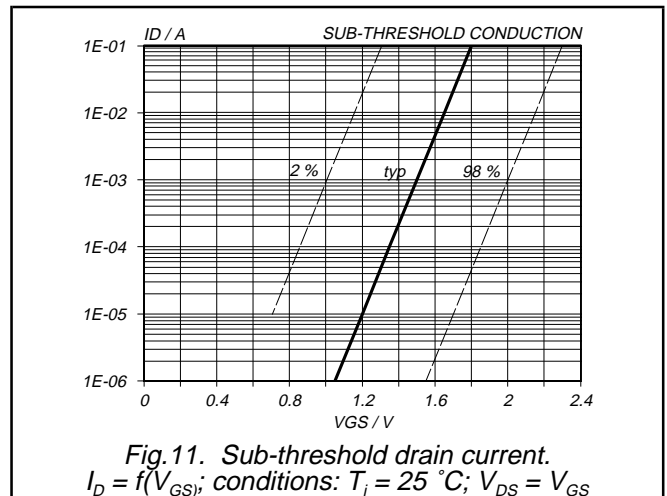
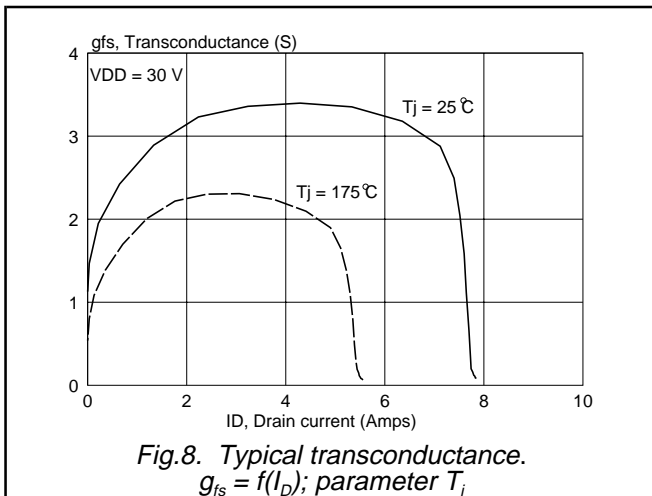
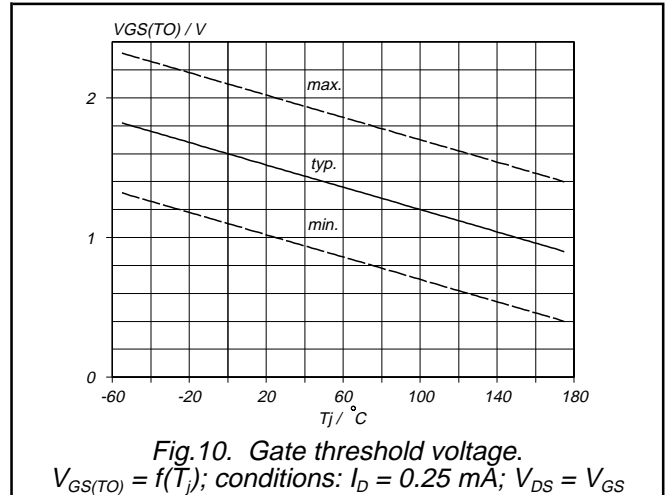
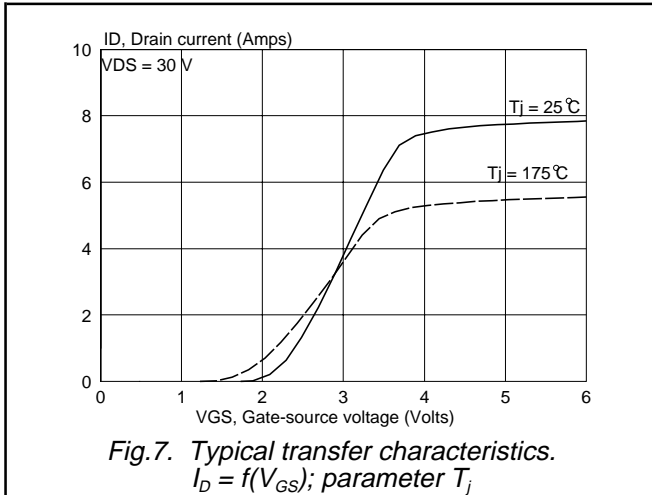
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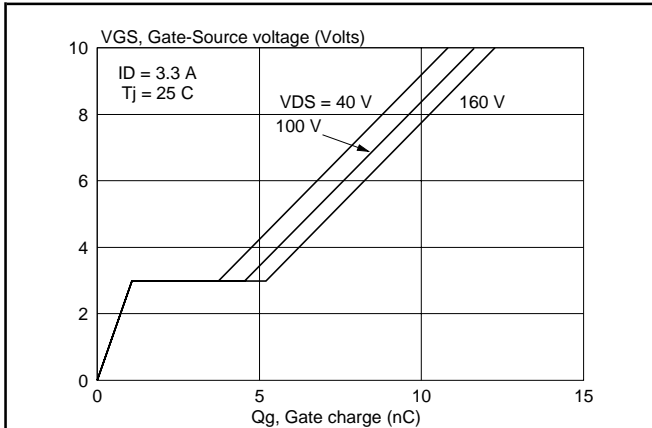


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

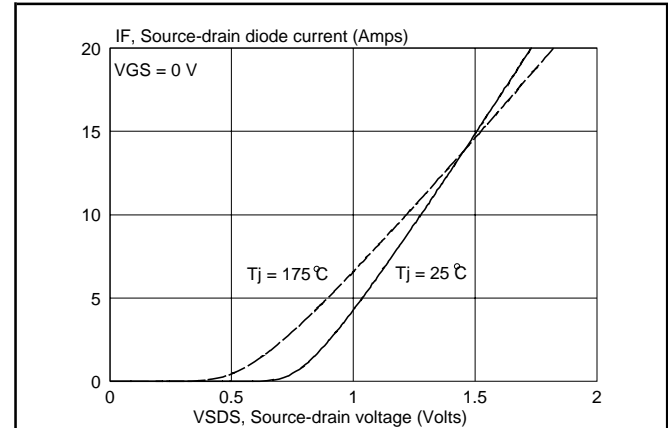


Fig.16. Source-Drain diode characteristic.
 $I_F = f(V_{SDS})$; parameter T_j

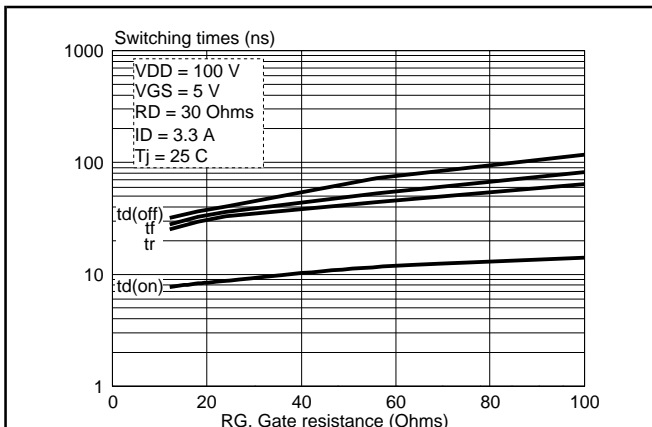


Fig.14. Typical switching times.
 $t_{d(on)}, t_r, t_{d(off)}, t_f = f(R_G)$

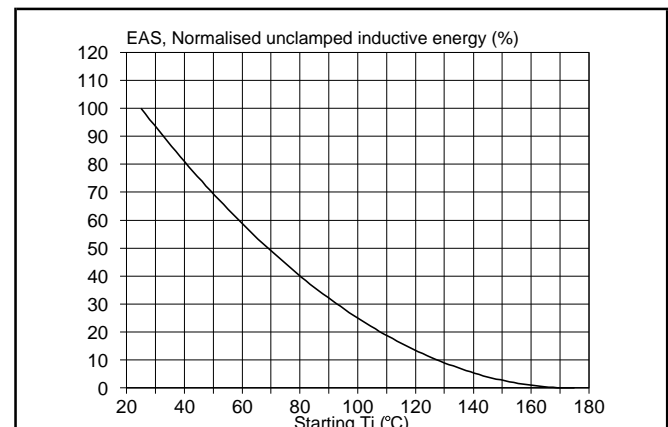


Fig.17. Normalised unclamped inductive energy.
 $E_{AS} \% = f(T_j)$

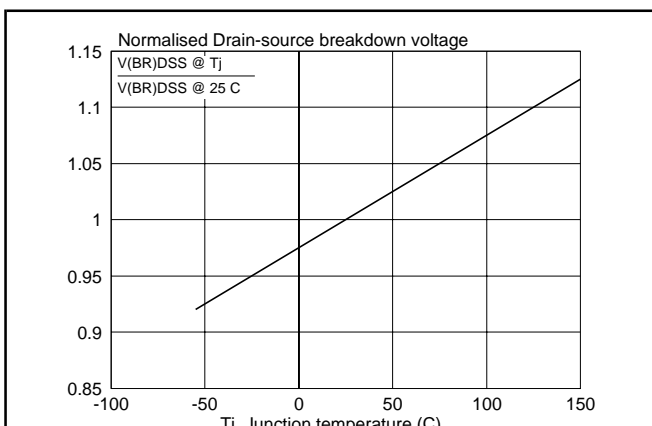


Fig.15. Normalised drain-source breakdown voltage.
 $V_{(BR)DSS} / V_{(BR)DSS 25^\circ C} = f(T_j)$

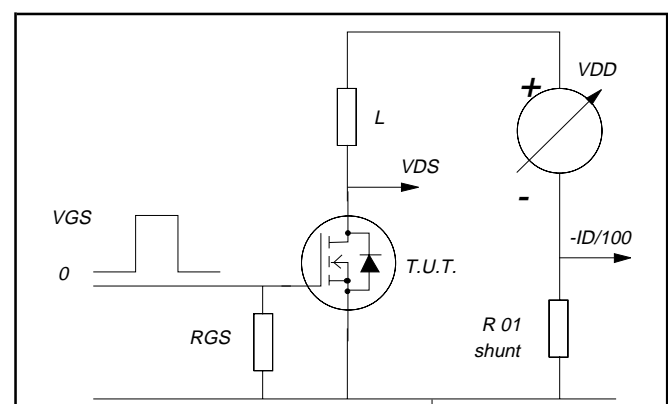
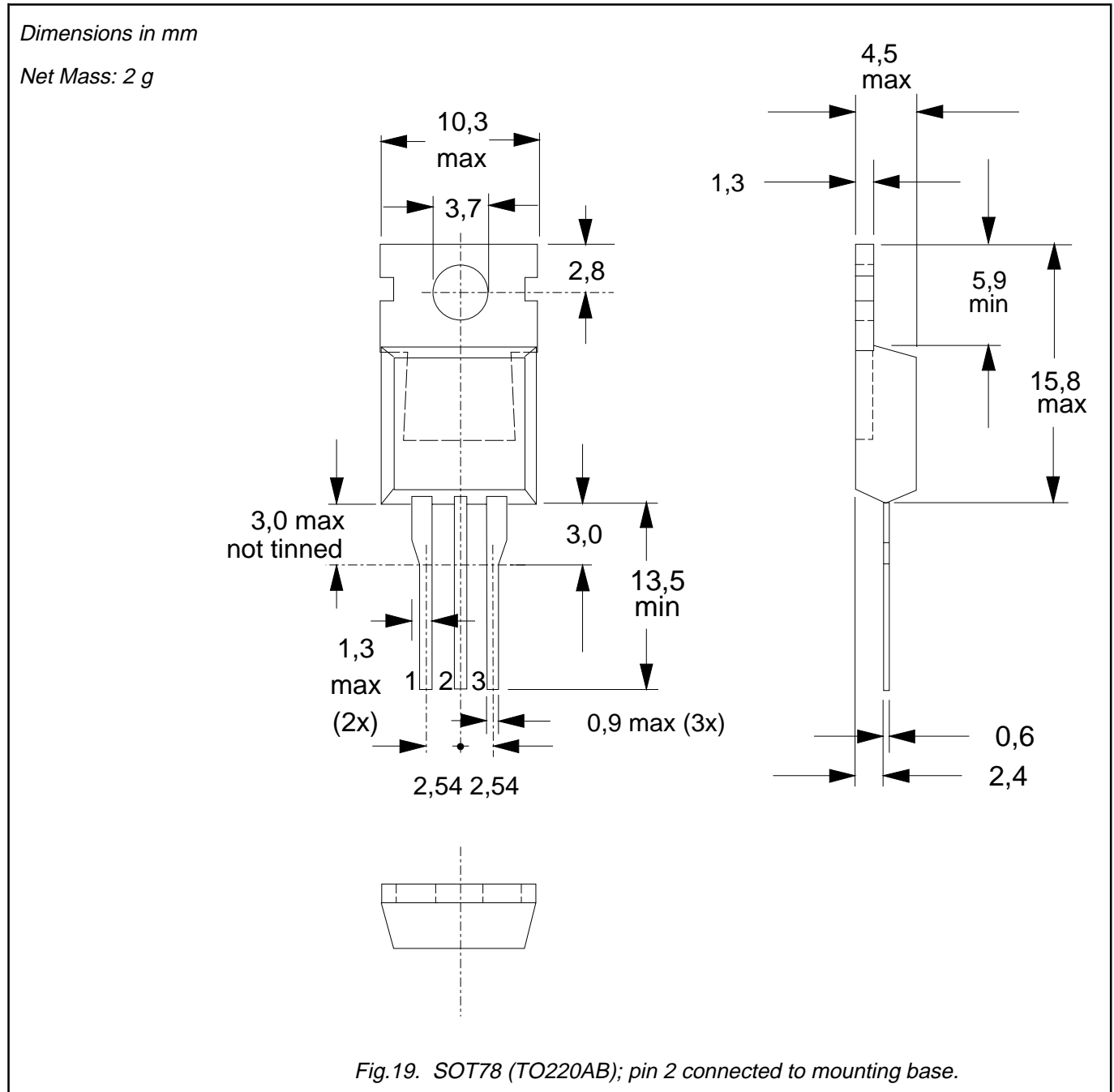


Fig.18. Unclamped inductive test circuit.
 $E_{AS} = 0.5 \cdot L I_D^2 \cdot V_{(BR)DSS} / (V_{(BR)DSS} - V_{DD})$

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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

| | |
|--|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |
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