

**PowerMOS transistors
Avalanche energy rated**

PHU2N50E

FEATURES

- Repetitive Avalanche Rated
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance
- Extremely high dV/dt capability

QUICK REFERENCE DATA

$V_{DSS} = 500\text{ V}$
$I_D = 2\text{ A}$
$R_{DS(ON)} \leq 5\ \Omega$

GENERAL DESCRIPTION

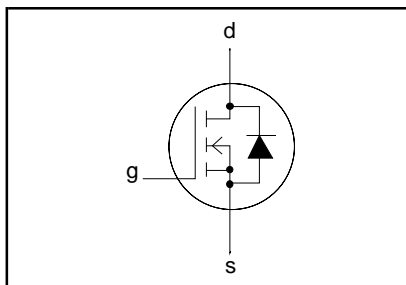
N-channel, enhancement mode field-effect power transistor, intended for use in **Compact Fluorescent Lamps (CFL)** and low power ballasts. The PHU2N50E is compatible with self oscillating and IC driven circuits, including the UBA2021 ballast controller IC. Other applications include off line switched mode power supplies and D.C. to D.C. converters.

The PHU2N50E is supplied in the SOT533 (I-PAK) leaded package.

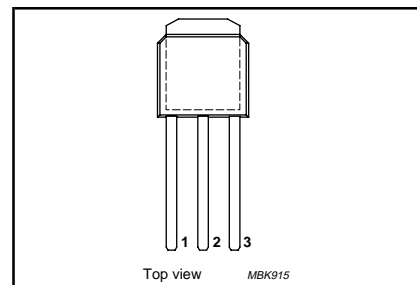
PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SYMBOL



SOT533



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$	-	500	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	500	V
V_{GS}	Gate-source voltage		-	± 30	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$ $T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	2	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	1.3	A
P_D	Total dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	8	W
dV/dt	Peak Diode Recovery voltage slope. (See fig. 19)	$I_{ds} = 2.0\text{ A}$; $dl/dt = 100\text{ A}/\mu\text{s}$; $V_s = 8\text{ V}$; $T_j < T_{jmax}$	-	5.2	V/ns
T_j, T_{stg}	Operating junction and storage temperature range		- 55	150	$^\circ\text{C}$

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AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, $I_{AS} = 1.26$ A; $t_p = 0.2$ ms; T_j prior to avalanche = 25 °C; $V_{DD} \leq 50$ V; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig:17	-	82	mJ
E_{AR}	Repetitive avalanche energy ¹	$I_{AR} = 2$ A; $t_p = 2.5$ μ s; T_j prior to avalanche = 25 °C; $R_{GS} = 50$ Ω ; $V_{GS} = 10$ V; refer to fig:18	-	3.3	mJ
I_{AS}, I_{AR}	Repetitive and non-repetitive avalanche current		-	2	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	In free air	-	70	-	K/W

ELECTRICAL CHARACTERISTICS

 $T_j = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0.25$ mA	500	-	-	V
$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	Drain-source breakdown voltage temperature coefficient	$V_{DS} = V_{GS}$; $I_D = 0.25$ mA	-	0.1	-	%/K
$R_{DS(ON)}$	Drain-source on resistance	$V_{GS} = 10$ V; $I_D = 1$ A	-	3.1	5	Ω
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 0.25$ mA	2.0	3.0	4.0	V
g_{fs}	Forward transconductance	$V_{DS} = 30$ V; $I_D = 1$ A	0.5	1.3	-	S
I_{DSS}	Drain-source leakage current	$V_{DS} = 500$ V; $V_{GS} = 0$ V	-	1	25	μ A
		$V_{DS} = 500$ V; $V_{GS} = 0$ V; $T_j = 125$ °C	-	77	250	μ A
I_{GSS}	Gate-source leakage current	$V_{GS} = \pm 30$ V; $V_{DS} = 0$ V	-	10	200	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 2$ A; $V_{DD} = 400$ V; $V_{GS} = 10$ V	-	20	25	nC
Q_{gs}	Gate-source charge		-	2	3	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	15	nC
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250$ V; $R_D = 120$ Ω ;	-	10	-	ns
t_r	Turn-on rise time	$R_G = 24$ Ω	-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Turn-off fall time		-	20	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; $f = 1$ MHz	-	236	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Feedback capacitance		-	22	-	pF

¹ pulse width and repetition rate limited by T_j max.

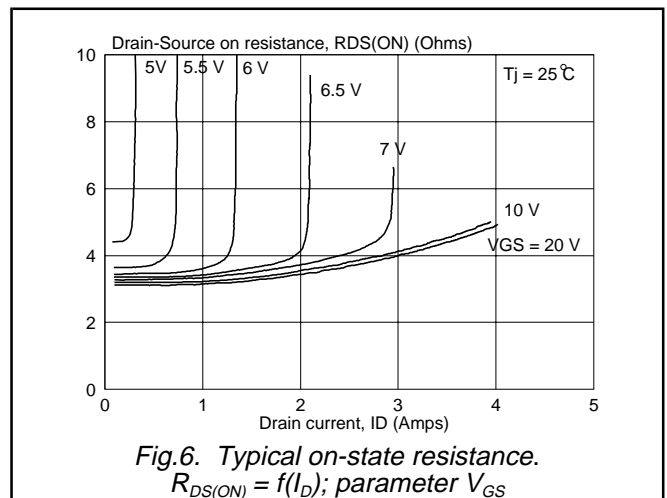
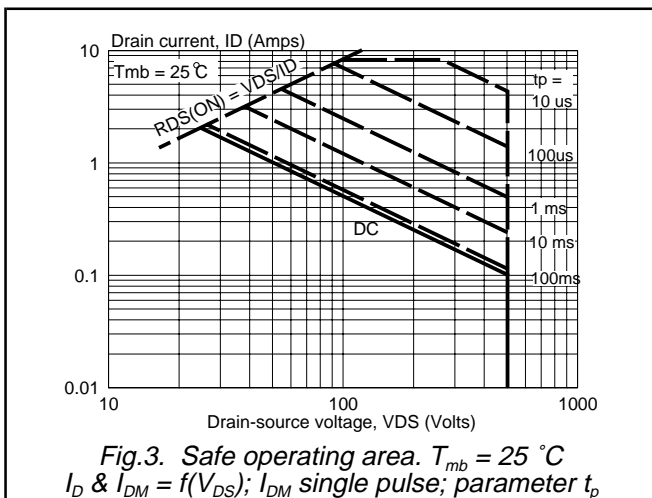
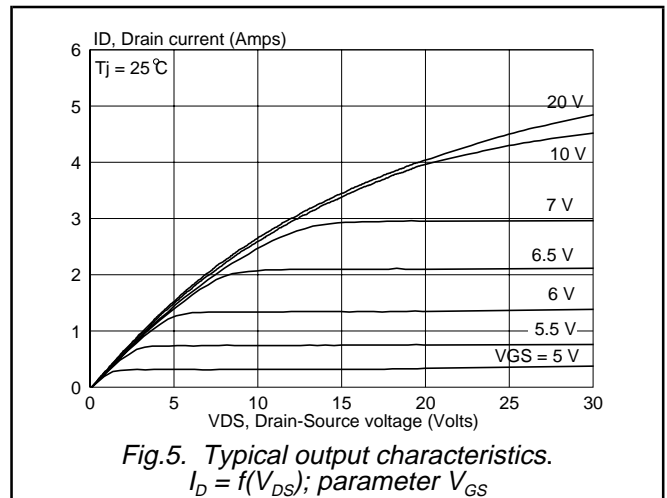
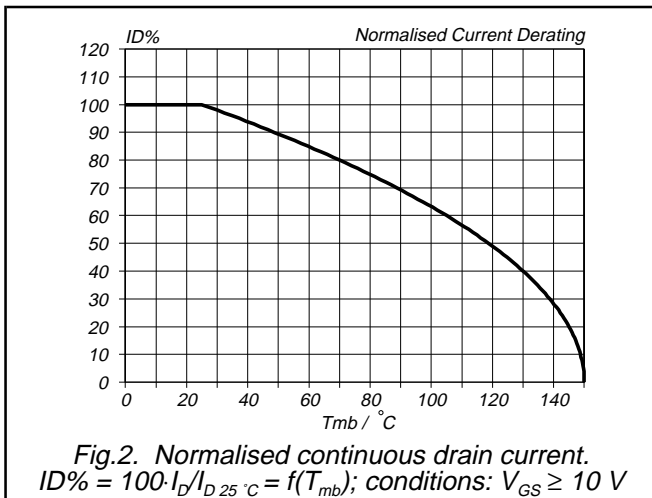
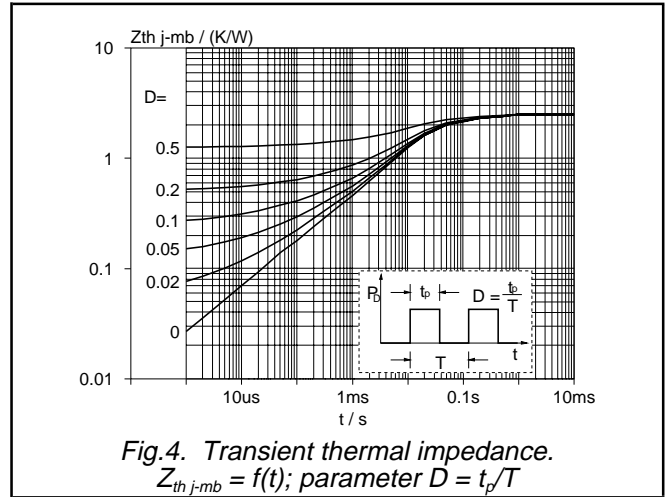
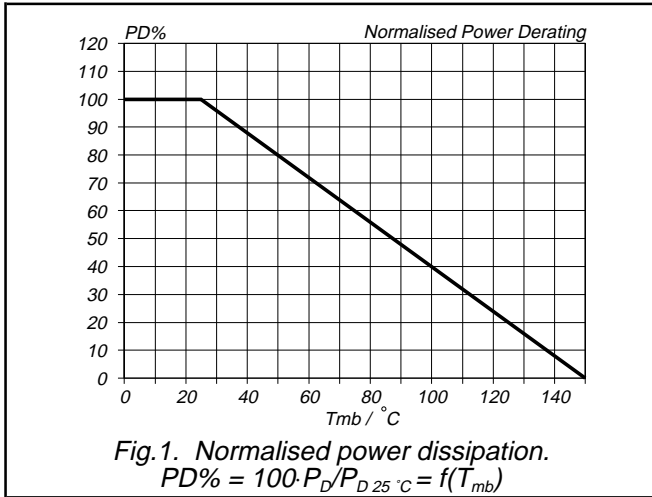
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PHU2N50E**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS** $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	-	2	A
I_{SM}	Pulsed source current (body diode)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	-	8	A
V_{SD}	Diode forward voltage	$I_S = 2\text{ A}; V_{GS} = 0\text{ V}$	-	-	1.2	V
t_{rr}	Reverse recovery time	$I_S = 2\text{ A}; V_{GS} = 0\text{ V}; di/dt = 100\text{ A}/\mu\text{s}$	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	2.1	-	μC

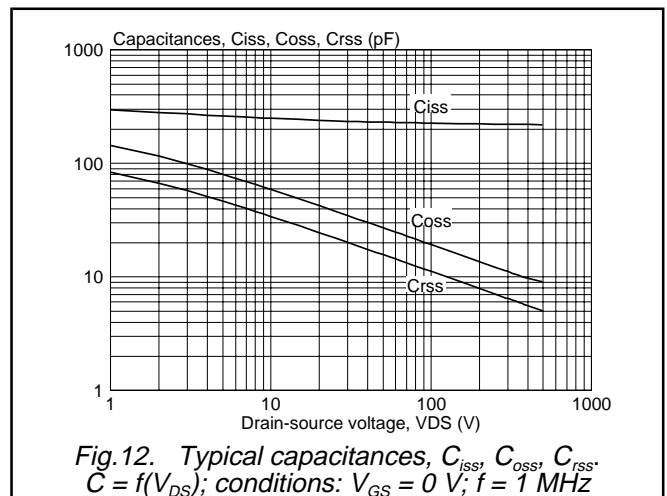
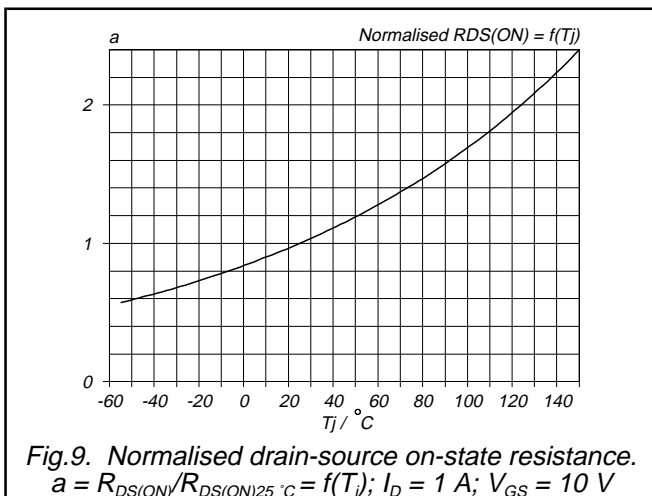
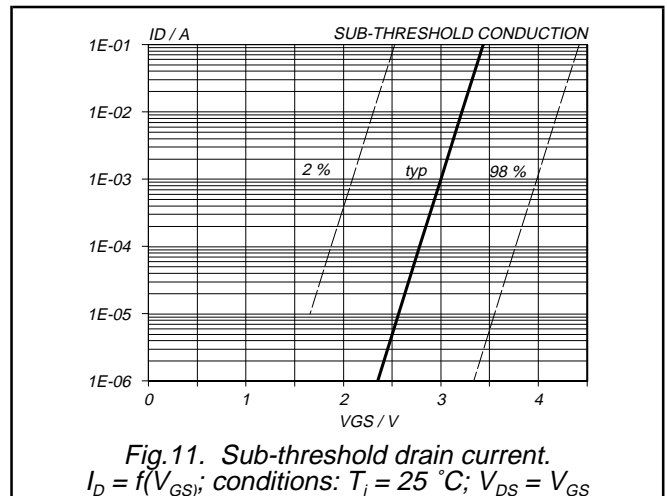
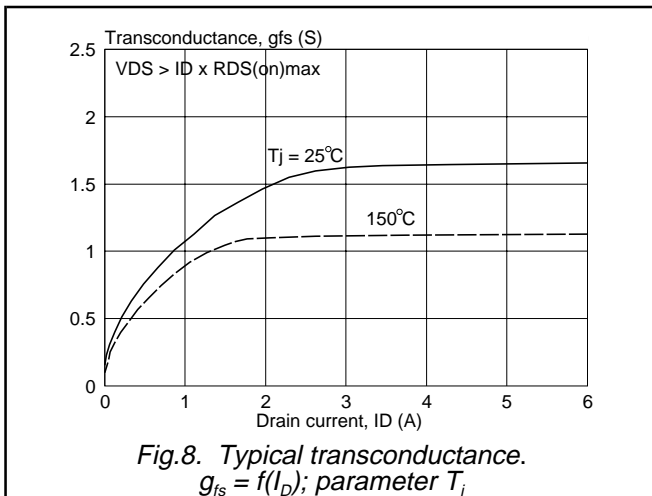
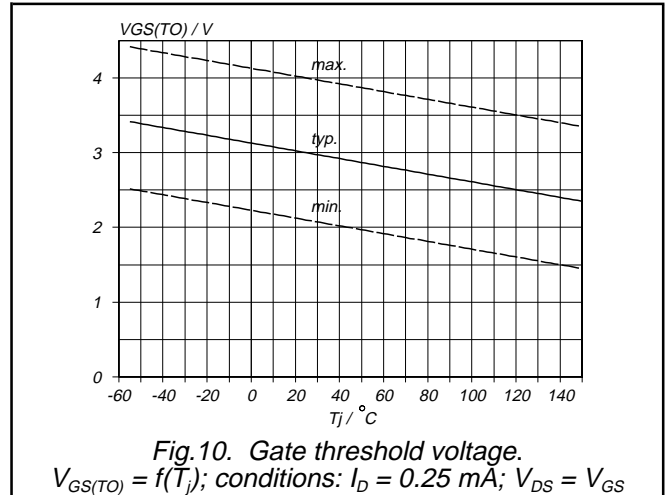
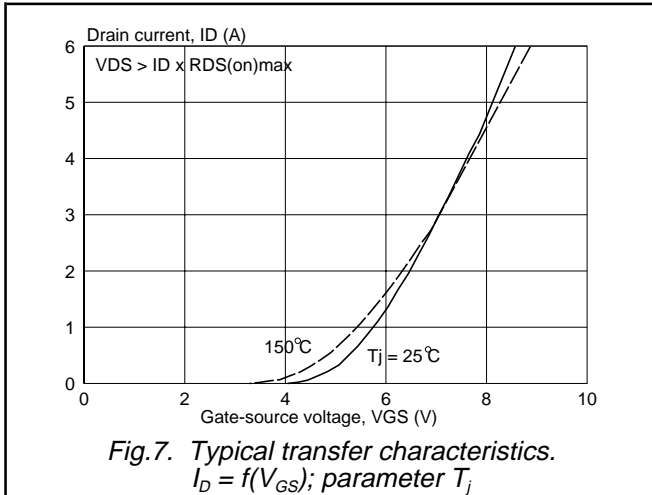
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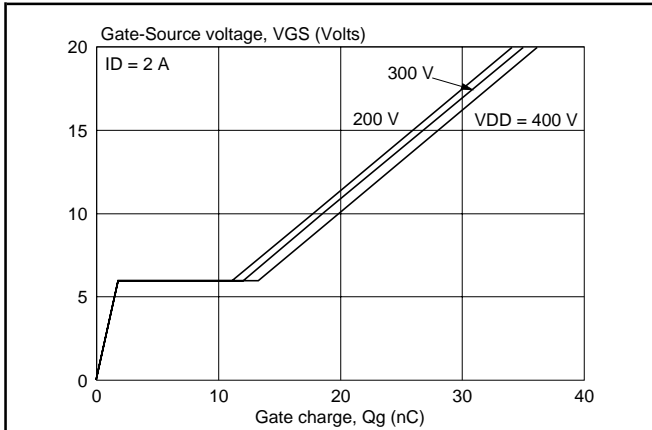


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; parameter V_{DS}

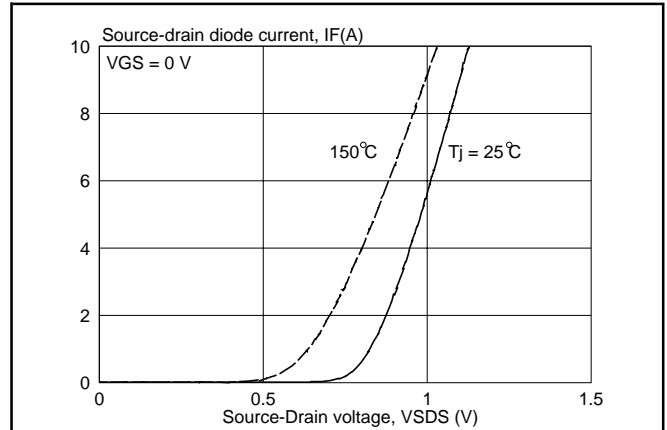


Fig. 16. Source-Drain diode characteristic.
 $I_F = f(V_{SDS})$; parameter T_j

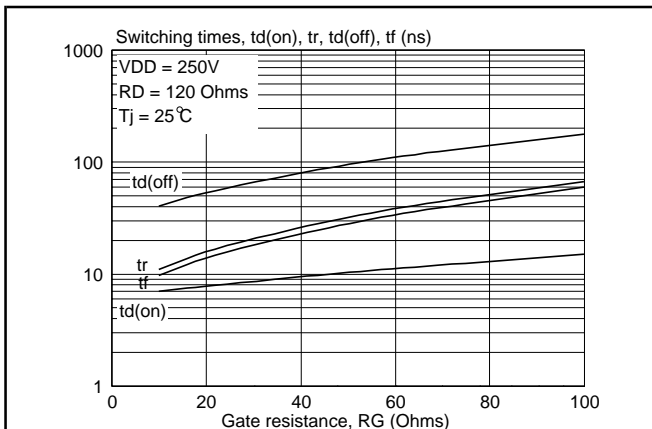


Fig. 14. Typical switching times; $t_{d(on)}$, t_r , $t_{d(off)}$, $t_f = f(R_G)$

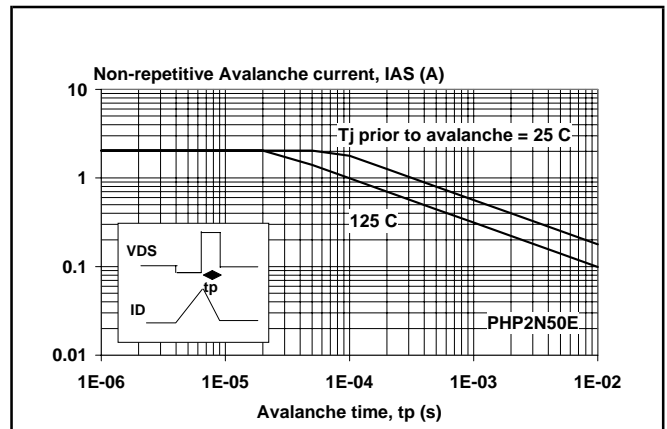


Fig. 17. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_p); unclamped inductive load

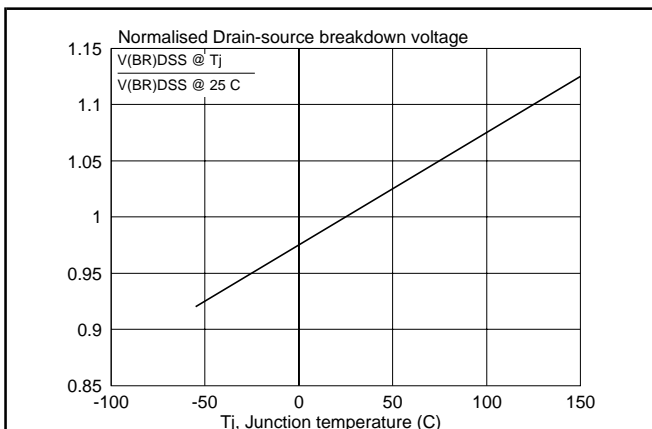


Fig. 15. Normalised drain-source breakdown voltage;
 $V_{(BR)DSS} / V_{(BR)DSS 25^\circ C} = f(T_j)$

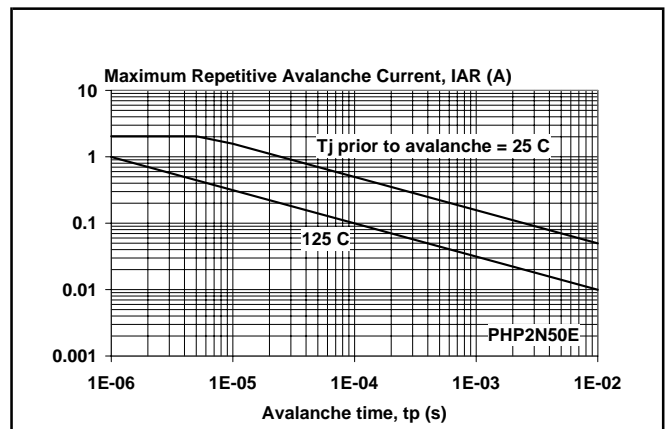
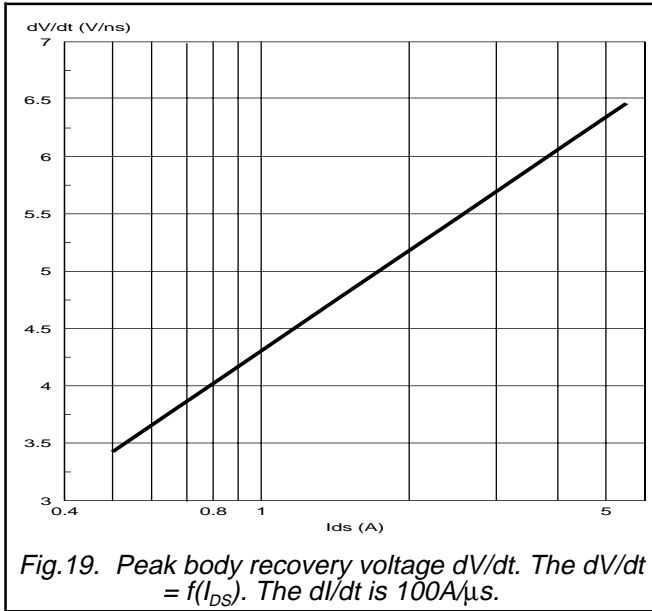


Fig. 18. Maximum permissible repetitive avalanche current (I_{AR}) versus avalanche time (t_p)

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MECHANICAL DATA

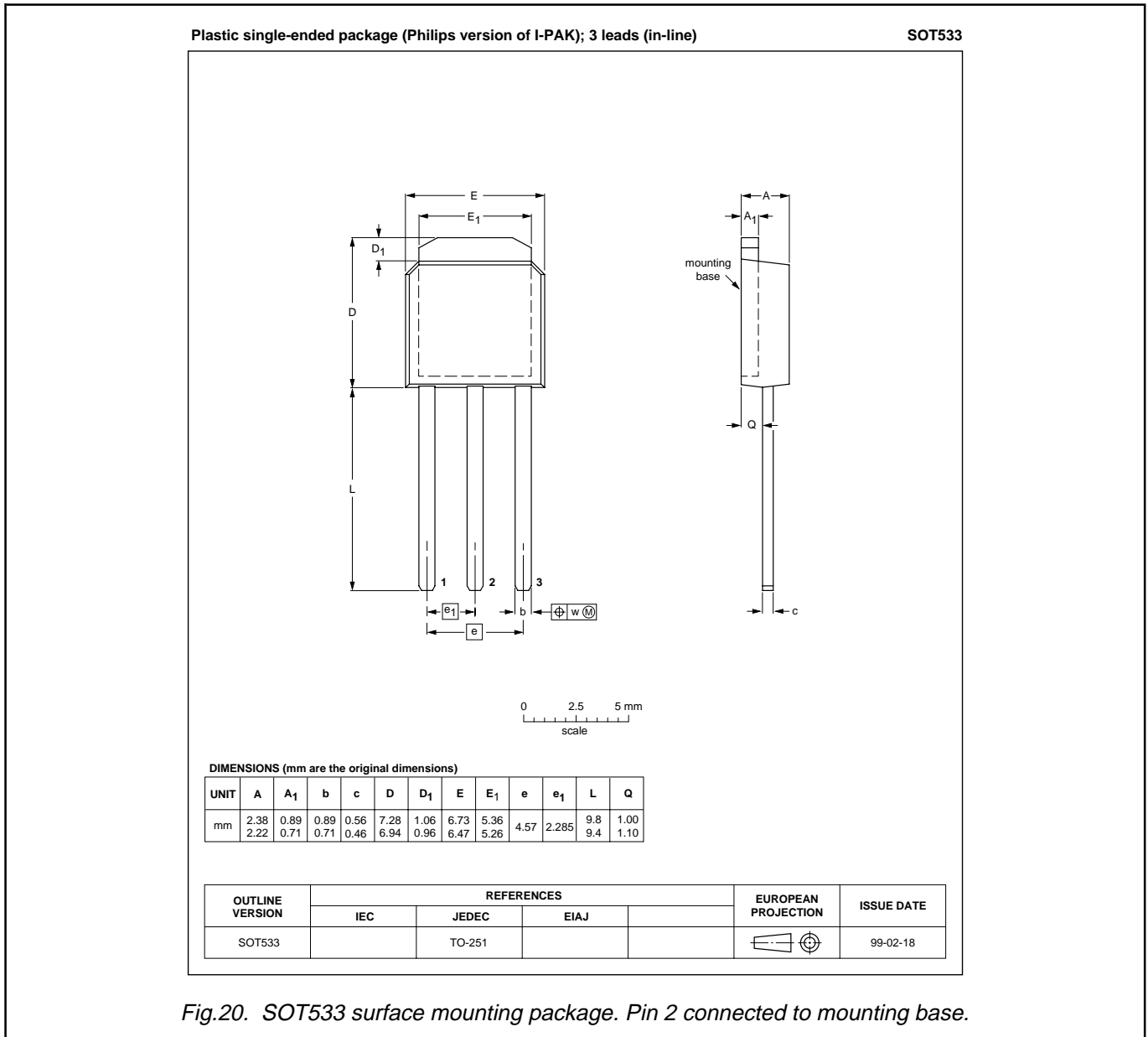


Fig.20. SOT533 surface mounting package. Pin 2 connected to mounting base.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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