DATA SHEET

SAA4963
Integrated NTSC comb filter

Preliminary specification
Supersedes data of 1996 Nov 22
File under Integrated Circuits, IC02

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Philips
Semiconductors

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FEATURES

- One chip NTSC comb filter
- Time discrete but continuous amplitude signal processing with analog interfaces
- Internal delay lines, filters, clock processing and signal switches
- Alignment-free
- Few external components.

GENERAL DESCRIPTION

The SAA4963 is an alignment-free one chip comb filter compatible with NTSC M systems.

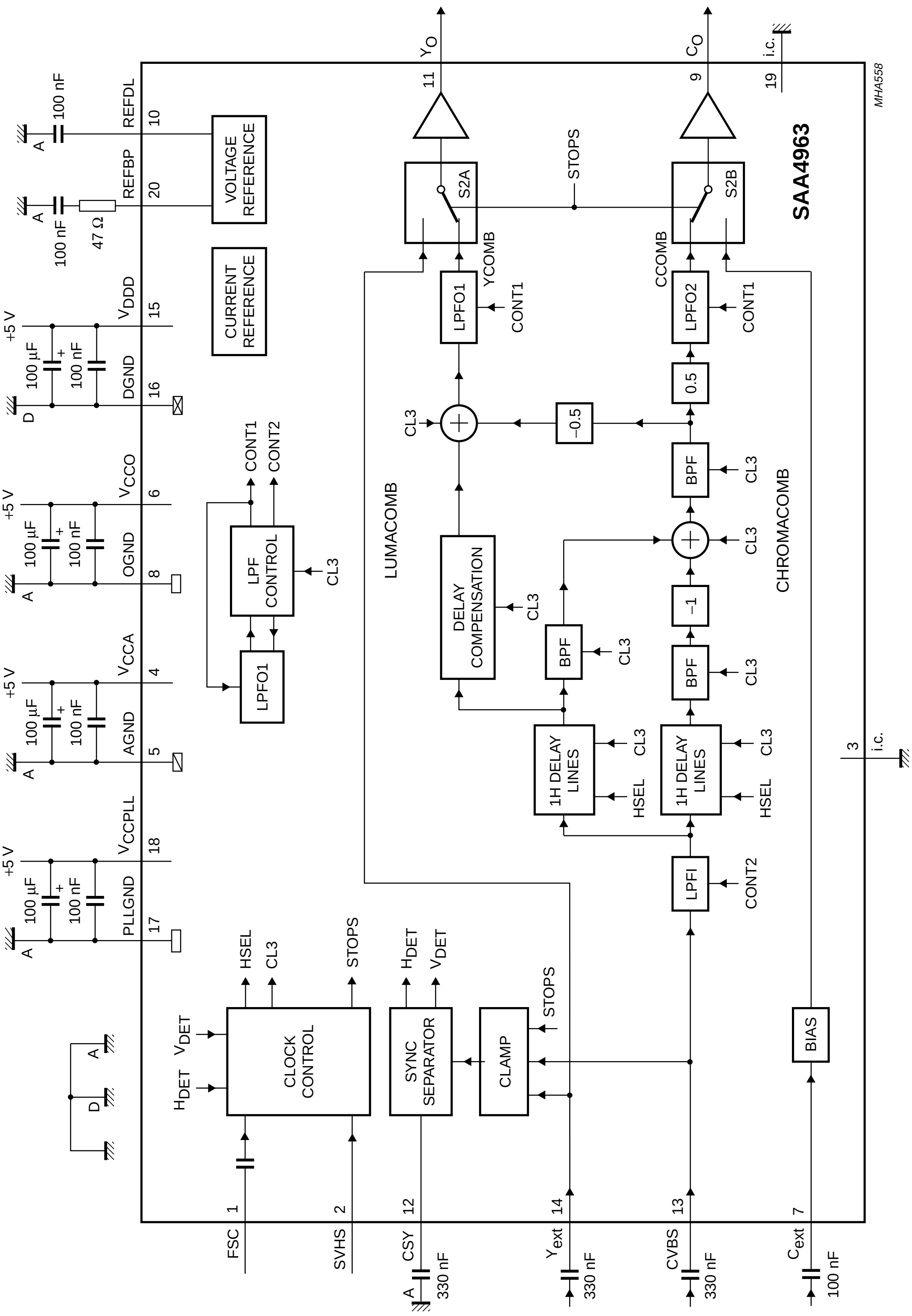
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.75	5	5.5	V
V_{DDD}	digital supply voltage	4.75	5	5.5	V
V_{CCO}	analog supply voltage output buffer	4.75	5	5.5	V
V_{CCPLL}	analog supply voltage PLL	4.75	5	5.5	V
I_{CCO}	analog supply current output buffer	–	35	45	mA
I_{DDD}	digital supply current	–	3	6	mA
I_{CCA}	analog supply current	–	10	17	mA
I_{CCPLL}	analog supply current PLL	–	1.5	2.5	mA
$V_{13(p-p)}$	CVBS input signal (peak-to-peak value)	0.7	1	1.4	V
$V_{14(p-p)}$	luminance input signal (peak-to-peak value)	0.7	1	1.4	V
$V_{7(p-p)}$	chrominance input signal (peak-to-peak value)	–	0.7	1	V
$V_{1(p-p)}$	subcarrier input signal (peak-to-peak value)	100	200	400	mV
$V_{11(p-p)}$	luminance output signal (peak-to-peak value)	0.6	1	1.54	V
$V_{9(p-p)}$	chrominance output signal (peak-to-peak value)	–	0.7	1.1	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA4963	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
SAA4963T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

BLOCK DIAGRAM



Remark: all switches in LOW position.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
FSC	1	subcarrier frequency input
SVHS	2	SVHS mode forcing
i.c.	3	internally connected
V_{CCA}	4	analog supply voltage
AGND	5	analog ground
V_{CCO}	6	analog supply voltage output buffer
C_{ext}	7	external chrominance input
OGND	8	analog ground output buffer
C_O	9	chrominance output signal
REFDL	10	decoupling capacitor for delay lines
Y_O	11	luminance output signal
CSY	12	storage capacitor
CVBS	13	CVBS input signal
Y_{ext}	14	external luminance input
V_{DDD}	15	digital supply voltage
DGND	16	digital ground
PLLGND	17	analog ground PLL
V_{CCPLL}	18	analog supply voltage PLL
i.c.	19	internally connected
REFBP	20	decoupling capacitor for band-pass filter reference

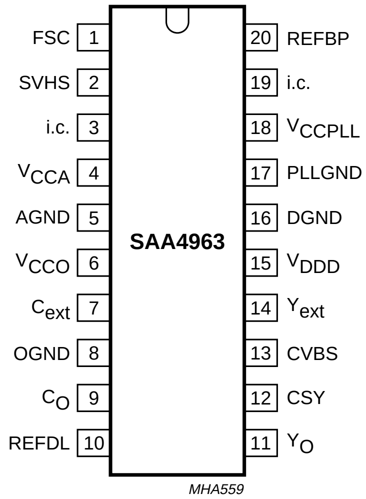


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Functional requirements

The NTSC comb filter processes the video standard NTSC M. For SVHS signals the input signals are bypassed to the output without processing by selecting the SVHS mode.

A sync separation circuit is incorporated to generate control signals for the internal clock processing. With a sync compression of up to 12 dB (see Fig.5) the sync separator works properly.

The IC is controlled via the pin SVHS (pin 2) which forces the IC into the SVHS mode (bypass) if the comb filter function is not desired. It is possible to select the following modes:

COMB-mode: Luminance and chrominance comb filter function active, if SVHS mode not active

SVHS-mode: No IC function active, all clocks inactive, C_{ext} (pin 7) is bypassed to C_O (pin 9) and Y_{ext} (pin 14) is bypassed to Y_O (pin 11). This mode is forced via SVHS (pin 2).

The mode changes from SVHS to COMB and vice versa are always performed asynchronously with respect to the vertical blanking interval.

Pin description

FSC (PIN 1)

Input for the reference frequency f_{sc} (see note 3 of Chapter “Characteristics”). For SVHS signals the signal performance can be increased by switching the input signal at FSC off.

SVHS (PIN 2)

Input signal that controls the operation mode. An internal low-pass filter suppresses the subcarrier frequencies. Thus applications are supported where the operation mode (COMB or SVHS) is controlled by the DC level of the FSC input signal at pin 1. For those applications the SVHS input can be externally connected to FSC (pin 1).

Table 1 SVHS function

SVHS	SELECTED MODE
LOW	COMB
HIGH	SVHS (PLL and clock processing stopped)

The PLL and the clock processing are always stopped if the selected level for SVHS is applied to SVHS (independent of the vertical pulse).

V_{CCA}, V_{CCO}, V_{DDD} AND V_{CCPLL} (PINS 4, 6, 15 AND 18)

Supply voltages.

AGND, OGND, DGND AND PLLGND (PINS 5, 8, 16 AND 17)

Ground connection. AGND is used as signal reference for all analog input and output signals.

C_{ext} (PIN 7)

Input for an external chrominance signal which is correlated with the external VBS signal in SVHS-mode.

C_O (PIN 9)

Chrominance output signal. This output delivers the comb filtered chrominance from the CVBS signal in COMB-mode or the external chrominance signal from the input C_{ext} if the IC is forced into the SVHS-mode.
In COMB-mode the output is delayed by an additional processing delay.

Table 2 C_O output signal

MODE	C_O OUTPUT SIGNAL
COMB	comb filtered chrominance signal
SVHS	external chrominance signal from C_{ext} input

REFDL (PIN 10)

Decoupling capacitor for the delay line reference voltage.

Y_O (PIN 11)

VBS output signal. This output delivers the comb filtered luminance signal (including synchronization pulses) in COMB-mode or the external (C)VBS signal from the input Y_{ext} if the IC is forced into SVHS-mode. In COMB-mode the output is delayed by an additional processing delay.

Table 3 Y_O output signal

MODE	Y_O OUTPUT SIGNAL
COMB	comb filtered luminance signal
SVHS	external (C)VBS signal from Y_{ext} input

CSY (PIN 12)

Sync top capacitor for the sync separator.

CVBS (PIN 13)

Input for the CVBS signal in COMB-mode.

Y_{EXT} (PIN 14)

Input for an external luminance signal in SVHS-mode.

REFBP (PIN 20)

Decoupling capacitor for the band-pass filter reference voltage.

Internal functional description

SWITCHED CAPACITOR DELAY LINE

Delays the CVBS input signal by 1 line. Input signals for the delay lines are the CVBS signal, the clock CL3 ($3 \times f_{sc}$) and the control signal HSEL.

Output signals are the non-delayed and the 1-line delayed CVBS signal.

SWITCHED CAPACITOR BAND-PASS FILTERS (BPFS)

The comb filter input BPFs attenuate the low frequencies to guarantee a correct signal processing within the comb filter.

The comb filter output BPF reduces the alias components that are the result of the signal processing within the comb filter.

CHROMINANCE COMB FILTER

Separates the chrominance from the band-pass filtered CVBS signal.

DELAY COMPENSATION

Compensates the internal processing time of the band-pass filters and the chrominance comb filter section.

LUMINANCE COMB FILTER

The comb filtered luminance output signal is obtained by adding the delayed CVBS signal and the inverted comb filtered chrominance signal.

LOW-PASS FILTER INPUT (LPFI)

Analog input low-pass filter to reduce the outband frequencies of EMC. The input low-pass filter is included in the signal path.

LOW-PASS FILTER OUTPUTS (LPFO1 AND LPFO2)

Two different types of output low-pass filters LPFO1 and LPFO2 are necessary to get equal signal delays within the luminance path and the chrominance path (important for good transient behaviour). The low-pass output filter type LPFO1 is used for the luminance output while LPFO2 is used for the chrominance output. The filters are analog 3rd order elliptic low-pass filters that convert the output signals from the time discrete to the time continuous domain (reconstruction filter).

LPF CONTROL

Automatic tuning of the low-pass filters is achieved by adjusting the filter delays. The control information for all filters (CONT1 and CONT2) is derived from a built-in reference filter (LPFO1-type) that is part of a control loop. The control loop tunes the reference filter delay and thus all other filter delays to a time reference derived from the system clock CL3.

CONTROL AND CLOCK PROCESSING (CLOCK CONTROL)

The control and clock processing block consists of the sub-blocks PLL, clock processing and mode control. Only if the input level at SVHS (pin 2) selects the COMB mode the PLL and the clock processing are released for operation.

Main tasks of the control and clock processing are:

- Clock generation of system clock CL3
- Delay line start control
- Mode control.

The signal processing is based on a $3 \times f_{sc}$ system clock (CL3), that is generated by the clock processing from the f_{sc}-signal at FSC (pin 1) via a PLL. A clock phase correction of 180° is necessary every line because the subcarrier frequency divided by the line frequency results not in an integer value. Additionally the clock processing is synchronized fieldwise by the H-signal (correction of line frequency instabilities).

The PLL provides a master clock MCK of $6 \times f_{sc}$, which is locked to the subcarrier frequency at FSC (pin 1).
The system clock CL3 ($3 \times f_{sc}$) is obtained from MCK by a divide-by-two circuit. The 180° phase shift is generated by stopping the divide-by-two circuit for one MCK clock cycle.

The generated clock is a pseudo-line-locked clock that is referenced to f_{sc}. The sync separator generates the necessary signals H_{DET} and V_{DET} indicating the line (H) and the field (V) sync periods.

The input signals of the control and clock processing (CLOCK CONTROL) are:

H_{DET}: analog horizontal pulse from sync separator

V_{DET}: analog vertical pulse from sync separator

FSC: subcarrier frequency

SVHS: SVHS control signal.

The output signals are:

CL3: system clock ($3 \times f_{sc}$)

HSEL: line start signal for the delay line

STOPS: forces the IC via the switches S2A and S2B into the SVHS-mode or into COMB-mode (always asynchronous).

HORIZONTAL AND VERTICAL SYNC SEPARATOR

A built-in sync separator circuit generates the H_{DET} and V_{DET} signals from the CVBS input signal. This circuit is still working properly with a 12 dB attenuated sync in a normal 700 mV black-to-white video input signal (see Fig.5).

CLAMP

The black level clamping of the video input signals (CVBS and Y_{ext}) is performed by the sync separator stage.
The clamping level is nearly adequate to the voltage at REFDL (pin 10). The clamp consists of a pre clamp and a main clamp. Always the signal which is switched to the output is clamped via the main clamp while the other signal is pre clamped. This reduces the distortion during switching from COMB-mode to SVHS-mode and vice versa.

Table 4 Function of pre clamp and main clamp

INPUT	COMB-MODE	SVHS-MODE
CVBS	main clamp	pre clamp
Y_{ext}	pre clamp	main clamp

SIGNAL SWITCHES S2A AND S2B

Two switches are included to bypass the comb filter signal processing. The input video signal C_{ext} for the switch S2B is internally biased.

For the Y_O output two signals can be selected via S2A.

Table 5 Y_O output signal

SVHS	Y_O OUTPUT SIGNAL	MODE
LOW	YCOMB (combed luminance)	COMB
HIGH	input Y_{ext}	SVHS

For the C_O output two signals can be selected via S2B.

Table 6 C_O output signal

SVHS	C_O OUTPUT SIGNAL	MODE
LOW	CCOMB (combed chrominance)	COMB
HIGH	input C_{ext}	SVHS

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–	6.5	V
V	input voltage protection threshold (except pin 1)		–0.3	V_{CC} + 0.3	V
I_{CCA}	analog supply current		–	17	mA
I_{CCO}	analog supply current output buffer		–	45	mA
I_{DDD}	digital supply current		–	6	mA
I_{CCPLL}	analog supply current PLL		–	2.5	mA
I_O	output current at pins 11 and 9		–	±15	mA
P_{tot}	total power dissipation		–	400	mW
T_{stg}	storage temperature		–25	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
V_{es}	electrostatic handling (all pins)	note 1	–	±300	V
		note 2	–	±2000	V

Notes

1. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor (0 Ω means: 2.5 μH + 25 Ω); ESD classification B in accordance with *"UZW-B0/FQ-0601"*.
2. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor; ESD classification B in accordance with *"UZW-B0/FQ-0601"*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT146-1	65	K/W
	SOT163-1	80	K/W

CHARACTERISTICS

$V_{DDD} = V_{CCA} = V_{CCO} = V_{CCPLL}$ = 5 V; T_{amb} = 25 °C; input signal Y_{ext}/CVBS = 1 V (p-p) (0 dB); input signal C_{ext} = 0.7 V (p-p) (0 dB); input signal FSC = 200 mV (p-p), sine wave, DC level = 2 V; test signal: EBU colour bar 100/0/75/0 *"CCIR471-1"*; source impedance for Y_{ext}, CVBS, C_{ext} = 75 Ω decoupled with 100 nF; source impedance for FSC = 75 Ω; load impedance for Y_O, C_O = 1 kΩ and 20 pF in parallel; see Fig.9; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
V_{CCA}	analog supply voltage (pin 4)	note 1	4.75	5	5.5	V
V_{CCO}	analog supply voltage output buffer (pin 6)	note 1	4.75	5	5.5	V
V_{DDD}	digital supply voltage (pin 15)	note 1	4.75	5	5.5	V
V_{CCPLL}	analog supply voltage PLL (pin 18)	note 1	4.75	5	5.5	V
FSC (pin 1)						
$V_{1(p-p)}$	input AC voltage (peak-to-peak value)	note 2	100	200	400	mV
V_1	input DC level		0	–	5.3	V
C_1	input capacitance		–	–	10	pF
I_{leak}	input leakage current		–	–	10	μA
Z_1	source impedance		–	–	800	Ω
SVHS (pin 2)						
V_{IH}	HIGH level input voltage		2.4	–	V_{CC}	V
V_{IL}	LOW level input voltage		0	0.85	1.5	V
I_{leak}	input leakage current		–	–	10	μA
C_2	input capacitance		–	–	10	pF
V_{CCA} (pin 4)						
I_{CCA}	analog supply current		–	10	17	mA
V_{CCO} (pin 6)						
I_{CCO}	supply current		–	35	45	mA
C_{ext} (pin 7)						
V_7	input voltage (AC coupled)		–	0	3	dB
R_7	input resistance	1.25 V	100	250	400	kΩ
C_7	input capacitance		–	–	10	pF
Z_7	source impedance		–	–	1	kΩ
C_O (pin 9)						
V_9/V_7	SVHS-mode: C_O/C_{ext}	f_{sc} ±0.3f_{sc}; note 3	–1	0	+1	dB
COMB-mode: transfer function C-path see Fig.6						
V_9	DC offset voltage related to input		–400	0	+400	mV
$\|\Delta V_9\|$	DC jump when forcing into SVHS-mode		–	200	500	mV
R_9	output resistance		–	10	100	Ω
R_L	load resistance (to ground)		1.0	–	–	kΩ
C_L	load capacitance (to ground)		–	–	25	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_9	suppression (comb depth) related to the nearest ‘nominal’ chrominance frequency	see Fig.3 and note 4				
		$227 \times f_H$	26	30	–	dB
		$(227 - 35) \times f_H$	18	22	–	dB
		$(227 + 28) \times f_H$	18	22	–	dB
S/N	signal-to-noise ratio (0.7 V/V_{eff} noise)	unweighted; f_{sc} ±0.3f_{sc}; note 3	52	–	–	dB
FPN(p-p)	fixed pattern noise peak-to-peak referenced to 0.7 V (p-p) video	$3f_{sc}$	30	–	–	dB
		$\frac{3}{2}f_{sc}$	36	–	–	dB
		f_{sc}	50	–	–	dB
		$\frac{3}{4}f_{sc}$	30	–	–	dB
α_{cr}	crosstalk between different inputs	0 to 5 MHz	–	–60	–40	dB
V_9	FSC residue in SVHS mode related to 700 mV (p-p)		–	–	–60	dB
G_d	differential gain		0.95	–	–	
REFDL (pin 10)						
V_{10}	DC voltage		1.1	1.25	1.4	V
Y_O (pin 11)						
V_{11}/V_{14}	SVHS-mode: Y_O/Y_{ext}	0 to 5 MHz	–1	0	+1	dB
COMB-mode: transfer function Y-path see Fig.7						
V_{11}	DC offset voltage related to input		–400	0	+400	mV
$\lvert\Delta V_{11}\rvert$	DC jump when forcing into SVHS mode		–	200	500	mV
R_{11}	output resistance		–	10	100	Ω
R_L	load resistance (to ground)		1.0	–	–	kΩ
C_L	load capacitance (to ground)		–	–	25	pF
V_{11}	suppression (comb depth) related to the nearest ‘nominal’ luminance frequency	see Fig.4 and note 4				
		$227.5 \times f_H$	26	30	–	dB
		$(227.5 - 35) \times f_H$	19	21	–	dB
		$(227.5 + 28) \times f_H$	10	12	–	dB
S/N	signal-to-noise ratio (0.7 V/V_{eff} noise)	unweighted; 200 kHz to 5 MHz	52	–	–	dB
FPN(p-p)	fixed pattern noise peak-to-peak referenced to 0.7 V (p-p) video	$3f_{sc}$	30	–	–	dB
		$\frac{3}{2}f_{sc}$	30	–	–	dB
		f_{sc}	30	–	–	dB
		$\frac{3}{4}f_{sc}$	40	–	–	dB
α_{cr}	crosstalk between different inputs	0 to 5 MHz	–	–60	–40	dB
V_{11}	FSC residue in SVHS mode related to 700 mV (p-p)		–	–	–60	dB
G_d	differential gain		0.95	–	–	
CSY (pin 12)						
V_{12}	DC voltage		0	2.0	V_{CC}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CVBS (pin 13)						
V_{13}	input voltage (AC coupled)	12 dB sync compression possible; see Fig.5	–3	0	+3	dB
I_{13}	input current	during sync pulse; main clamp active	–30	–16	–	µA
		during active video; main clamp active	–	2.2	4.5	µA
V_{13}	DC voltage during black level		1.1	1.25	1.4	V
Z_{13}	source impedance		–	–	1	kΩ
Y_{ext} (pin 14)						
V_{14}	input voltage (AC coupled)	12 dB sync compression possible; see Fig.5	–3	0	+3	dB
I_{14}	input current	during sync pulse; pre clamp active	–30	–20	–	µA
		during active video; pre clamp active	–	2.2	4.5	µA
V_{14}	DC voltage during black level		1.1	1.25	1.4	V
Z_{14}	source impedance		–	–	1	kΩ
V_{DDD} (pin 15)						
I_{DDD}	supply current		–	3	6	mA
V_{CCPLL} (pin 18)						
I_{18}	supply current		–	1.5	2.5	mA
REFBP (pin 20)						
V_{20}	DC voltage		1.1	1.25	1.4	V

Notes

1. $\Delta V = |V_{CCA} - V_{DDD}| \leq 300$ mV $\Delta V = |V_{CCA} - V_{CCPLL}| \leq 300$ mV

   $\Delta V = |V_{CCA} - V_{CCO}| \leq 300$ mV $\Delta V = |V_{CCO} - V_{CCPLL}| \leq 300$ mV

   $\Delta V = |V_{CCO} - V_{DDD}| \leq 300$ mV $\Delta V = |V_{DDD} - V_{CCPLL}| \leq 300$ mV

2. Input AC voltage and detection level are valid for sine wave signals and for square wave signals with a duty factor of 0.4 to 0.6.
3. Subcarrier frequency f_{sc} = 3.579545 MHz.
4. Line frequency f_H = 15.734264 kHz.

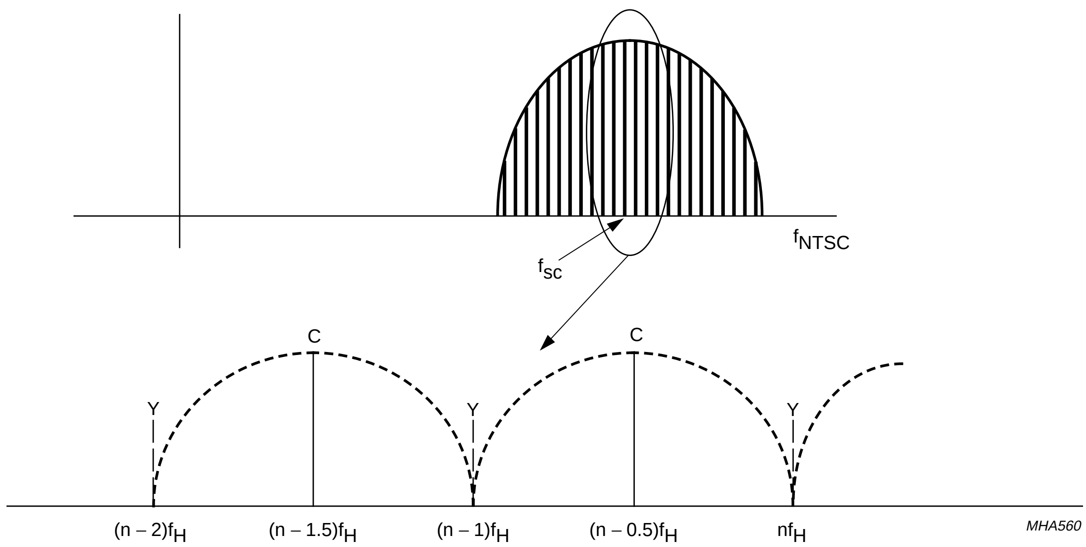


Fig.3 Principle frequency response of a comb filtered NTSC chrominance signal.

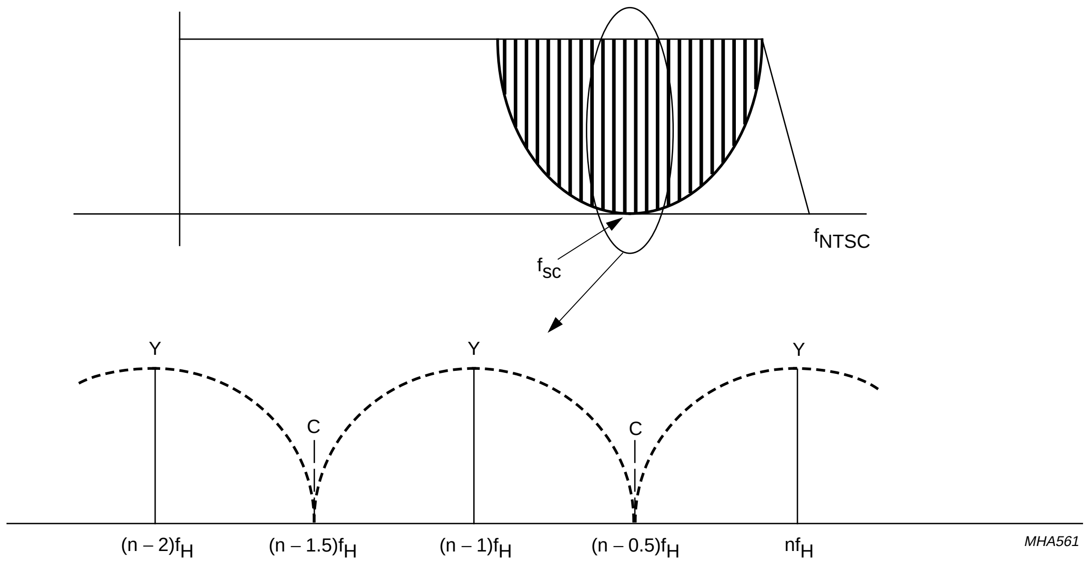


Fig.4 Principle frequency response of a comb filtered NTSC luminance signal.

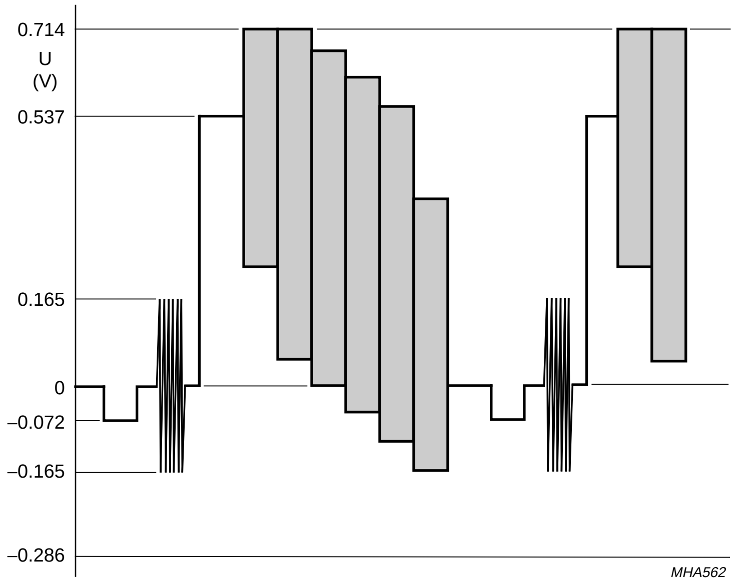


Fig.5 FCC/EIA colour bar 100% saturation, 75% amplitude with 12 dB sync attenuation.

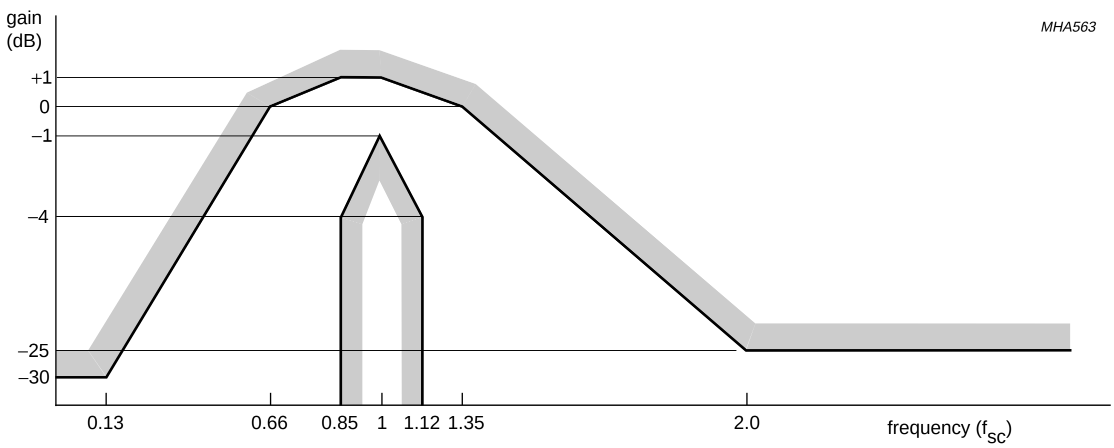


Fig.6 Chrominance path: tolerance band with anti-alias filter.

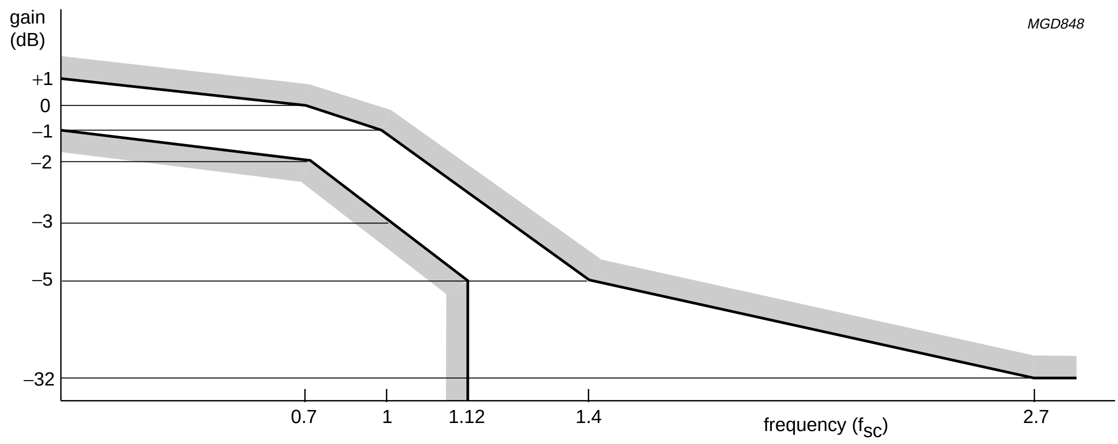


Fig.7 Luminance path: tolerance band with anti-alias filter.

TEST AND APPLICATION INFORMATION

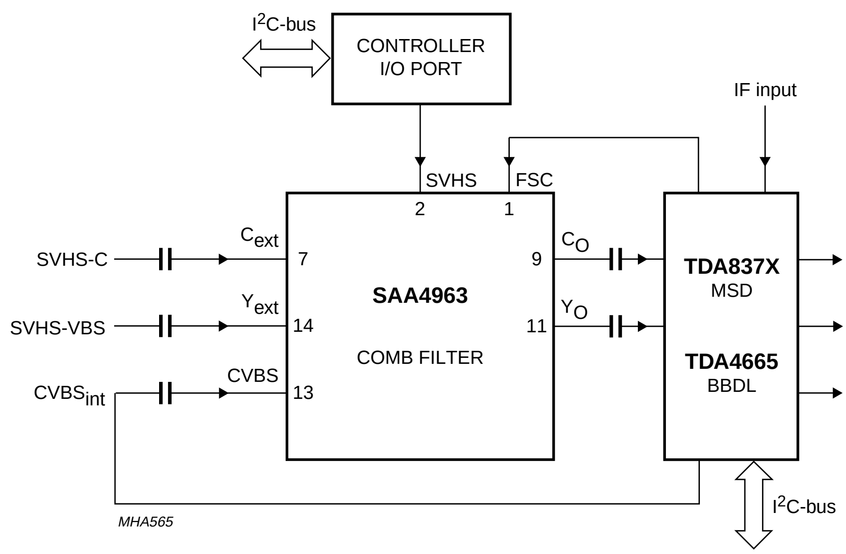


Fig.8 Application diagram: SAA4963 with TDA837X.

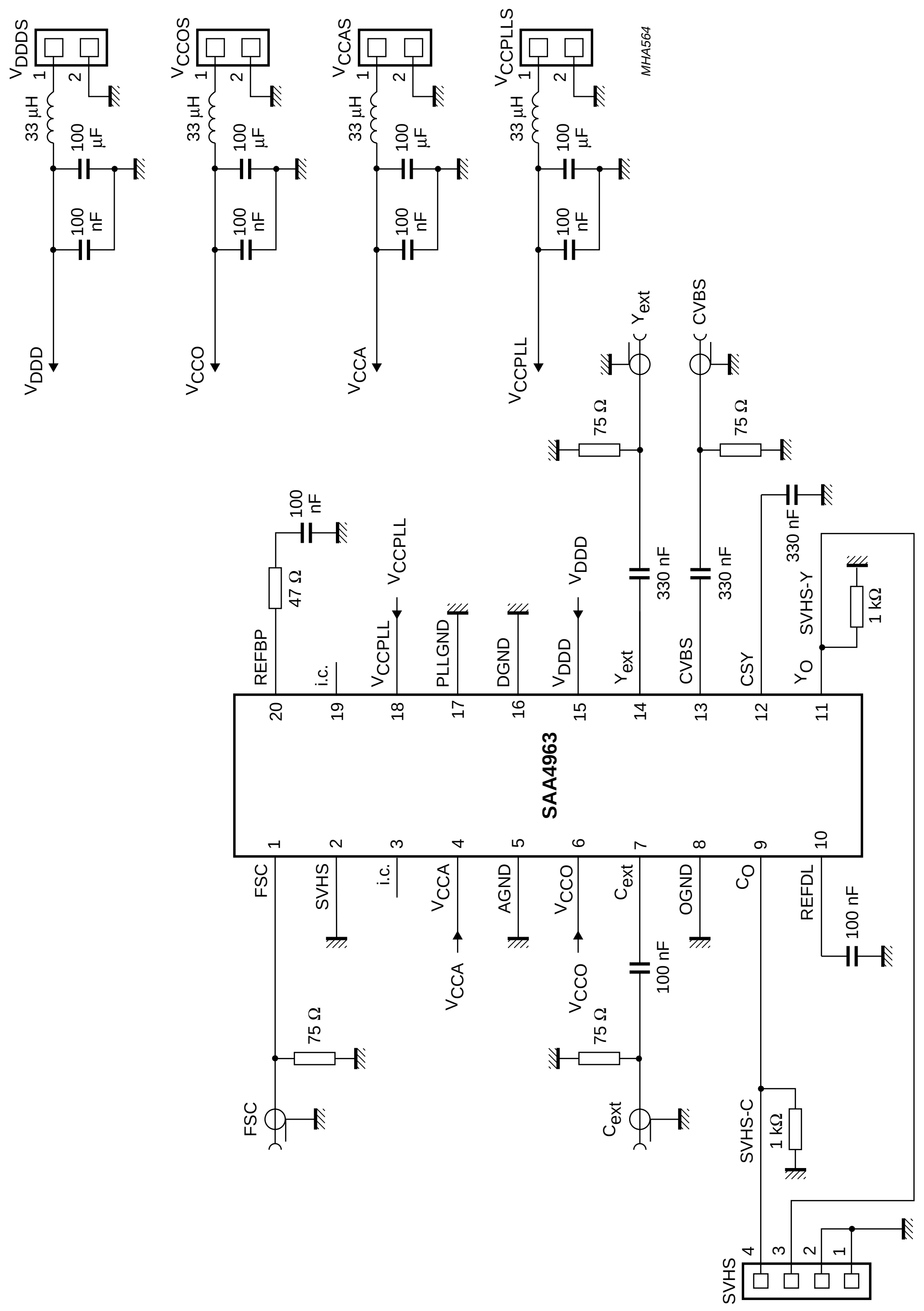
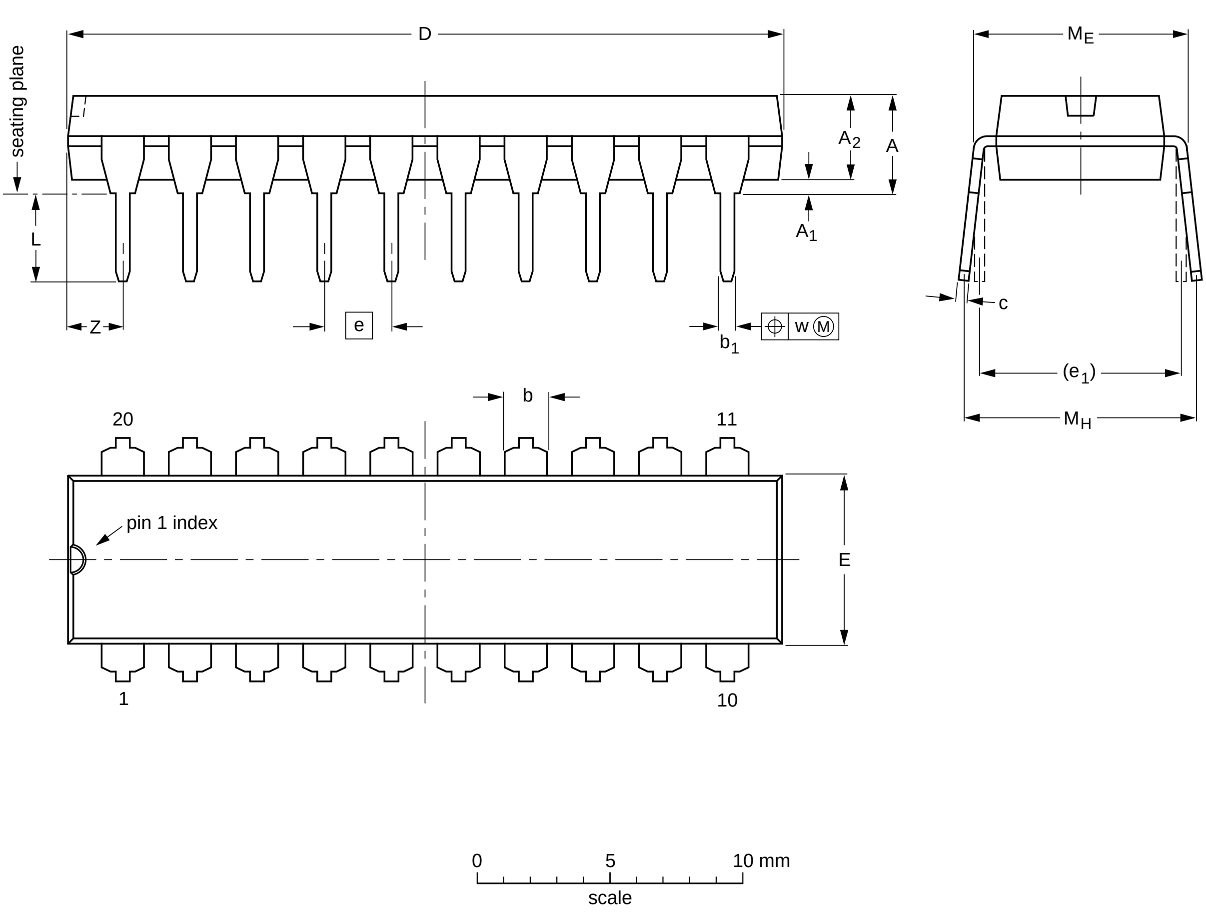


Fig.9 Test circuit.

PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil) SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

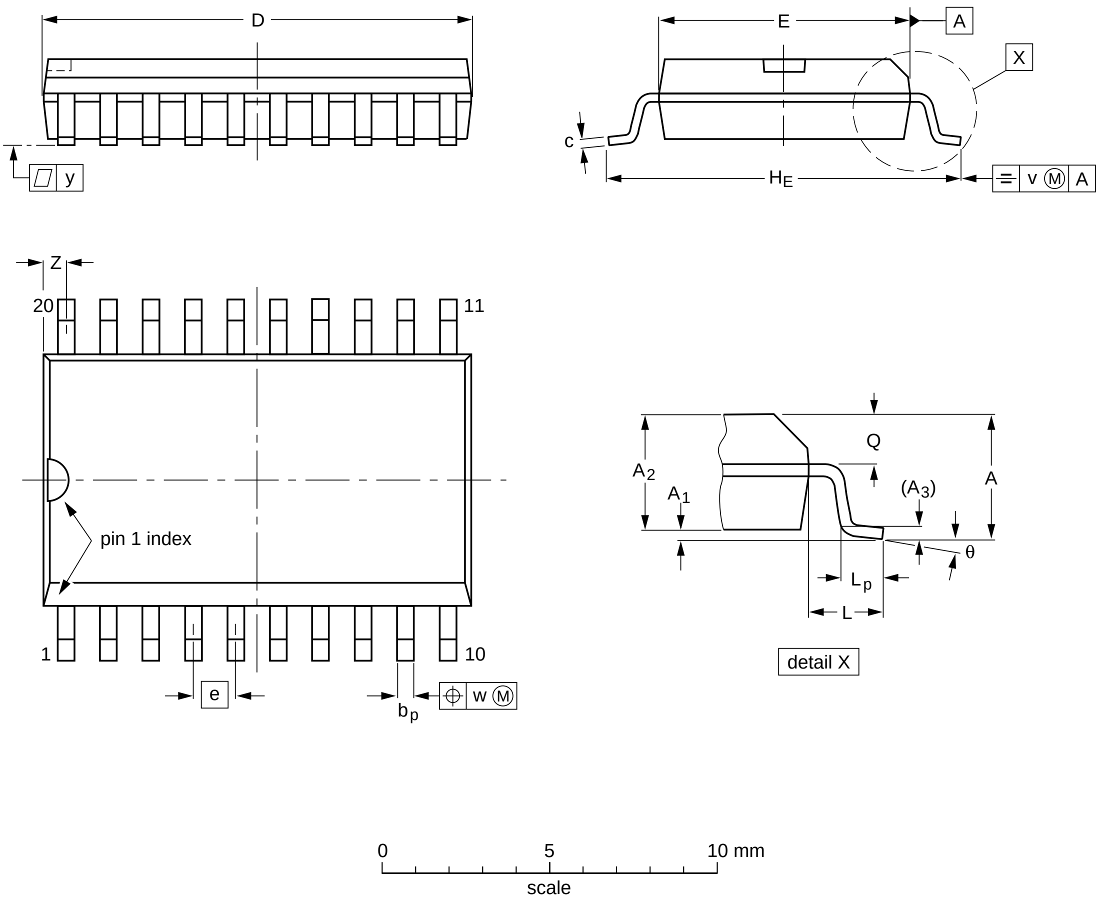
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~92-11-17~~ 95-01-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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