DATA SHEET

TDA8043
Satellite Demodulator and Decoder (SDD)

Product specification
Supersedes data of 1997 Nov 07
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Satellite Demodulator and Decoder (SDD) TDA8043

FEATURES

- One-chip Digital Video Broadcasting (DVB) compliant demodulator and concatenated Viterbi/Reed-Solomon decoder with de-interleaver and de-randomizer
- 3.3 V supply voltage (up to 5 V allowed)
- Internal clock divider
- On-chip crystal oscillator
- QPSK/BPSK demodulator:
  - Interpolator to handle variable symbol rates without an external anti-aliasing filter
  - On-chip Automatic Gain Control (AGC) of the analog input I and Q baseband signals or tuner AGC control
  - Two on-chip matched Analog-to-Digital Converters (ADCs; 7 bits)
  - Square-Root Raised-Cosine Nyquist filter with programmable roll-off factor
  - High maximum symbol frequency: 32 Msymbols/s
  - Can be used at low channel Es/No (Symbol energy-to-noise ratio)
  - Internal carrier recovery, clock recovery and AGC loops with programmable loop filters
  - Two carrier recovery loops enabling phase tracking of the incoming symbols
  - Different modulation schemes: Quadrature Phase Shift Keying (QPSK) and Binary-Phase Shift Keying (BPSK)
  - Signal-to-noise ratio (S/N) estimation
  - External indication of demodulator lock.
- Viterbi decoder:
  - Rate $\frac{1}{2}$ convolutional code based
  - Constraint length K = 7 with $G_1 = 171_{oct}$ and $G_2 = 133_{oct}$
  - Supported puncturing code rates: $\frac{1}{2}$, $\frac{2}{3}$, $\frac{3}{4}$, $\frac{4}{5}$, $\frac{5}{6}$, $\frac{6}{7}$, $\frac{7}{8}$ and $\frac{8}{9}$
  - 4 bits ‘soft decision’ inputs for both I and Q
  - Truncation length: 144
  - Automatic synchronization to correct puncturing rate and spectral inversion
  - Channel Bit Error Rate (BER) estimation from 10^{-2} to 10^{-8}
  - External indication of Viterbi synchronization lock
  - Differential decoding supported.
- Reed-Solomon (RS) decoder:
  - (204, 188 and T = 8) Reed Solomon code
  - Automatic (I^2C-bus configurable) synchronization of bytes, transport packets and frames
  - Internal convolutional de-interleaving (I = 12; using internal memory)
  - De-randomizer based on Pseudo Random Binary Sequence (PRBS)
  - External indication of RS decoder sync lock
  - External indication of uncorrectable errors (transport error indicator is set)
  - Indication of the number of lost blocks
  - Indication of the number of corrected blocks/bytes.
- I^2C-bus interface:
  - I^2C-bus interface initializes and monitors the demodulator and Forward Error Correction (FEC) decoder with standby mode; when no I^2C-bus is used, default mode is defined
  - 4-bit I/O expander for flexible access to and from the I^2C-bus
  - I^2C-bus configurable interrupt pin
  - Standby mode for reduced power consumption.
- Package: QFP100
- Boundary scan test.

APPLICATIONS

- Demodulation and FEC for digital satellite TV.

GENERAL DESCRIPTION

This document specifies a DVB compliant demodulator and forward error correction decoder IC for reception of QPSK and BPSK modulated signals for satellite applications.

The TDA8043 can handle variable symbol rates without adapting the analog filters within the tuner. Typical applications for this device are:

- **Single Carrier Per Channel (SCPC)**: two or more QPSK or BPSK modulated signals in a single satellite channel (transponder)
- **Multi-Carrier Per Channel (MCPC)**: one QPSK or BPSK modulated signal in a single satellite channel (transponder)
- **Simul-cast**: QPSK or BPSK modulated signal together with a Frequency Modulated (FM) signal in a single satellite channel.

The SDD requires the analog in-phase (I) and quadrature (Q) components as an input and provides 8-bit wide MPEG2 transport packet data at the output. The outputs of the SDD can be directly connected to a descrambler (SAA7206) or a demultiplexer (SAA7205).

For evaluation purposes, the output can also be used to monitor internal data, for example I/Q after demodulation.

The SDD requires a single clock frequency which is independent of the received symbol rate, providing the clock frequency is slightly higher than twice the highest symbol frequency.

All loops to recover the data from the received symbols are internal. No external loop components are required. Loop parameters for the clock, carrier recovery and AGC can be controlled via the I^2C-bus.

The Forward Error Correction (FEC) unit has a built-in state machine to achieve lock without knowing the system parameters (depuncturing rate, spectral inversion, etc.). Once lock is achieved, all necessary parameters can be read via the I^2C-bus. By programming these parameters in advance lock can be achieved more quickly.

The SDD can be controlled and monitored via the I^2C-bus. An I^2C-bus default mode is specified which makes it possible to use the device by software control. A 4-bit bidirectional I/O expander and an interrupt line are available. By sending an interrupt signal, the SDD can inform the microcontroller of its internal status (lock).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8043H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT317-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current	V_{DDD} = 3.3 V; note 1	–	390	–	mA
f_{clk}	clock frequency		–	–	65	MHz
r_s	symbol rate	note 2	0.5	–	32	Msymbols/s
α	nyquist roll-off (selectable)		–	35 or 50	–	%
IL	implementation loss	note 3	–	0.3	–	dB
S/N	signal-to-noise ratio for locking the SDD	QPSK mode; note 1	2	–	–	dB
P_{tot}	total power dissipation	T_{amb} = 70°C; note 1	–	1285	1650	mW
T_{stg}	IC storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		0	–	70	°C
T_j	operating junction temperature	T_{amb} = 70 °C	–	–	125	°C

Notes

1. These values are specified for a symbol rate of 27.5 Msymbols/s, a puncturing rate of $^3/_4$ and a clock frequency of 65 MHz.
2. A range from 3 to 32 Msymbols/s can be achieved with one SAW filter. By using an internal clock divider and reducing the external SAW filter bandwidth, symbol rates down to 0.5 Msymbols/s can be achieved by using a 65 MHz crystal clock.
3. This data was measured in a laboratory environment at a symbol rate of 27.5 Msymbols/s, a clock frequency of 65 MHz, a signal-to-noise ratio of 4.5 dB and including a tuner.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
I2	1	I	digital I-input bit 2 (ADC bypass); note 1
I3	2	I	digital I-input bit 3 (ADC bypass); note 1
V_{SSD1}	3	–	digital ground 1
n.c.	4	–	not connected
n.c.	5	–	not connected
I4	6	I	digital I-input bit 4 (ADC bypass); note 1
I5	7	I	digital I-input bit 5 (ADC bypass); note 1
I6	8	I	digital I-input bit 6 (ADC bypass: MSB); note 1
Q0	9	I	digital Q-input bit 0 (ADC bypass: LSB); note 1
V_{DDD1}	10	–	digital supply voltage 1
Q1	11	I	digital Q-input bit 1 (ADC bypass); note 1
Q2	12	I	digital Q-input bit 2 (ADC bypass); note 1
Q3	13	I	digital Q-input bit 3 (ADC bypass); note 1
Q4	14	I	digital Q-input bit 4 (ADC bypass); note 1
V_{SSD2}	15	–	digital ground 2
Q5	16	I	digital Q-input bit 5 (ADC bypass); note 1
Q6	17	I	digital Q-input bit 6 (ADC bypass: MSB); note 1

SYMBOL	PIN	I/O	DESCRIPTION
V_{SSD3}	18	–	digital ground 3
V_{DDD2}	19	–	digital supply voltage 2
PRESET	20	I	set device into default mode
P3	21	I/O	quasi-bidirectional I/O port (bit 3)
P2	22	I/O	quasi-bidirectional I/O port (bit 2)
P1	23	I/O	quasi-bidirectional I/O port (bit 1)
P0	24	I/O	quasi-bidirectional I/O port (bit 0)
V_{DDD3}	25	–	digital supply voltage 3
n.c.	26	–	not connected
n.c.	27	–	not connected
PDOCLK	28	O	output clock for transport stream bytes
PDO0	29	O	parallel data output (bit 0)
PDO1	30	O	parallel data output (bit 1)
PDO2	31	O	parallel data output (bit 2)
V_{SSD4}	32	–	digital ground 4
PDO3	33	O	parallel data output (bit 3)
PDO4	34	O	parallel data output (bit 4)
PDO5	35	O	parallel data output (bit 5)
n.c.	36	–	not connected
n.c.	37	–	not connected
PDO6	38	O	parallel data output (bit 6)
n.c.	39	–	not connected
V_{DDD4}	40	–	digital supply voltage 4
V_{DDD5}	41	–	digital supply voltage 5
V_{SSD5}	42	–	digital ground 5
V_{DDD6}	43	–	digital supply voltage 6
V_{DDD7}	44	–	digital supply voltage 7
PDO7	45	O	parallel data output (bit 7)
n.c.	46	–	not connected
n.c.	47	–	not connected
PDOERR	48	O	transport error indicator
PDOVAL	49	O	data valid indicator
PDOSYNC	50	O	transport packet synchronization signal
V_{SSD6}	51	–	digital ground 6
SCL	52	I	serial clock of I^2C-bus; note 1
SDA	53	I/O	serial data of I^2C-bus; note 1
$\overline{INT}$	54	O	interrupt output (active LOW); note 1
A0	55	I	I^2C hardware address; note 1
RSLOCK	56	O	Reed-Solomon lock indicator
VLOCK	57	O	Viterbi lock indicator
DLOCK	58	O	demodulator lock indicator
V_{DDD8}	59	–	digital supply voltage 8
V_{DDD9}	60	–	digital supply voltage 9
TEST	61	I	test pin (normally connected to ground); note 1

SYMBOL	PIN	I/O	DESCRIPTION
TRST	62	I	BST optional asynchronous reset (normally connected to ground); note 1
TCK	63	I	BST dedicated test clock (normally connected to ground); note 1
n.c.	64	–	not connected
n.c.	65	–	not connected
V_{DDD10}	66	–	digital supply voltage 10
V_{SSD7}	67	–	digital ground 7
V_{SSD8}	68	–	digital ground 8
TMS	69	I	BST input control signal (normally connected to ground); note 1
TDO	70	O	BST serial test data out
TDI	71	I	BST serial test data in (normally connected to ground); note 1
V_{DDD11}	72	–	digital supply voltage 11
V_{SSD9}	73	–	digital ground 9
$V_{SSD(AD)}$	74	–	digital ground for ADC
$V_{DDD(AD)}$	75	–	digital supply for ADC
$V_{ref(B)}$	76	O	bottom reference voltage for ADC
V_{SSA1}	77	–	analog ground 1
QA	78	I	analog input Q
$V_{ref(Q)}$	79	O	AGC decoupling for Q path
IA	80	I	analog input I
V_{SSA2}	81	–	analog ground 2
$V_{ref(I)}$	82	O	AGC decoupling for I path
V_{DDA}	83	–	analog supply voltage
V_{DDXTAL}	84	–	supply voltage for crystal oscillator
XTALI	85	I	crystal oscillator input
XTALO	86	O	crystal oscillator output
V_{SSXTAL}	87	–	ground for crystal oscillator
V_{DDD12}	88	–	digital supply voltage 12
V_{DDD13}	89	–	digital supply voltage 13
V_{SSD10}	90	–	digital ground 10
n.c.	91	–	not connected
n.c.	92	–	not connected
n.c.	93	–	not connected
V_{AGC}	94	O	AGC output voltage; note 1
n.c.	95	–	not connected
V_{DDD14}	96	–	digital supply voltage 14
V_{DDD15}	97	–	digital supply voltage 15
OUTSD	98	O	general purpose sigma-delta output
I0	99	I	digital I-input bit 0 (ADC bypass: LSB); note 1
I1	100	I	digital I-input bit 1 (ADC bypass); note 1

Note

1. This pin is 5 V tolerant.

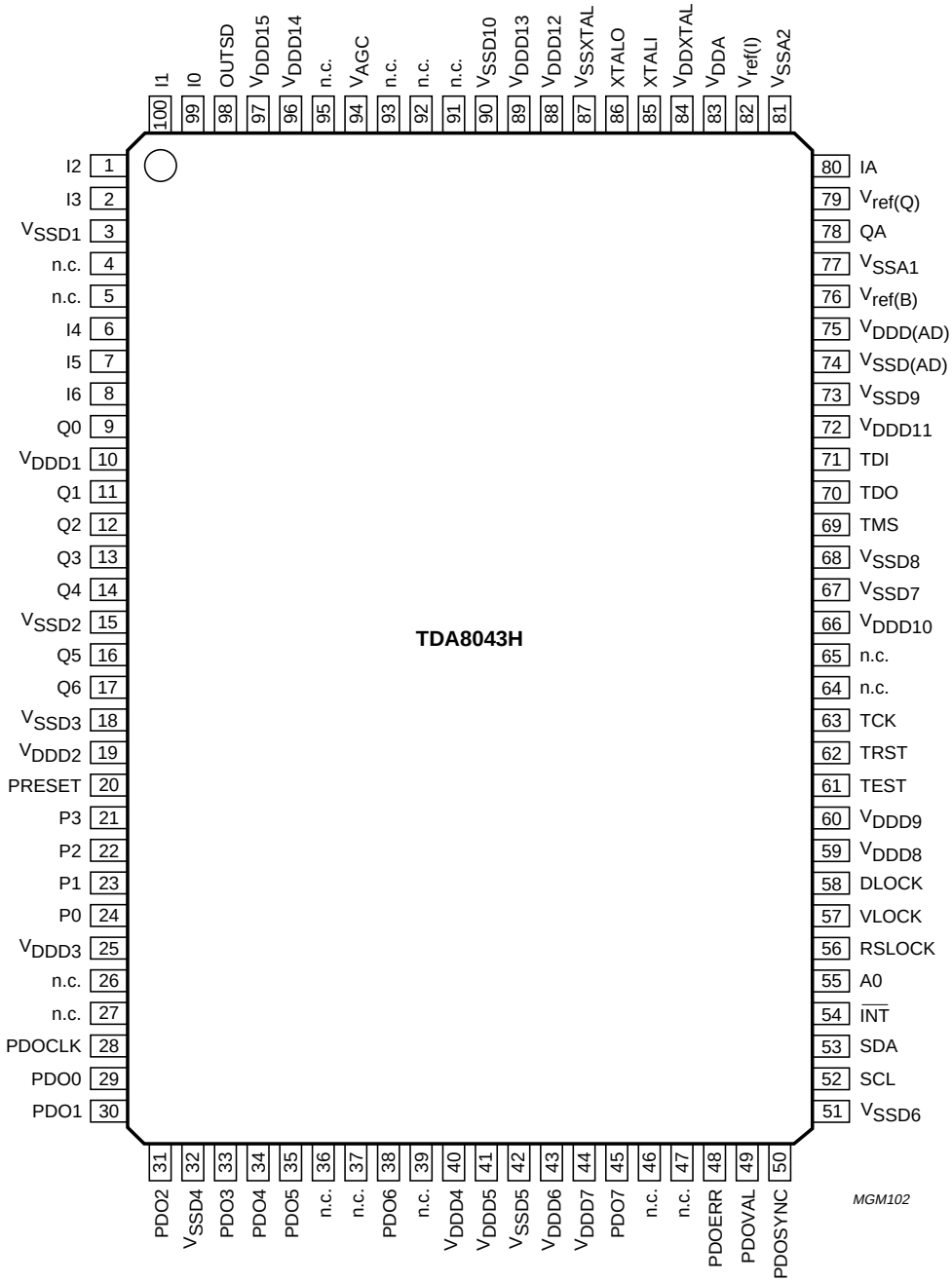


Fig.1 Pin configuration.

APPLICATION INFORMATION

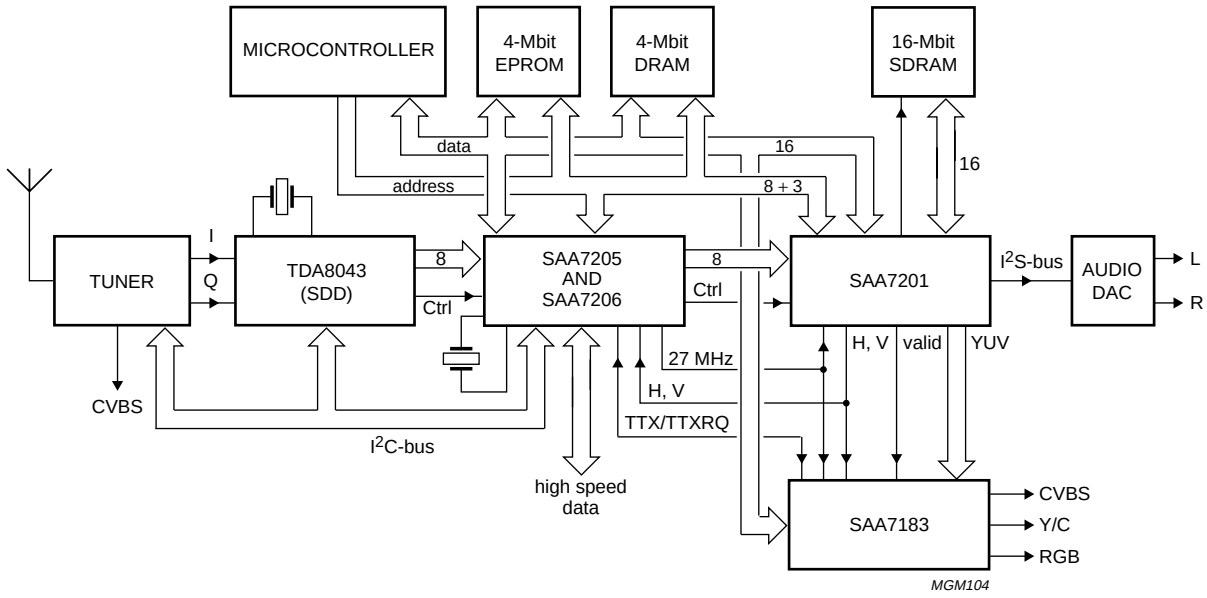
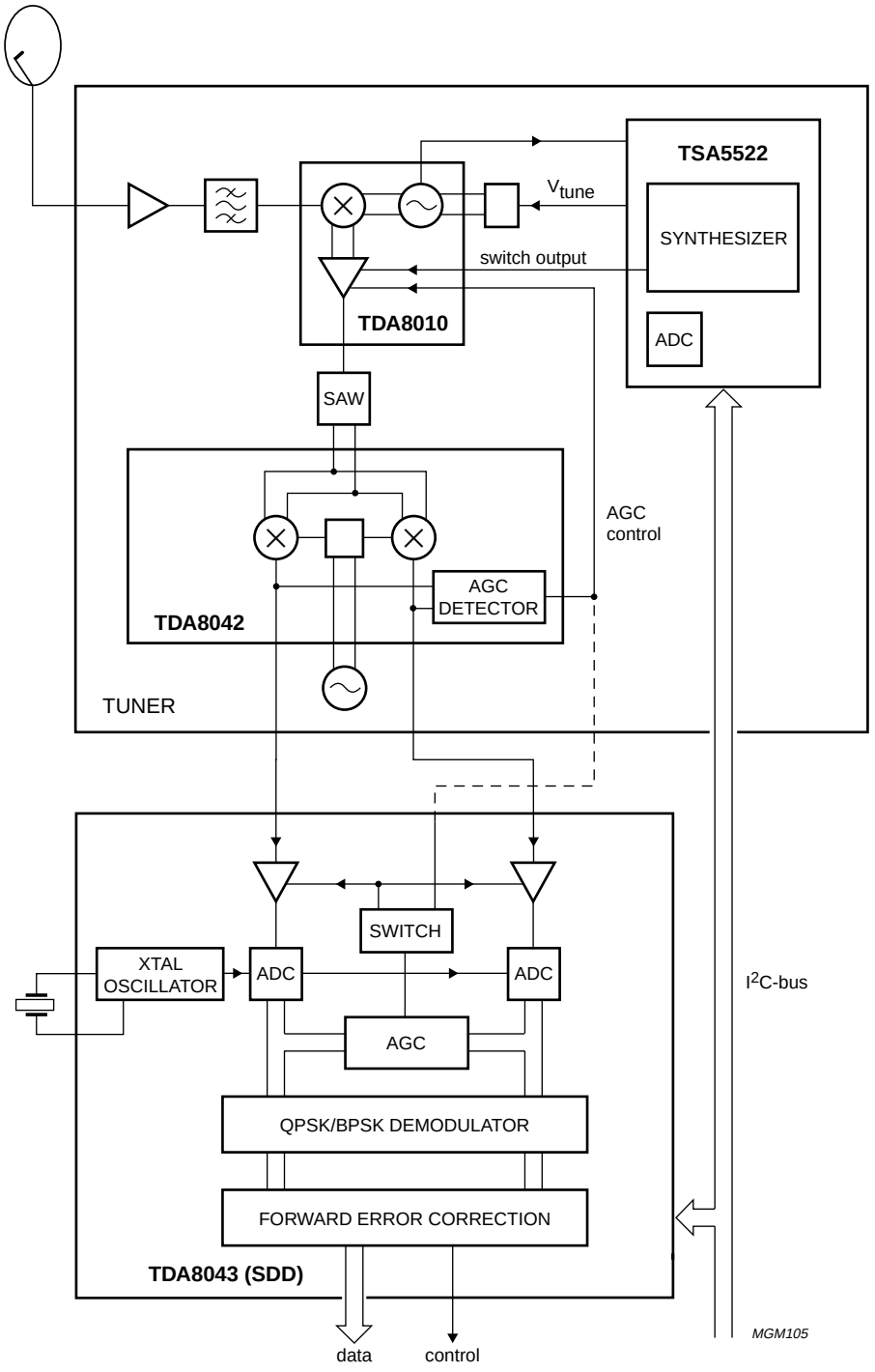
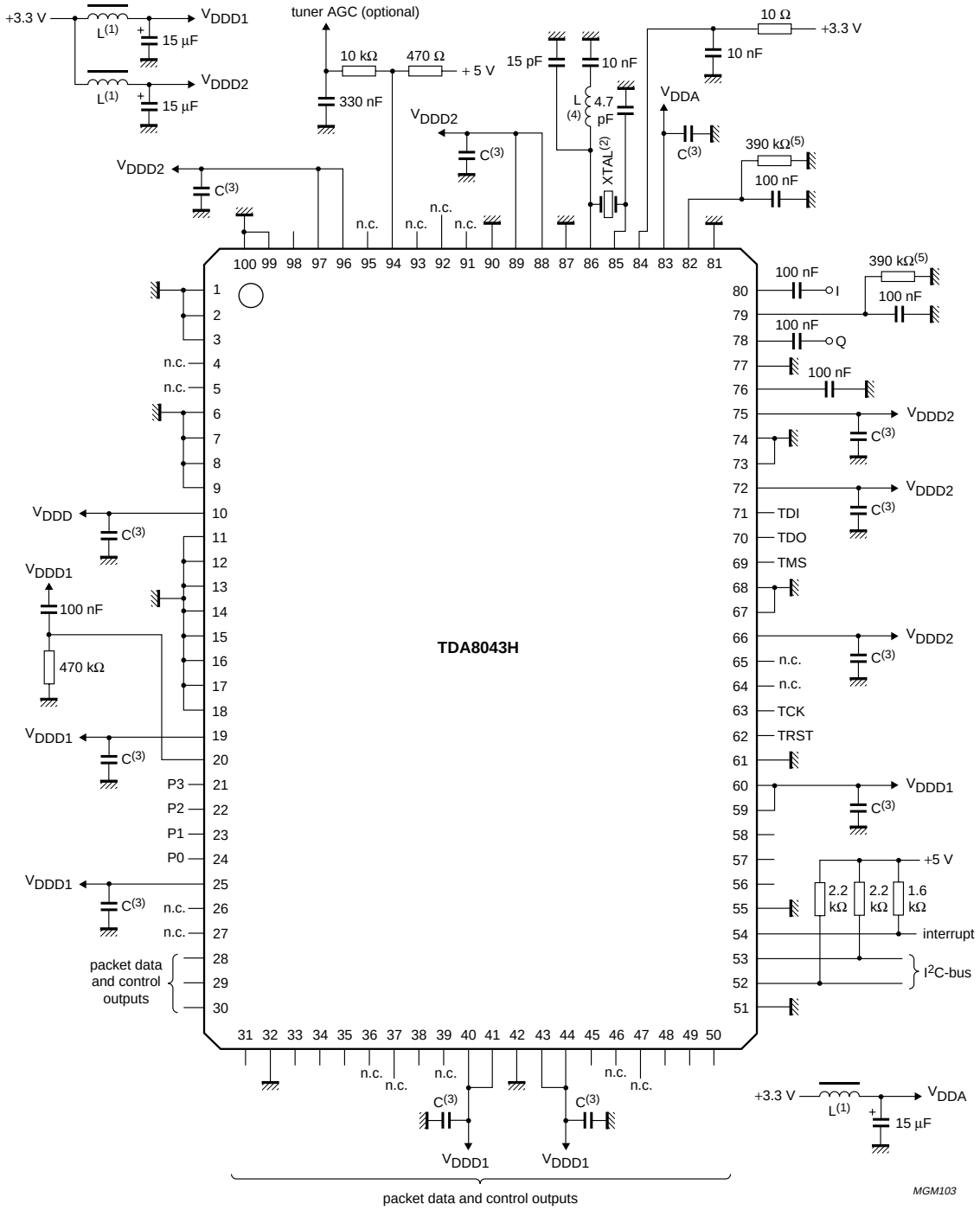


Fig.2 Satellite set-top box concept.



Note: Control for external AGC is also available using the internal AGC sigma-delta converter (indicated with the dashed line).

Fig.3 Application of satellite demodulator and decoder including tuner.



(1) B = SMD bead type CBD8.9/3/3 Grade 4S2.

(2) XTAL = 65 MHz, 3rd overtone.

(3) C = 6.8 nF, SMD.

(4) L = 560 nH, Taiyo Yuden LAL02.

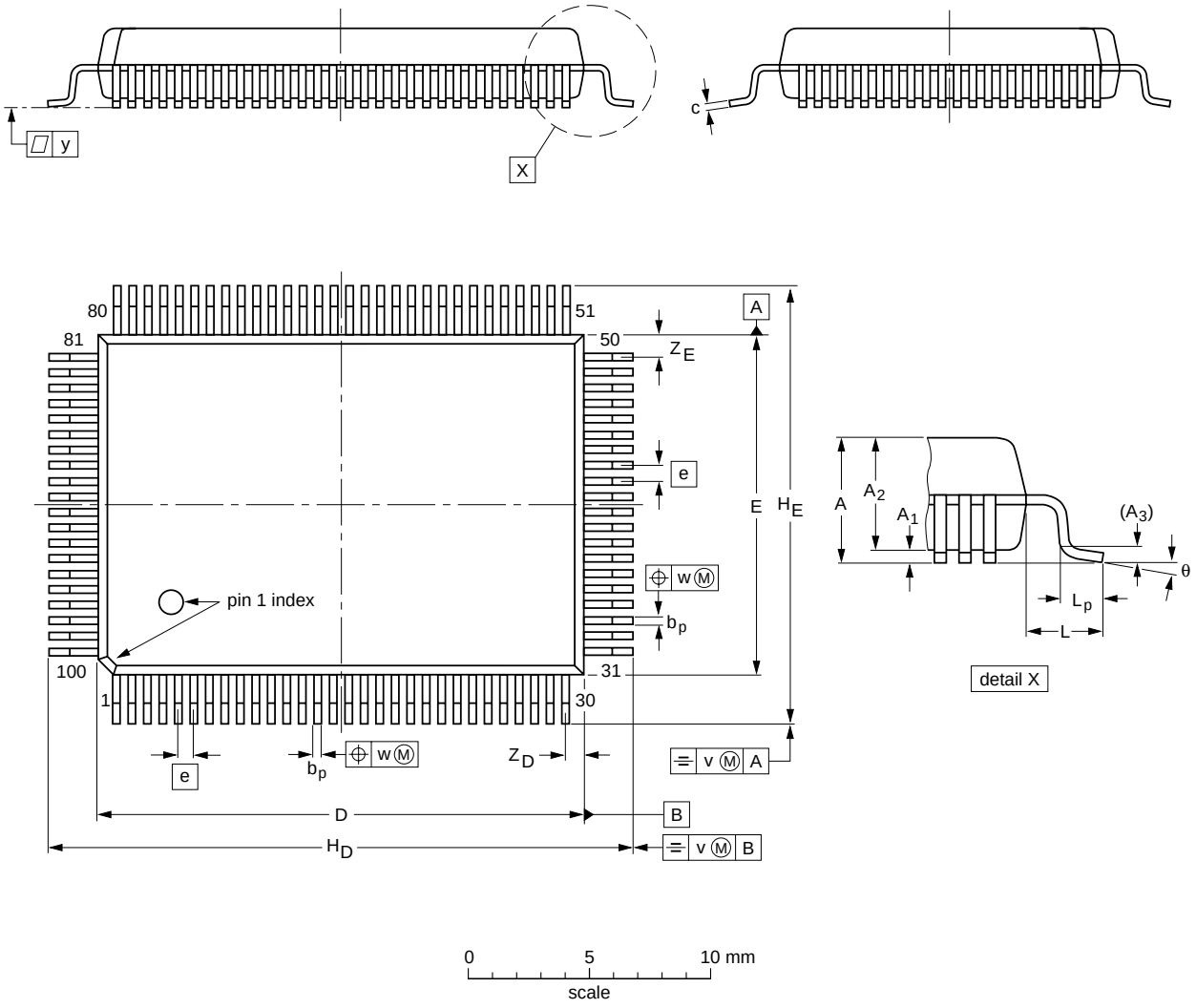
(5) Value specified for a 65 MHz clock. For other clock frequencies, refer to *"Application note AN96108"*.

If possible, connect 'n.c.' pins to ground to ease power dissipation.
TRST, TCK, TMS, and TDI pins can be connected to ground if they are not used.

Fig.4 Application diagram.

PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT317-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

NOTES

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