DATA SHEET

TDA8002
IC card interface

Product specification
Supersedes data of 1997 Mar 13
File under Integrated Circuits, IC02

1997 Nov 04

Philips
Semiconductors

PHILIPS

FEATURES

- Single supply voltage interface (3.3 or 5 V environment)
- Low-power sleep mode
- Three specific protected half-duplex bidirectional buffered I/O lines
- V_{CC} regulation (5 V ±5%, I_{CC} <65 mA at V_{DD} = 5 V, with controlled rise and fall times
- Thermal and short-circuit protections with current limitations
- Automatic ISO 7816 activation and deactivation sequences
- Enhanced ESD protections on card side (>6 kV)
- Clock generation for the card up to 12 MHz with synchronous frequency changes
- Clock generation up to 20 MHz (auxiliary clock)
- Synchronous and asynchronous cards (memory and smart cards)
- ISO 7816, GSM11.11 compatibility and EMV (Europay, Mastercard, Visa) compliant
- Step-up converter for V_{CC} generation
- Supply supervisor for spikes elimination and emergency deactivation.

APPLICATIONS

- IC card readers for:
  - GSM applications
  - banking
  - electronic payment
  - identification
  - Pay TV
  - road tolling.

GENERAL DESCRIPTION

The TDA8002 is a complete low-power, analog interface for asynchronous and synchronous cards. It can be placed between the card and the microcontroller. It performs all supply, protection and control functions. It is directly compatible with ISO 7816, GSM11.11 and EMV specifications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDA}	analog supply voltage		3.0	5	6.5	V
I_{DD}	supply current	sleep mode	–	–	150	µA
		idle mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	6	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 5 V	–	–	9	mA
		active mode; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz; V_{DD} = 3 V	–	–	12	mA
Card supply						
$V_{CC(O)}$	output voltage	DC load <65 mA	4.75	–	5.25	V
$I_{CC(O)}$	output current	V_{CC} short-circuited to GND	–	–	100	mA
General						
f_{CLK}	card clock frequency		0	–	12	MHz
T_{de}	deactivation cycle time		60	80	100	µs
P_{tot}	continuous total power dissipation					
	TDA8002AT; TDA8002BT	T_{amb} = –25 to +85 °C	–	–	0.56	W
	TDA8002G	T_{amb} = –25 to +85 °C	–	–	0.46	W
T_{amb}	operating ambient temperature		–25	–	+85	°C

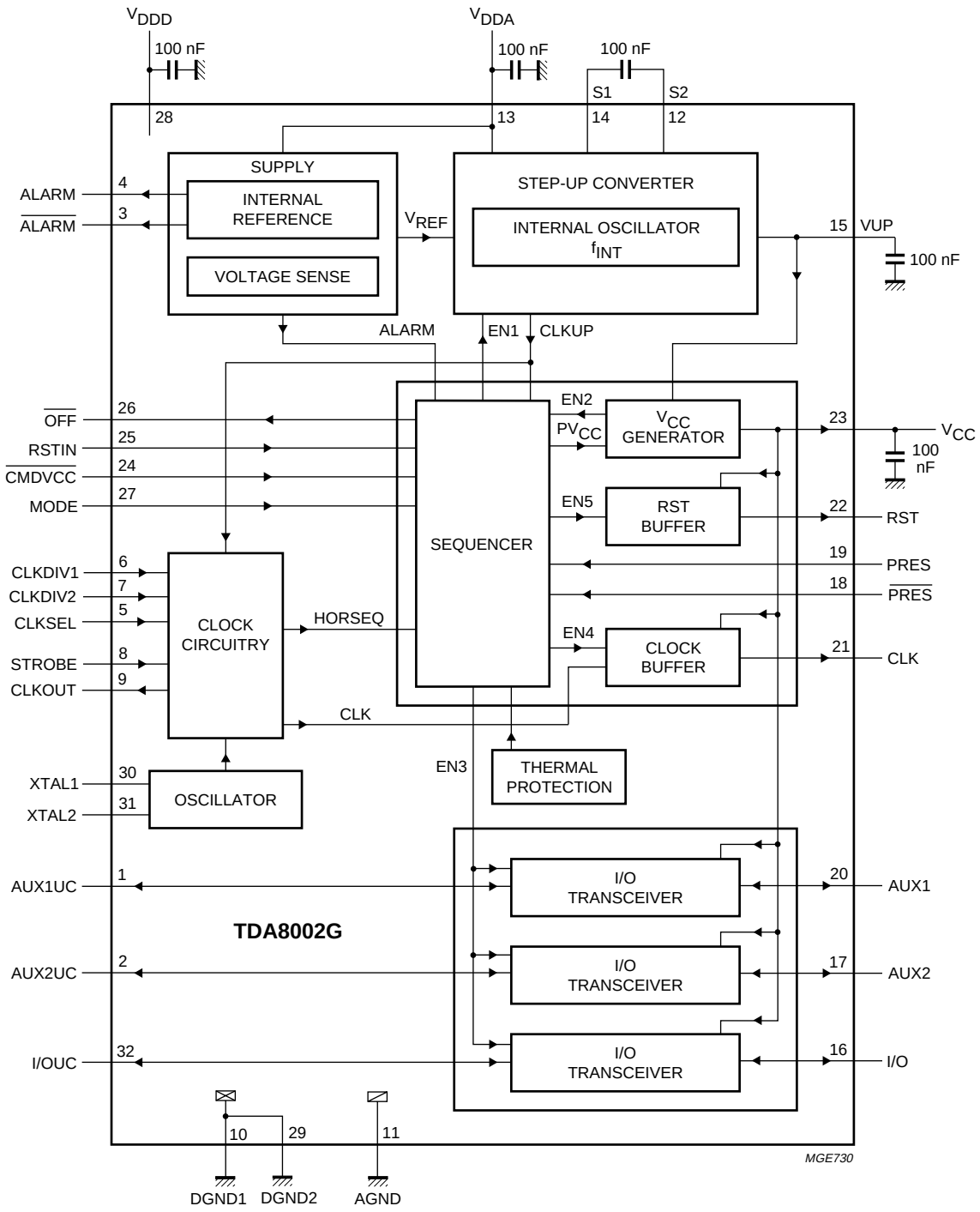
ORDERING INFORMATION

TYPE NUMBER[1]	PACKAGE			
	MARKING	NAME	DESCRIPTION	VERSION
TDA8002AT/3/C2[2]	TDA8002AT/3	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1
TDA8002AT/5/C2[3]	TDA8002AT/5			
TDA8002BT/3/C2[2]	TDA8002BT/3			
TDA8002BT/5/C2[3]	TDA8002BT/5			
TDA8002G/3/C2[2]	80023	LQFP32	plastic low profile quad flat package; 32 leads; body $5 \times 5 \times 1.4$ mm	SOT401-1
TDA8002G/5/C2[3]	80025			

Notes

1. The /3 or /5 suffix indicates the voltage supervisor option.
2. The /3 version can be used with a 3 or 5 V power supply environment (see Chapter “Functional description”).
3. The /5 version can be used with a 5 V power supply environment.

BLOCK DIAGRAM



All capacitors are mandatory.

Fig.1 Block diagram (TDA8002G).

PINNING

SYMBOL	PIN			I/O	DESCRIPTION
	TYPE A	TYPE B	TYPE G		
XTAL1	1	1	30	I/O	crystal connection or input for external clock
XTAL2	2	2	31	I/O	crystal connection
I/OUC	3	3	32	I/O	data I/O line to and from microcontroller
AUX1UC	4	4	1	I/O	auxiliary line to and from microcontroller for synchronous applications
AUX2UC	5	–	2	I/O	auxiliary line to and from microcontroller for synchronous applications
$\overline{\text{ALARM}}$	–	5	3	O	open drain NMOS reset output for microcontroller (active LOW)
ALARM	6	6	4	O	open drain PMOS reset output for microcontroller (active HIGH)
CLKSEL	7	7	5	I	control input signal for CLK (LOW = XTAL oscillator; HIGH = STROBE input)
CLKDIV1	8	8	6	I	control input with CLKDIV2 for choosing CLK frequency
CLKDIV2	9	9	7	I	control input with CLKDIV1 for choosing CLK frequency
STROBE	10	10	8	I	external clock input for synchronous applications
CLKOUT	11	11	9	O	clock output (see Table 1)
DGND1	12	12	10	supply	digital ground 1
AGND	13	13	11	supply	analog ground
S2	14	14	12	I/O	capacitance connection for voltage doubler
V_{DDA}	15	15	13	supply	analog supply voltage
S1	16	16	14	I/O	capacitance connection for voltage doubler
VUP	17	17	15	I/O	output of voltage doubler (connect to 100 nF)
I/O	18	18	16	I/O	data I/O line to and from card
AUX2	19	–	17	I/O	auxiliary I/O line to and from card
$\overline{\text{PRES}}$	20	19	18	I	active LOW card input presence contact
PRES	–	20	19	I	active HIGH card input presence contact
AUX1	21	21	20	I/O	auxiliary I/O line to and from card
CLK	22	22	21	O	clock to card output (C3) (see Table 1)
RST	23	23	22	O	card reset output (C2)
V_{CC}	24	24	23	O	supply for card (C1) (decouple with 100 nF)
$\overline{\text{CMDVCC}}$	25	25	24	I	active LOW start activation sequence input from microcontroller
RSTIN	26	26	25	I	card reset input from microcontroller
$\overline{\text{OFF}}$	27	27	26	O	open drain NMOS interrupt output to microcontroller (active LOW)
MODE	28	28	27	I	operating mode selection input (HIGH = normal; LOW = sleep)
V_{DDD}	–	–	28	supply	digital supply voltage
DGND2	–	–	29	supply	digital ground 2

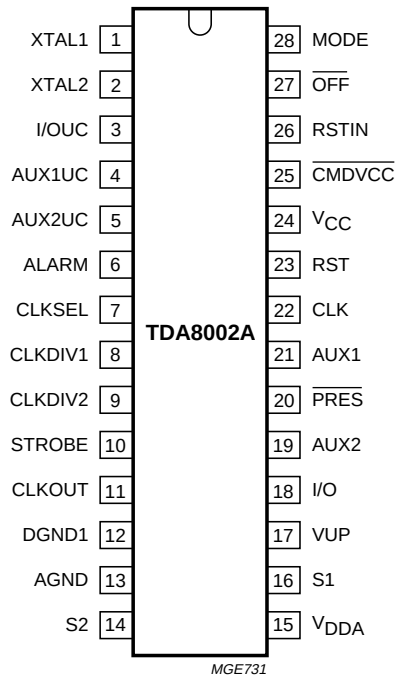


Fig.2 Pin configuration (TDA8002A).

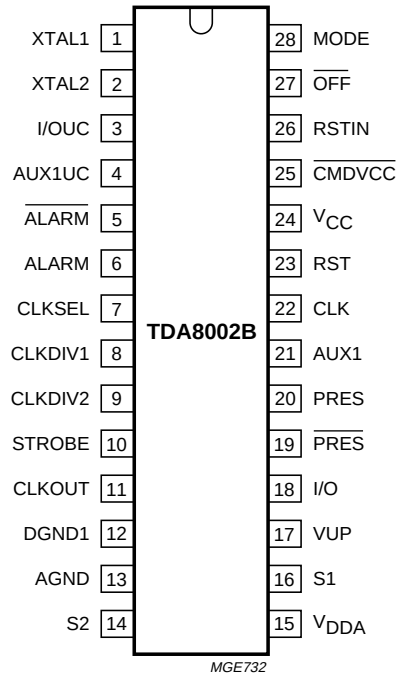


Fig.3 Pin configuration (TDA8002B).

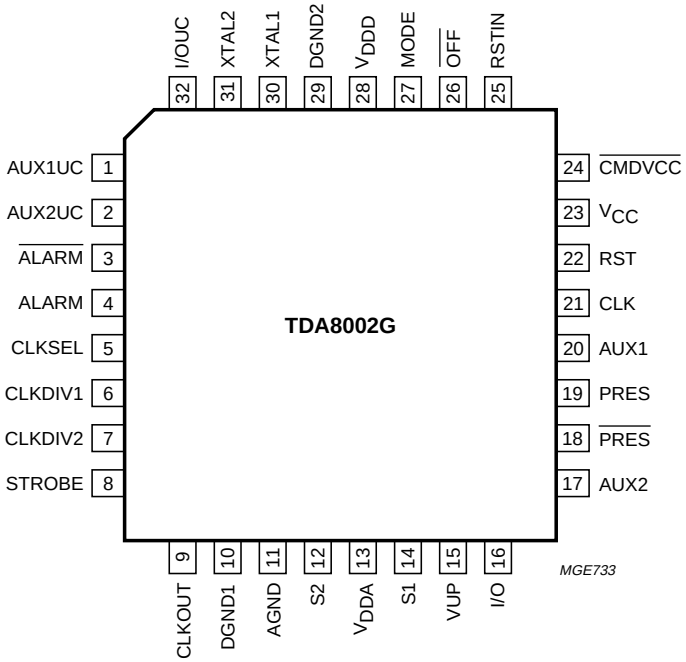


Fig.4 Pin configuration (TDA8002G).

FUNCTIONAL DESCRIPTION

Power supply

The supply pins for the chip are V_{DDA}, V_{DDD}, AGND, DGND1 and DGND2. V_{DDA} and V_{DDD} (i.e. V_{DD}) should be in the range of 3.0 to 6.5 V. All card contacts remain inactive during power-up or power-down.

On power-up, the logic is reset by an internal signal. The sequencer is not activated until V_{DD} reaches $V_{th2} + V_{hys2}$ (see Fig.5). When V_{DD} falls below V_{th2}, an automatic deactivation sequence of the contacts is performed.

Supply voltage supervisor (V_{DD})

This block surveys the V_{DD} supply. A defined reset pulse of 10 ms minimum (t_W) can be retriggered and is delivered on the ALARM outputs during power-up or power-down of V_{DD} (see Fig.5). This signal is also used for eliminating the spikes on card contacts during power-up or power-down.

When V_{DD} reaches $V_{th2} + V_{hys2}$, an internal delay is started. The ALARM outputs are active until this delay has expired. When V_{DD} falls below V_{th2}, ALARM is activated and a deactivation sequence of the contacts is performed.

For 3 V supply, the supervisor option must be chosen at 3 V. For 5 V supply, both options (3 or 5 V) may be chosen depending on the application.

Clock circuitry

The TDA8002 supports both synchronous and asynchronous cards (I^2C-bus memories requiring an acknowledge signal from the master are not supported). There are three methods to clock the circuitry:

- Apply a clock signal to pin STROBE
- Use of an internal RC oscillator
- Use of a quartz oscillator which should be connected between pins XTAL1 and XTAL2.

When CLKSEL is HIGH, the clock should be applied on the STROBE pin, and when CLKSEL is LOW, one of the internal oscillators is used.

When an internal clock is used, the clock output is available on pin CLKOUT. The RC oscillator is selected by making CLKDIV1 HIGH and CLKDIV2 LOW. The clock output to the card is available on pin CLK. The frequency of the card clock can be the input frequency divided by 2 or 4, STOP LOW or 1.25 MHz, depending on the states of CLKDIV1 or CLKDIV2 (see Table 1).

Do not change CLKSEL during activation. When in low-power (sleep) mode, the internal oscillator frequency which is available on pin CLKOUT is lowered to approximately 16 kHz for power-economy purposes.

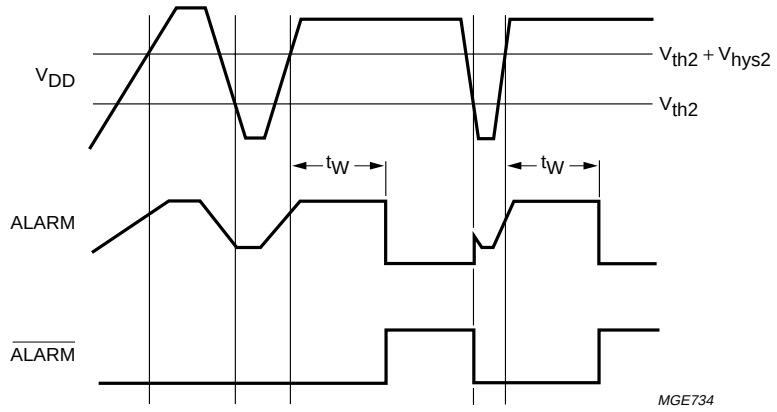


Fig.5 Alarm as a function of V_{DD} (pulse width 10 ms).

Table 1 Clock circuitry definition

MODE	CLKSEL	CLKDIV1	CLKDIV2	FREQUENCY OF CLK	FREQUENCY OF CLKOUT
HIGH	LOW	HIGH	LOW	$\frac{1}{2}f_{int}$	$\frac{1}{2}f_{int}$
HIGH	LOW	LOW	LOW	$\frac{1}{4}f_{xtal}$	f_{xtal}
HIGH	LOW	LOW	HIGH	$\frac{1}{2}f_{xtal}$	f_{xtal}
HIGH	LOW	HIGH	HIGH	STOP LOW	f_{xtal}
HIGH	HIGH	X(1)	X(1)	STROBE	f_{xtal}
LOW(2)	X(1)	X(1)	X(1)	STOP LOW	$\frac{1}{2}f_{int}$(3)

Notes

1. X = don't care.
2. In low-power mode.
3. f_{int} = 32 kHz in low-power mode.

I/O circuitry

The three I/O transceivers are identical. The state is HIGH for all I/O pins (i.e. I/O, I/OUC, AUX1, AUX1UC, AUX2 and AUX2UC). Pin I/O is referenced to V_{CC} and pin I/OUC to V_{DD}, thus ensuring proper operation in case $V_{CC} \neq V_{DD}$.

The first side on which a falling edge is detected becomes a master (input). An anti-latch circuitry first disables the detection of the falling edge on the other side, which becomes slave (output).

After a delay time t_d (about 50 ns), the logic 0 present on the master side is transferred on the slave side.

When the input is back to HIGH level, a current booster is turned on during the delay t_d on the output side and then both sides are back to their idle state, ready to detect the next logic 0 on any side.

In case of a conflict, both lines may remain LOW until the software enables the lines to be HIGH. The anti-latch circuitry ensures that the lines do not remain LOW if both sides return HIGH, regardless of the prior conditions. The maximum frequency on the lines is approximately 1 MHz.

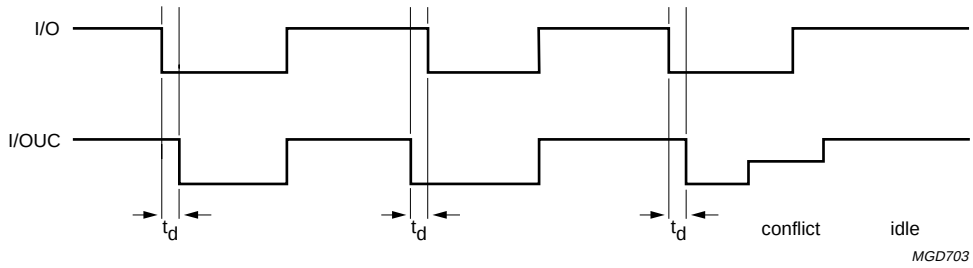


Fig.6 Master and slave signals.

Logic circuitry

After power-up, the circuit has six possible states of operation. Table 1 shows the sequence of these states.

IDLE MODE

After reset, the circuit enters the idle mode.
A minimum number of functions in the circuit are active while waiting for the microcontroller to start a session:

- All card contacts are inactive
- I/OUC, AUX1UC and AUX2UC are high-impedance
- Oscillator XTAL runs, delivering CLKOUT
- Voltage supervisor is active.

LOW-POWER (SLEEP) MODE

When pin MODE goes LOW, the circuit enters the low-power (sleep) mode. As long as pin MODE is LOW, no activation is possible.

If pin MODE goes LOW in the active mode, a normal deactivation sequence is performed before entering low-power mode. When pin MODE goes HIGH, the circuit enters normal operation after a delay of at least 6 ms (96 cycles of CLKOUT). During this time the CLKOUT remains at 16 kHz.

- All card contacts are inactive
- Oscillator XTAL does not run
- The V_{DD} supervisor, ALARM output, card presence detection and $\overline{OFF}$ output remain functional
- Internal oscillator is slowed to 32 kHz, CLKOUT providing 16 kHz.

ACTIVE MODE

When the activation sequence is completed, the TDA8002 will be in the active mode. Data is exchanged between the card and the microcontroller via the I/O lines.

State diagram

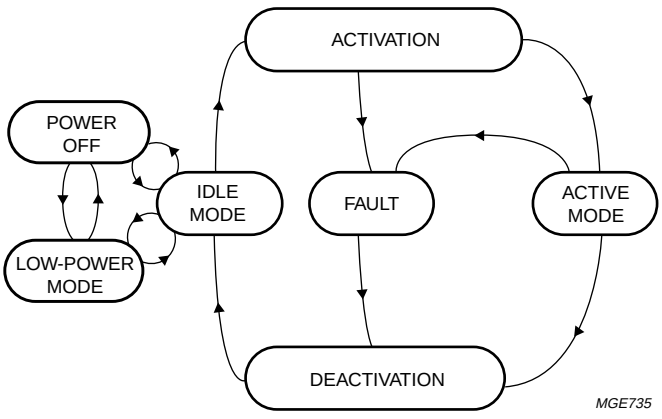


Fig.7 State diagram.

ACTIVATION SEQUENCE

From idle mode, the circuit enters the activation mode when the microcontroller sets the $\overline{\text{CMDVCC}}$ line LOW or sets the MODE line HIGH when the $\overline{\text{CMDVCC}}$ line is already LOW. The internal circuitry is then activated, the internal clock is activated and an activation sequence is executed. When RST is enabled, it becomes the inverse of RSTIN.

Figures 8 to 10 illustrate the activation sequence as described below:

1. Step-up converter is started ($t_1 \approx t_0$)
2. V_{CC} rises from 0 to 5 V ($t_2 = t_1 + 1\frac{1}{2}T$)
3. I/O, AUX1, AUX2 are enabled and CLK is enabled ($t_3 = t_1 + 4T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
4. CLK is set by setting RSTIN to HIGH (t_4)
5. RST is enabled ($t_5 = t_1 + 7T$); after t_5, RSTIN has no further action on CLK, but is only controlling RST.

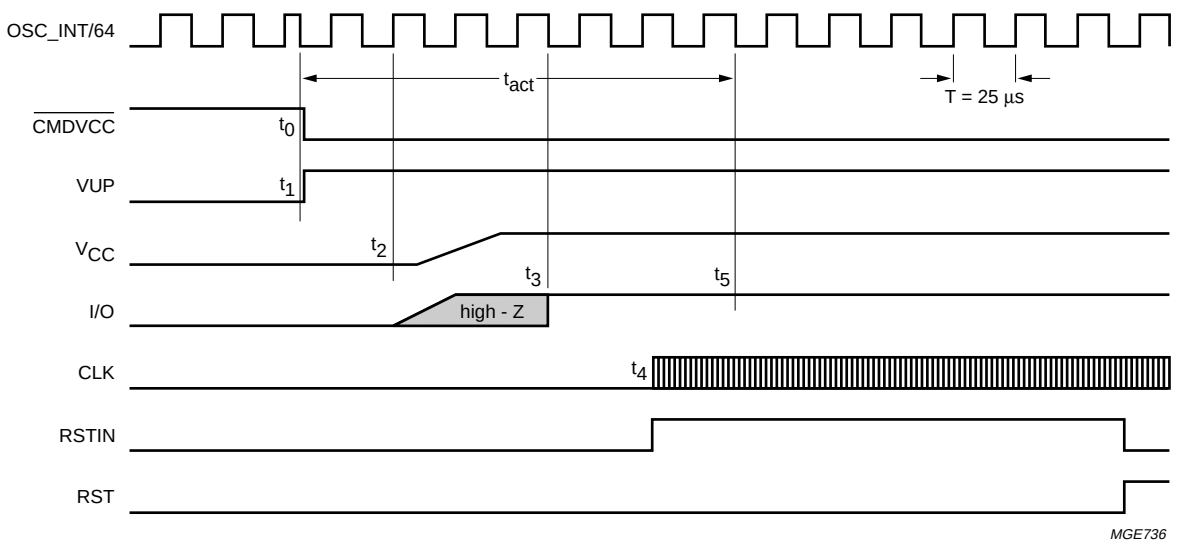


Fig.8 Activation sequence using RSTIN and $\overline{\text{CMDVCC}}$.

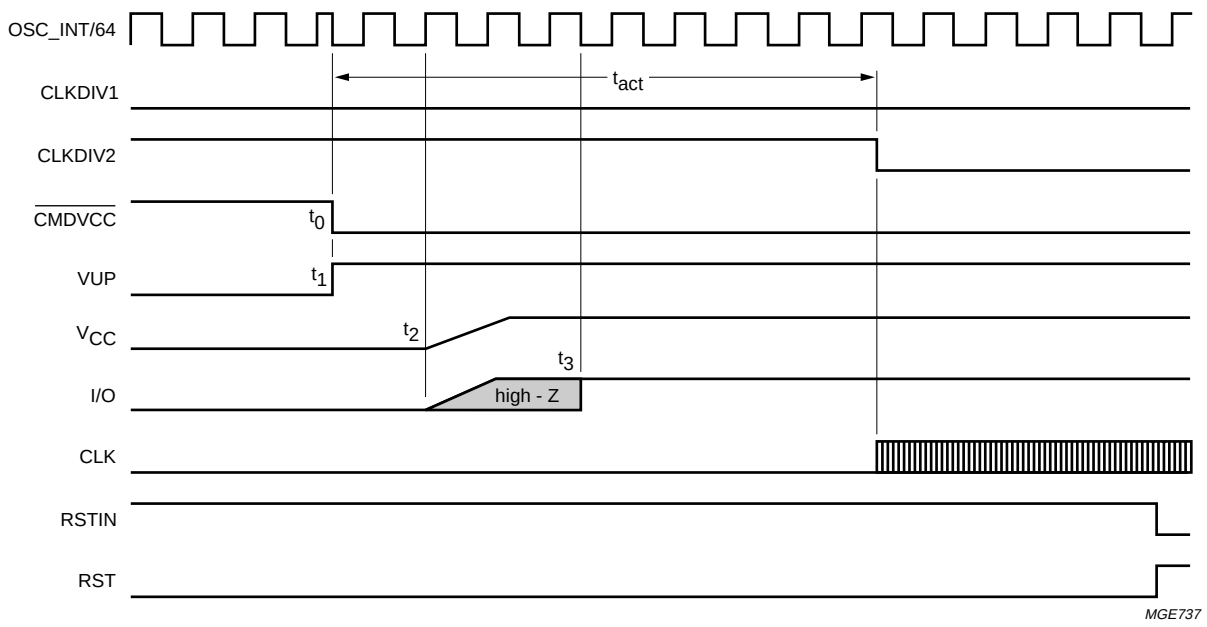


Fig.9 Activation sequence using $\overline{\text{CMDVCC}}$, CLKDIV1 and CLKDIV2 signals to enable CLK.

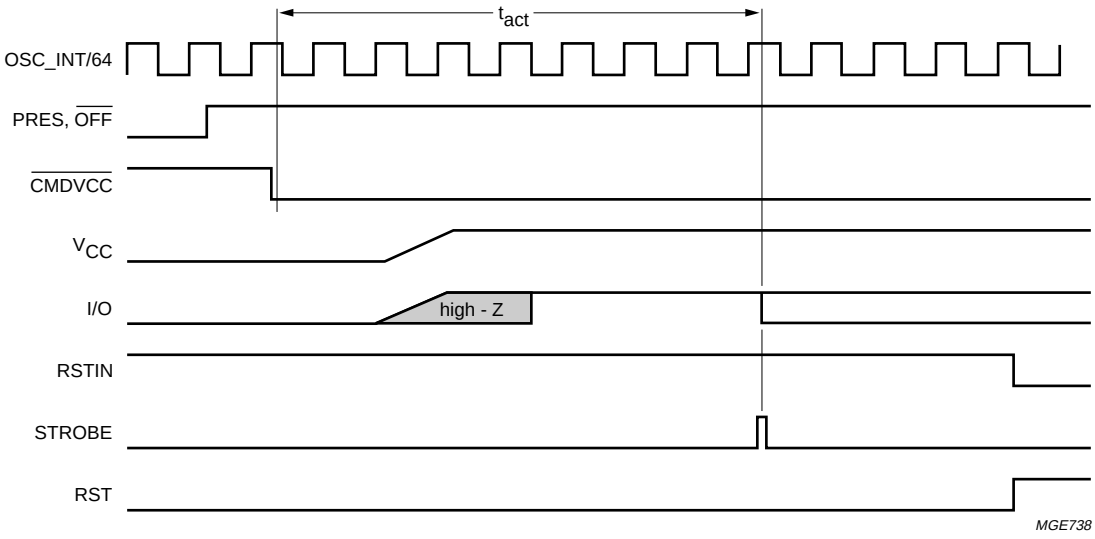


Fig.10 Activation sequence for synchronous application.

DEACTIVATION SEQUENCE

When a session is completed, the microcontroller sets the $\overline{\text{CMDVCC}}$ line to HIGH state or MODE line to LOW state. The circuit then executes an automatic deactivation sequence by counting the sequencer down and ends in idle mode.

Figures 11 and 12 illustrate the deactivation sequence as described below:

1. RST goes LOW ($t_{11} \approx t_{10}$)
2. CLK is stopped ($t_{12} = t_{11} + \frac{1}{2}T$)
3. I/O, AUX1, AUX2 are outputs into high-impedance state ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 1\frac{1}{2}T$); a special circuitry ensures that I/O remains below V_{CC} during falling slope of V_{CC}
5. VUP falls ($t_{15} = t_{11} + 5T$).

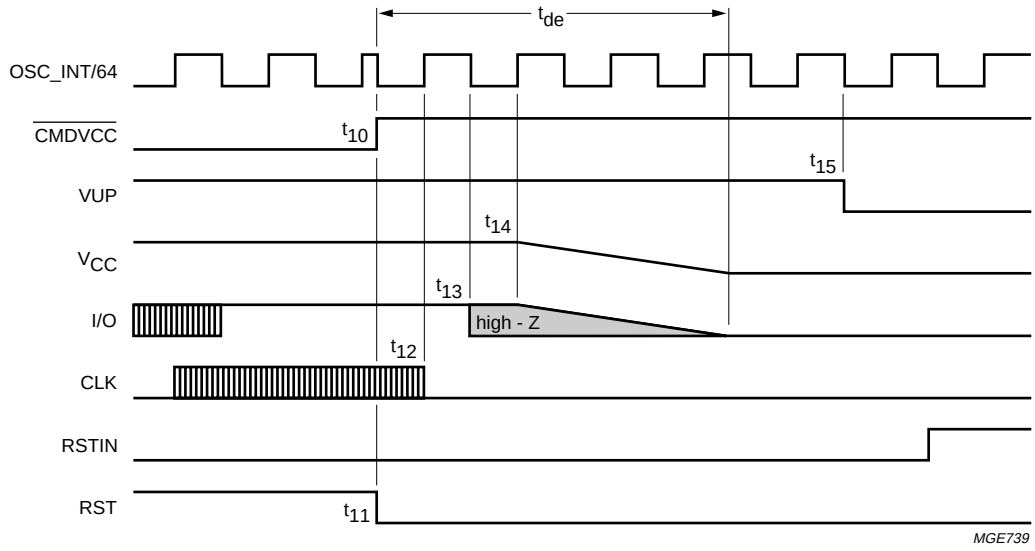


Fig.11 Deactivation sequence.

Fault detection

The following fault conditions are monitored by the circuit:

- Short-circuit or high current on V_{CC}
- Removing card during transaction
- V_{DD} dropping
- Overheating.

When one or more of these faults are detected, the circuit pulls the interrupt line $\overline{OFF}$ to its active LOW state and a deactivation sequence is initiated. In case the card is present the interrupt line $\overline{OFF}$ is set to HIGH when the microcontroller has reset the $\overline{CMDVCC}$ line HIGH (after completion of the deactivation sequence). In case the card is not present $\overline{OFF}$ remains LOW.

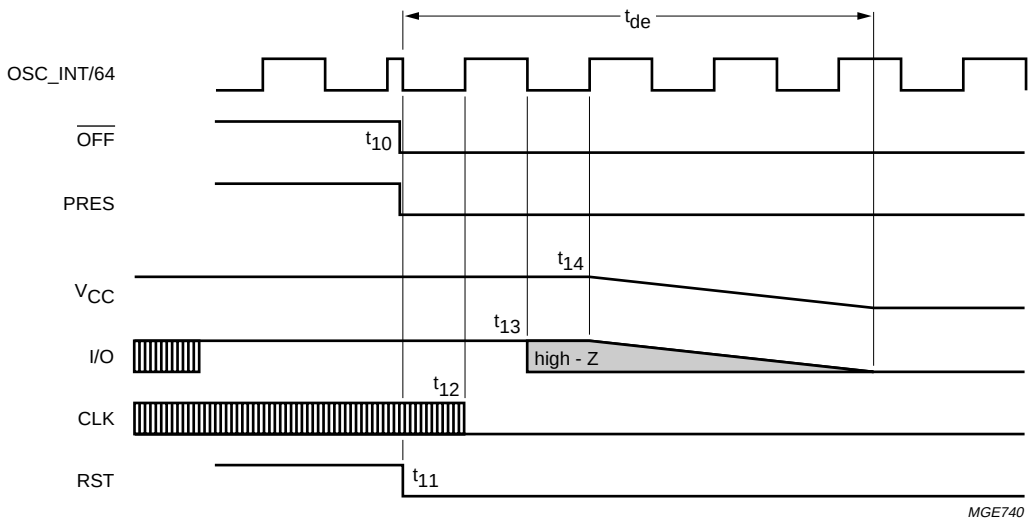


Fig.12 Emergency deactivation sequence.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.3	+6.5	V
$V_{i(CMOS)}$	voltage on CMOS pins				
	XTAL1, XTAL2, ALARM, $\overline{ALARM}$, MODE, RSTIN, CLKSEL, AUX2UC, AUX1UC, CLKDIV1, $\overline{CLKDIV2}$, $\overline{CLKOUT}$, STROBE, $\overline{CMDVCC}$ and $\overline{OFF}$		–0.3	+6.5	V
$V_{i(card)}$	voltage on card contact pins				
	I/O, AUX2, $\overline{PRES}$, PRES, AUX1, CLK, RST and V_{CC}		–0.3	+6.5	V
V_{es}	electrostatic handling				
	on pins I/O, RST, V_{CC}, CLK, AUX1, AUX2, PRES and $\overline{PRES}$		–6	+6	kV
	on all other pins		–2	+2	kV
T_{stg}	storage temperature		–55	+125	°C
P_{tot}	continuous total power dissipation				
	TDA8002T	T_{amb} = –25 to +85 °C	–	0.56	W
	TDA8002G	T_{amb} = –25 to +85 °C	–	0.46	W
T_{amb}	operating ambient temperature		–25	+85	°C
T_j	junction temperature		–	150	°C

Note

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

HANDLING

Every pin withstands the ESD test according to MIL-STD-883C class 3 for card contacts, class 2 for the remaining. Method 3015 (HBM 1500 Ω, 100 pF) 3 positive pulses and 3 negative pulses on each pin referenced to ground.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient in free air		
	SOT136-1	70	K/W
	SOT401-1	91	K/W

CHARACTERISTICS

V_{DD} = 5 V; T_{amb} = 25 °C; f_{xtal} = 10 MHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	positive supply voltage	option 5 V power supply (TDA8002xx/5)	4.5	5	6.5	V
		option 3.3 V or 5 V power supply (TDA8002xx/3)	3	5	6.5	V
$I_{DD(sl)}$	supply current	sleep mode; V_{DD} = 5 V	–	–	200	µA
$I_{DD(idle)}$	supply current	idle mode; V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	6	mA
$I_{DD(active)}$	supply current	active mode				
		V_{DD} = 5 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	9	mA
		V_{DD} = 3.3 V; f_{CLK} = 2.5 MHz; f_{CLKOUT} = 10 MHz	–	–	12	mA
V_{th2}	threshold voltage on V_{DD} for voltage supervisor	falling				
		option 5 V power supply (TDA8002xx/5)	3.9	4.05	4.2	V
		option 3.3 V or 5 V power supply (TDA8002xx/3)	2.6	2.7	2.8	V
		rising				
		option 5 V power supply (TDA8002xx/5)	4	4.2	4.4	V
		option 3.3 or 5 V power supply (TDA8002xx/3)	2.7	2.85	2.99	V
V_{hys2}	hysteresis on V_{th2}		100	150	200	mV
CARD SUPPLY						
$V_{CC(O)(idle)}$	output voltage	idle mode	–	–	0.4	V
$V_{CC(O)(active)}$	output voltage	active mode				
		I_{CC} < 20 mA: DC load with 3 V < V_{DD} < 3.3 V	4.75	–	5.25	V
		I_{CC} < 65 mA: DC load with 3.3 V < V_{DD} < 6.5 V	4.75	–	5.25	V
		I_{CC} = 40 mA: AC load	4.6	–	5.4	V
$I_{CC(O)}$	output current	$V_{CC(O)}$ = from 0 to 5 V	–	–	65	mA
		V_{CC} short-circuited to ground	–	–	100	mA
SR	slew rate	rising or falling slope	0.12	0.17	0.22	V/µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal connections (XTAL1 and XTAL2)						
C_{ext}	external capacitors	note 1	–	15	–	pF
f_{xtal}	resonance frequency	note 2	2	–	24	MHz
Data lines						
GENERAL						
t_{edge}	delay between falling edge of I/O, AUX1, AUX2 and I/OUC, AUX1UC, AUX2UC		–	200	–	ns
	delay between falling edge of I/OUC, AUX1UC, AUX2UC and I/O, AUX1, AUX2		–	200	–	ns
t_r, t_f	rise and fall times	$C_i = C_o = 30$ pF	–	–	0.5	µs
DATA LINES I/O, AUX1 AND AUX2						
$V_{OH(I/O)}$	HIGH-level output voltage on data lines	$I_{OH} = -20$ µA	$V_{CC} - 0.5$	–	$V_{CC} + 0.1$	V
		$I_{OH} = -100$ µA	3.5	–	–	V
$V_{OL(I/O)}$	LOW-level output voltage on data lines	$I_{I/O} = 1$ mA	–	–	300	mV
$V_{IH(I/O)}$	HIGH-level input voltage on data lines		1.8	–	V_{CC}	V
$V_{IL(I/O)}$	LOW-level input voltage on data lines		0	–	0.8	V
$V_{I/O(idle)}$	voltage on data lines outside a session		–	–	0.4	V
R_{pu}	internal pull-up resistance between data lines and V_{CC}		8	10	12	kΩ
I_{edge}	current from data lines when active pull-up is active		–	1	–	mA
$I_{IL(I/O)}$	LOW-level input current on data lines	$V_{IL} = 0.4$ V	–	–	–600	µA
$I_{IH(I/O)}$	HIGH-level input current on data lines	$V_{IH} = V_{CC}$	–	–	10	µA
DATA LINES I/OUC, AUX1UC AND AUX2UC						
$V_{OH(I/OUC)}$	HIGH-level output voltage on data lines	$I_{OH} = -20$ µA	$V_{DD} - 1$	–	$V_{DD} + 0.2$	V
$V_{OL(I/OUC)}$	LOW-level output voltage on data lines	$I_{I/OUC} = 1$ mA	–	–	300	mV
$V_{IH(I/OUC)}$	HIGH-level input voltage on data lines		$0.7V_{DD}$	–	V_{DD}	V
$V_{IL(I/OUC)}$	LOW-level input voltage on data lines		0	–	$0.3V_{DD}$	V
$Z_{I/OUC(idle)}$	impedance on data lines outside a session		10	–	–	MΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ALARM, $\overline{\text{ALARM}}$ and $\overline{\text{OFF}}$ when connected (open-drain outputs)						
$I_{OH(\overline{ALARM})}$	HIGH-level output current on pin $\overline{\text{ALARM}}$	$V_{OH(\overline{ALARM})}$ = 5 V	–	–	5	µA
$V_{OL(\overline{ALARM})}$	LOW-level output voltage on pin $\overline{\text{ALARM}}$	$I_{OL(\overline{ALARM})}$ = 2 mA	–	–	0.4	V
$I_{OH(OFF)}$	HIGH-level output current on pin $\overline{\text{OFF}}$	$V_{OH(OFF)}$ = 5 V	–	–	5	µA
$V_{OL(OFF)}$	LOW-level output voltage on pin $\overline{\text{OFF}}$	$I_{OL(OFF)}$ = 2 mA	–	–	0.4	V
$I_{OL(ALARM)}$	LOW-level output current on pin ALARM	$V_{OL(ALARM)}$ = 0 V	–	–	–5	µA
$V_{OH(ALARM)}$	HIGH-level output voltage on pin ALARM	$I_{OH(ALARM)}$ = –2 mA	V_{DD} – 1	–	–	V
t_W	ALARM pulse width		6	–	20	ms
Clock output (CLKOUT; powered from V_{DD})						
f_{CLKOUT}	frequency on CLKOUT		0	–	20	MHz
		low power	–	16	–	kHz
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{DD} – 0.5	–	–	V
t_r, t_f	rise and fall times	C_L = 15 pF; notes 3 and 5	–	–	8	ns
δ	duty factor	C_L = 15 pF; notes 3 and 5	40	–	60	%
Internal oscillator						
f_{int}	frequency of internal oscillator	active mode	2.2	2.7	3.2	MHz
		sleep mode	–	32	–	kHz
Card reset output (RST)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
$t_{d(RST)}$	delay between RSTIN and RST	RST enabled	–	–	100	ns
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	4.3	–	V_{CC}	V
		I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
Card clock output (CLK)						
$V_{O(inact)}$	output voltage	inactive modes	0	–	0.3	V
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	0	–	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –50 µA	V_{CC} – 0.5	–	V_{CC}	V
t_r	rise time	C_L = 30 pF; note 3	–	–	8	ns
t_f	fall time	C_L = 30 pF; note 3	–	–	8	ns
δ	duty factor	C_L = 30 pF; note 3	45	–	55	%
SR	slew rate (rise and fall)		0.2	–	–	V/ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Strobe input (STROBE)						
f_{STROBE}	frequency on STROBE		0	–	20	MHz
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
Logic inputs (CLKSEL, CLKDIV1, CLKDIV2, MODE, $\overline{\text{CMDVCC}}$ and RSTIN); note 4						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		1.8	–	V_{DD}	V
Logic inputs (PRES, $\overline{\text{PRES}}$); note 4						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD}	V
$I_{IL(PRES)}$	LOW-level input current on pin PRES	V_{OL} = 0 V	–	–	–10	µA
$I_{IH(PRES)}$	HIGH-level input current on pin PRES		–	–	10	µA
Protections						
T_{sd}	shut-down local temperature		–	135	–	°C
$I_{CC(sd)}$	shut-down current at V_{CC}		–	–	90	mA
Timing						
t_{act}	activation sequence duration	see Fig.9; guaranteed by design	–	180	220	µs
t_{de}	deactivation sequence duration	see Fig.11; guaranteed by design	50	70	90	µs
t_3	start of the window for sending CLK to the card	see Figs 8 and 9	–	–	130	µs
t_5	end of the window for sending CLK to the card	see Fig.8	150	–	–	µs

Notes

1. It may be necessary to put capacitors from XTAL1 and XTAL2 to ground depending on the choice of crystal or resonator.
2. When the oscillator is stopped in mode 1, XTAL1 is set to HIGH.
3. The transition time and duty cycle definitions are shown in Fig.13; $\delta = \frac{t_1}{t_1 + t_2}$
4. $\overline{\text{PRES}}$ and $\overline{\text{CMDVCC}}$ are active LOW; RSTIN and PRES are active HIGH.
5. CLKOUT transition time and duty cycle do not need to be tested.

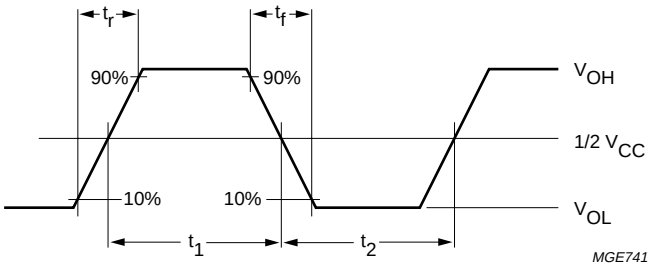


Fig.13 Definition of transition times.

APPLICATION INFORMATION

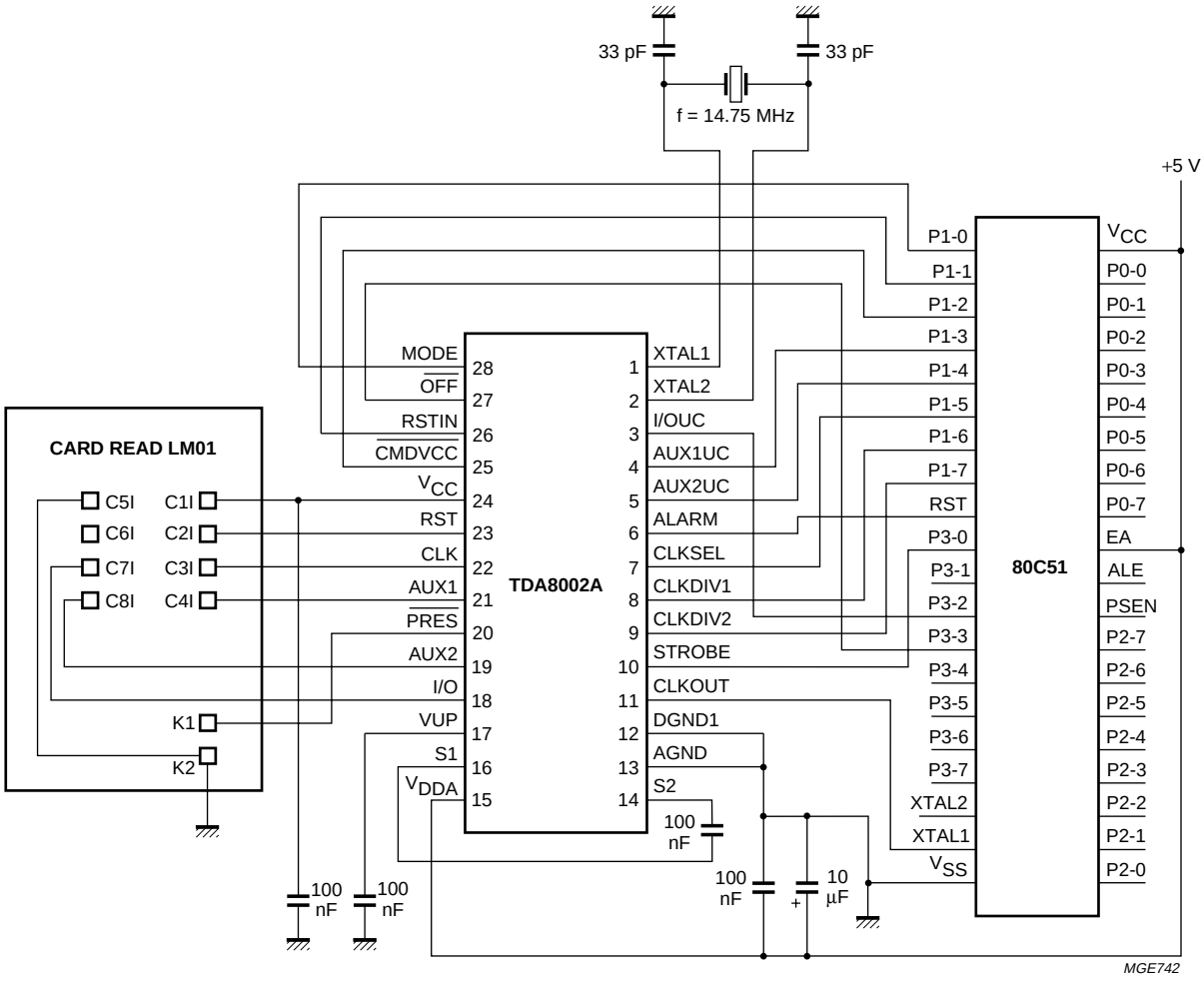
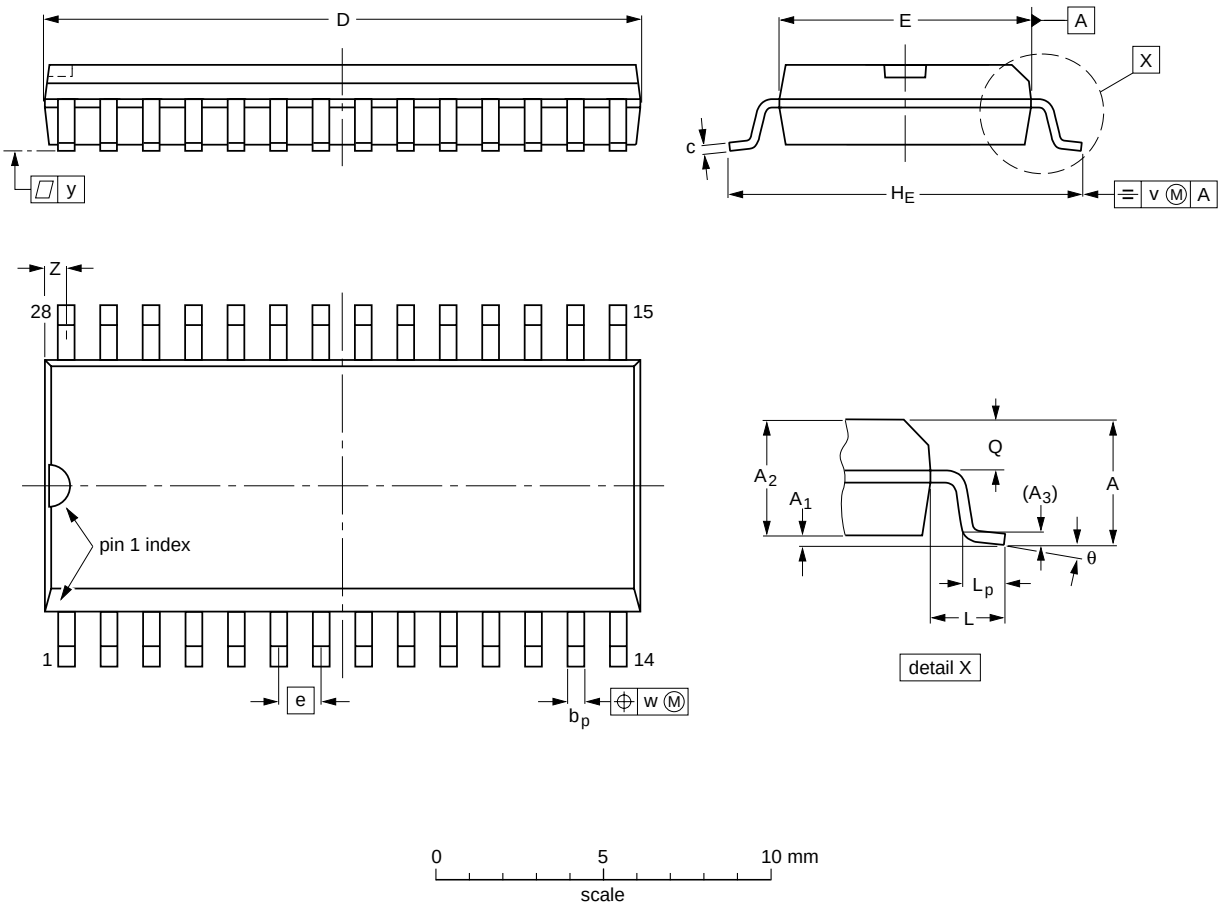


Fig.14 Application diagram (for more details, consult "*Application Note AN96096*").

PACKAGE OUTLINES

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

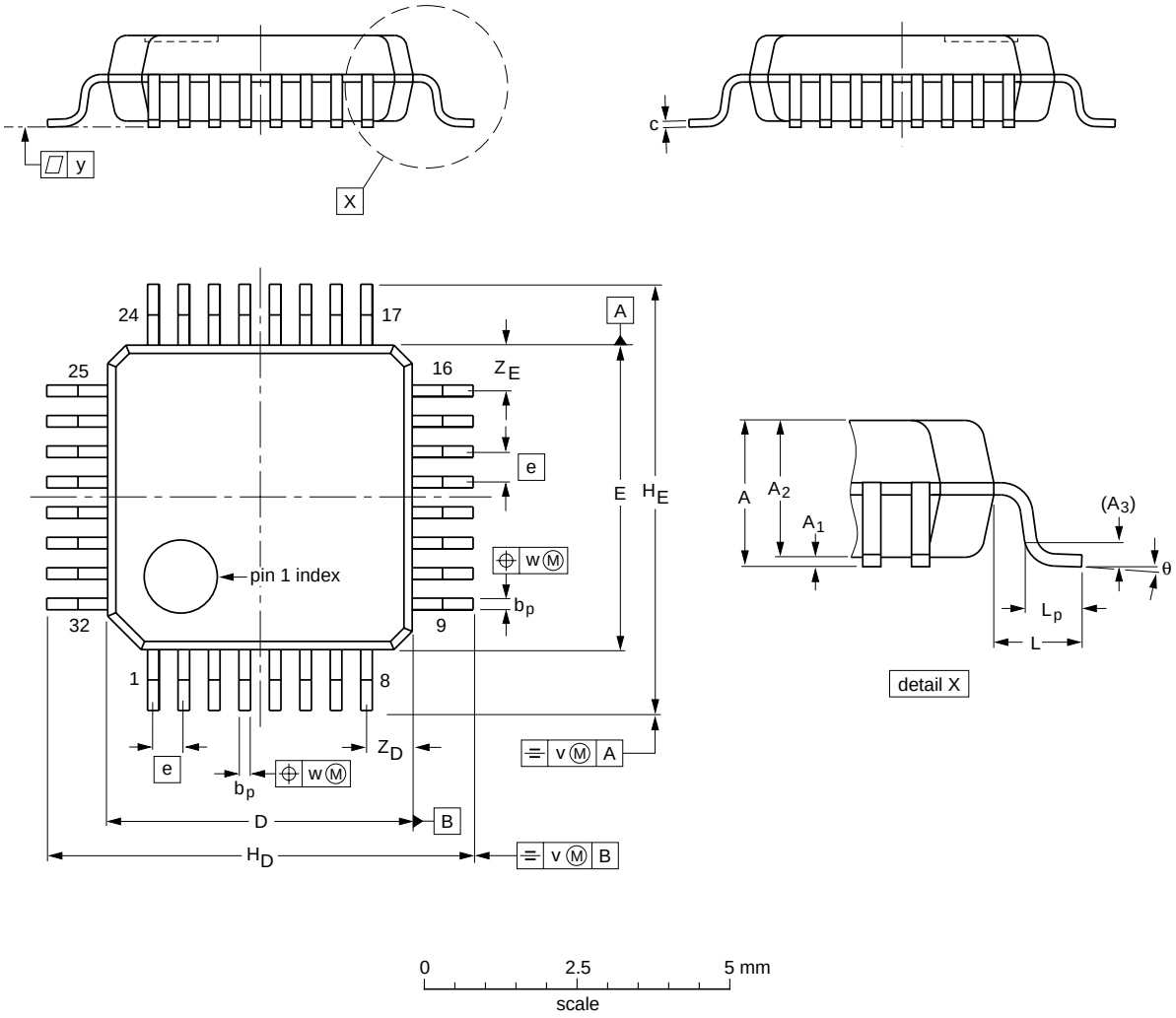
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

LQFP32: plastic low profile quad flat package; 32 leads; body 5 x 5 x 1.4 mm **SOT401-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.15 0.05	1.5 1.3	0.25	0.27 0.17	0.18 0.12	5.1 4.9	5.1 4.9	0.5	7.15 6.85	7.15 6.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT401-1						~~95-12-19~~ 97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP and SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

LQFP

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

METHOD (LQFP AND SO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 547047/1200/03/pp28 Date of release: 1997 Nov 04 Document order number: 9397 750 02454

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