

DATA SHEET

BSP110

**N-channel enhancement mode
vertical D-MOS transistor**

Product specification
File under Discrete Semiconductors, SC13b

April 1995

N-channel enhancement mode vertical D-MOS transistor

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DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a miniature SOT223 envelope and designed for use in telephone ringer circuits and for application in relay, high-speed and line transformer drivers.

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown

QUICK REFERENCE DATA

| | | | |
|--|---------------|------|--------------|
| Drain-source voltage | V_{DS} | max. | 80 V |
| Drain source voltage (non-repetitive peak; $t_p \leq 2$ ms) | $V_{DS(SM)}$ | max. | 100 V |
| Gate-source voltage (open drain) | $\pm V_{GSO}$ | max. | 20 V |
| Drain current (DC) | I_D | max. | 325 mA |
| Total power dissipation up to $T_{amb} = 25$ °C | P_{tot} | max. | 1.5 W |
| Drain-source ON-resistance $I_D = 200$ mA; $V_{GS} = 10$ V | $R_{DS(on)}$ | typ. | 4.5 Ω |
| | | max. | 7 Ω |
| Transfer admittance $I_D = 200$ mA; $V_{DS} = 15$ V | $ Y_{fs} $ | min. | 75 mS |
| | | typ. | 150 mS |

PINNING - SOT223

- 1 = gate
- 2 = drain
- 3 = source
- 4 = drain

MARKING CODE

BSP110

PIN CONFIGURATION

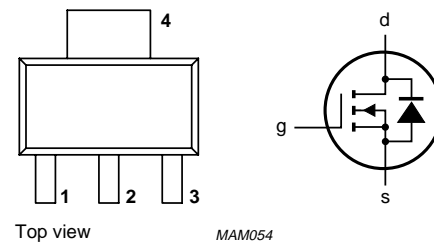


Fig.1 Simplified outline and symbol.

N-channel enhancement mode vertical D-MOS transistor

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| | | | |
|--|---------------|------|-----------------|
| Drain-source voltage | V_{DS} | max. | 80 V |
| Drain-source voltage (non-repetitive peak; $t_p \leq 2$ ms) | $V_{DS(SM)}$ | max. | 100 V |
| Gate-source voltage (open drain) | $\pm V_{GSO}$ | max. | 20 V |
| Drain current (DC) | I_D | max. | 325 mA |
| Drain current (peak) | I_{DM} | max. | 650 mA |
| Total power dissipation up to $T_{amb} = 25$ °C (note 1) | P_{tot} | max. | 1.5 W |
| Storage temperature range | T_{stg} | | -65 to + 150 °C |
| Junction temperature | T_j | max. | 150 °C |

THERMAL RESISTANCE

| | | | |
|-----------------------------------|---------------|---|----------|
| From junction to ambient (note 1) | $R_{th\ j-a}$ | = | 83.3 K/W |
|-----------------------------------|---------------|---|----------|

Note

- Device mounted on an epoxy printed-circuit board 40 mm × 40 mm × 1.5 mm; mounting pad for the drain lead min. 6 cm².

CHARACTERISTICS

 $T_j = 25$ °C unless otherwise specified

| | | | |
|--|-----------------|--------------|-----------------|
| Drain-source breakdown voltage $I_D = 10$ μA; $V_{GS} = 0$ | $V_{(BR)\ DSS}$ | min. | 80 V |
| Drain-source leakage current $V_{DS} = 60$ V; $V_{GS} = 0$ | I_{DSS} | max. | 1.0 μA |
| Gate-source leakage current $V_{GS} = 20$ V; $V_{DS} = 0$ | I_{GSS} | max. | 100 nA |
| Gate threshold voltage $I_D = 1$ mA; $V_{DS} = V_{GS}$ | $I_{GS(th)}$ | min. max. | 0.8 V 2.8 V |
| Drain-source ON-resistance (see Fig.4) $I_D = 150$ mA; $V_{GS} = 5$ V | $R_{DS(on)}$ | typ. max. | 7 Ω 10 Ω |
| $I_D = 200$ mA; $V_{GS} = 10$ V | $R_{DS(on)}$ | typ. max. | 4.5 Ω 7 Ω |
| Transfer admittance $I_D = 200$ mA; $V_{DS} = 5$ V | $ Y_{fs} $ | min. typ. | 75 mS 150 mS |
| Input capacitance at $f = 1$ MHz; $V_{DS} = 10$ V; $V_{GS} = 0$ | C_{iss} | typ. max. | 15 pF 30 pF |

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Output capacitance at $f = 1 \text{ MHz}$;

$V_{DS} = 10 \text{ V}$; $V_{GS} = 0$

| | | |
|-----------|------|-------|
| C_{oss} | typ. | 13 pF |
| | max. | 20 pF |

Feedback capacitance at $f = 1 \text{ MHz}$;

$V_{DS} = 10 \text{ V}$; $V_{GS} = 0$

| | | |
|-----------|------|------|
| C_{rss} | typ. | 3 pF |
| | max. | 6 pF |

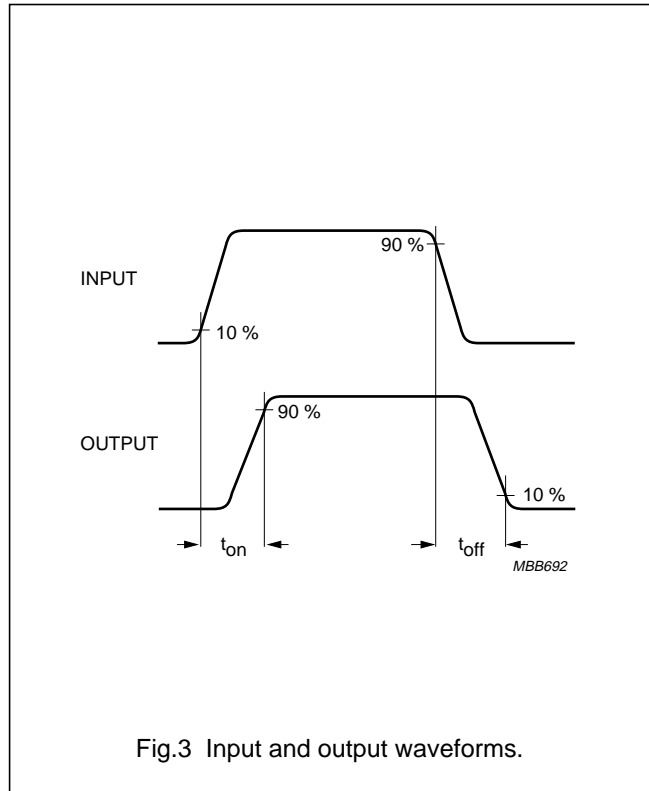
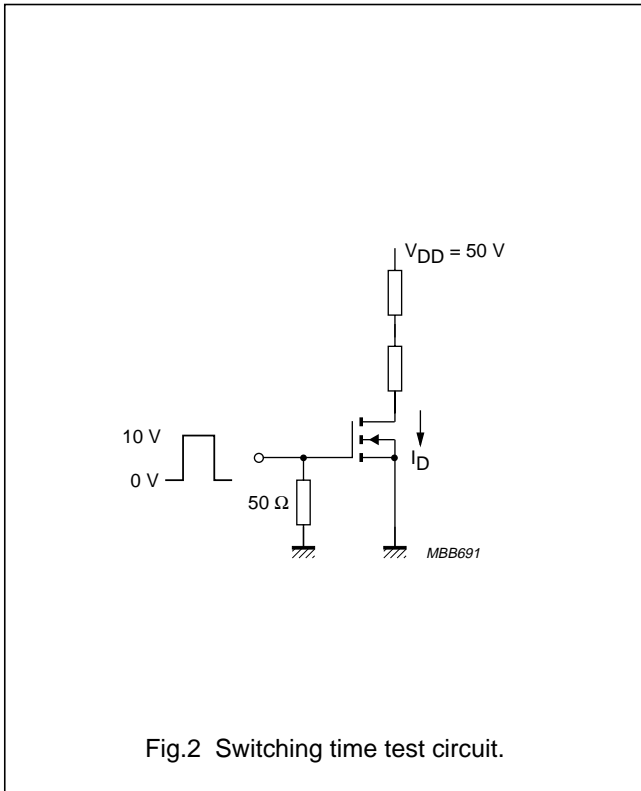
Switching times (see Figs 2 and 3)

$I_D = 200 \text{ mA}$; $V_{DD} = 50 \text{ V}$;

$V_{GS} = 0 \text{ to } 10 \text{ V}$

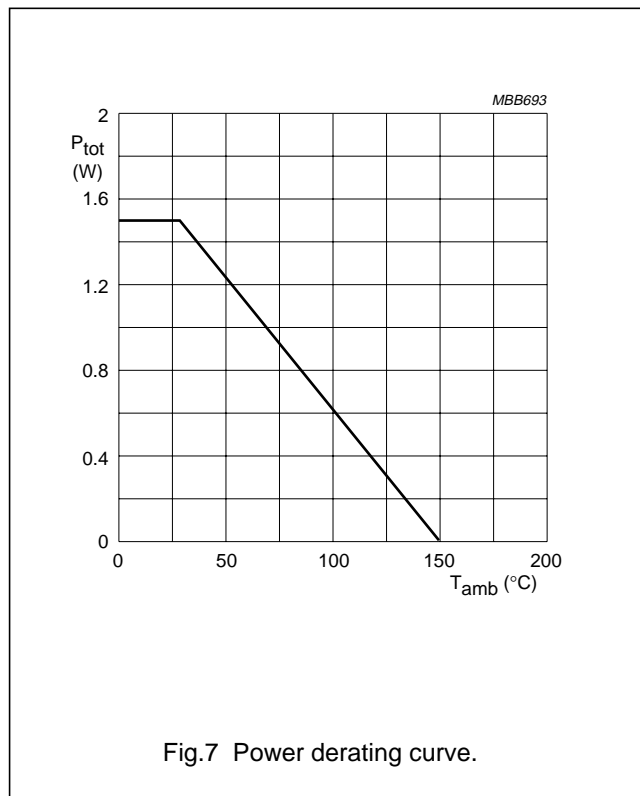
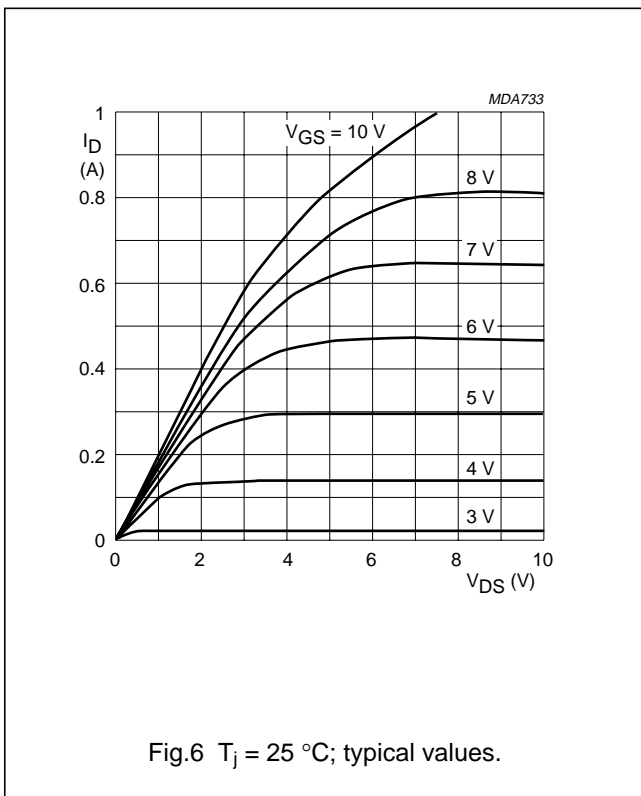
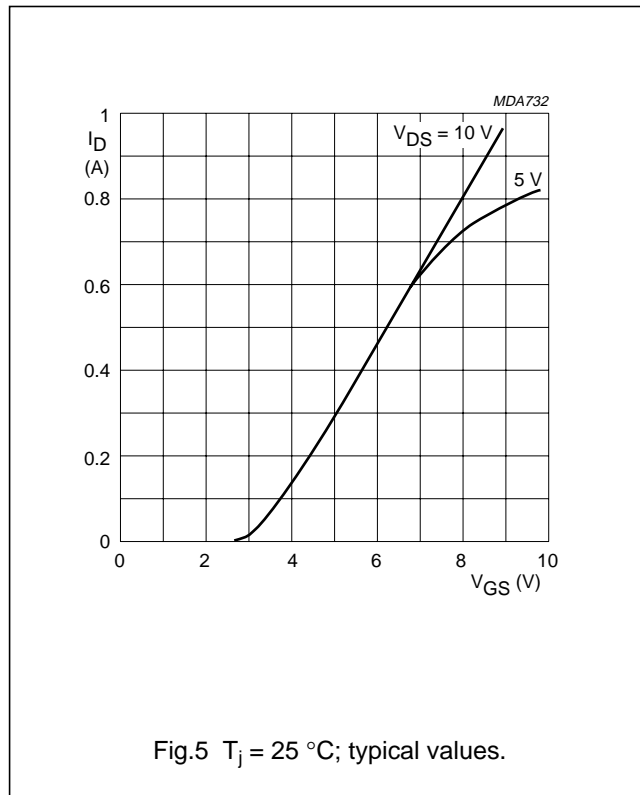
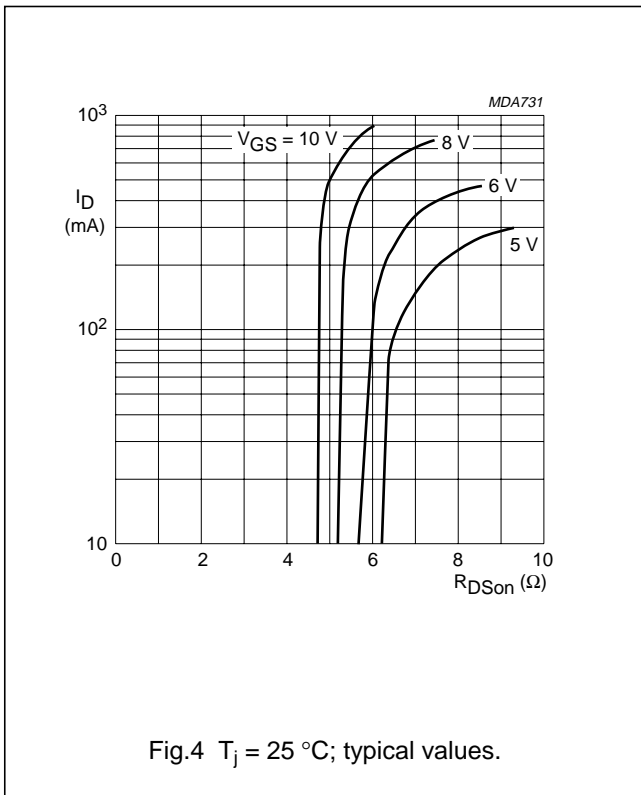
| | | |
|----------|------|------|
| t_{on} | typ. | 2 ns |
| | max. | 5 ns |

| | | |
|-----------|------|-------|
| t_{off} | typ. | 5 ns |
| | max. | 10 ns |



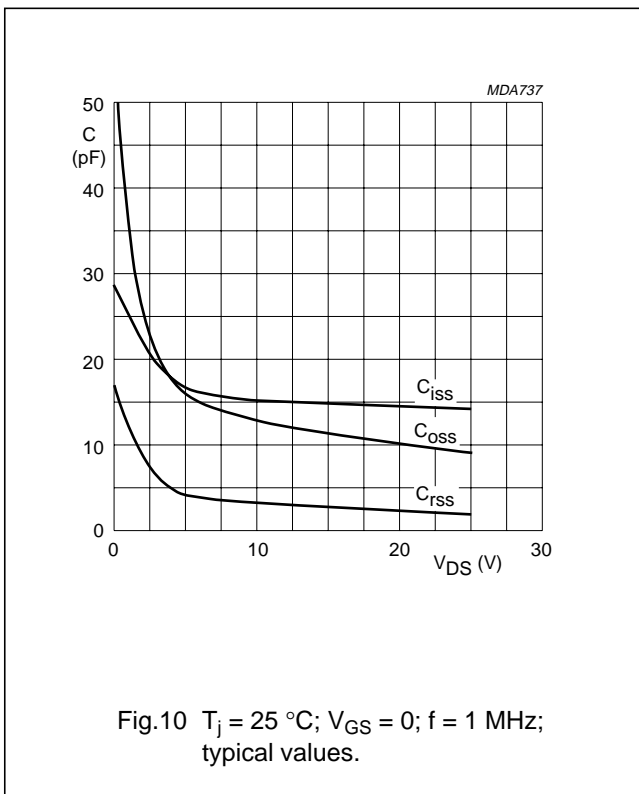
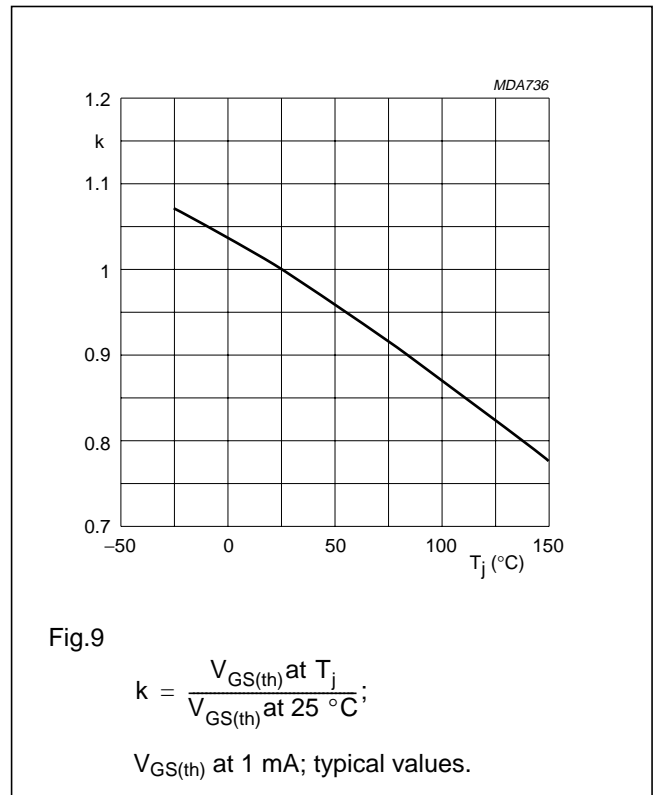
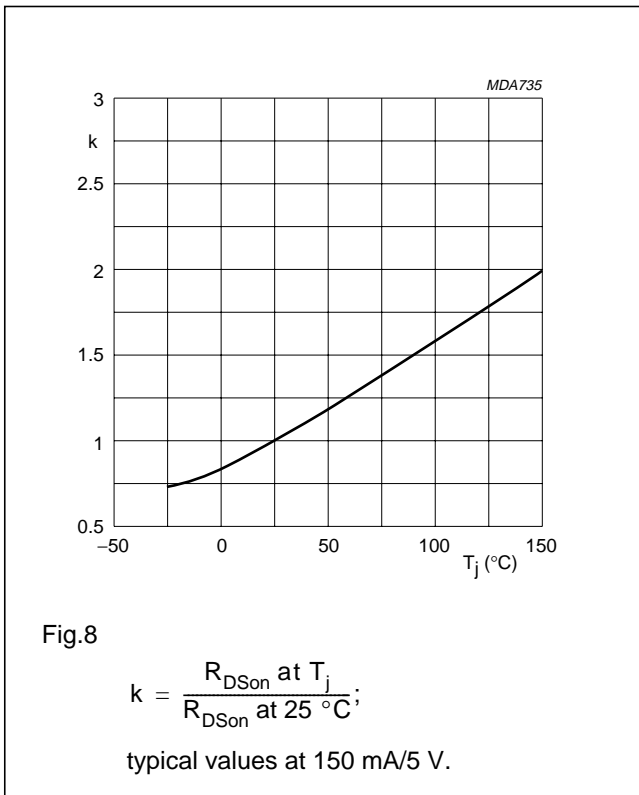
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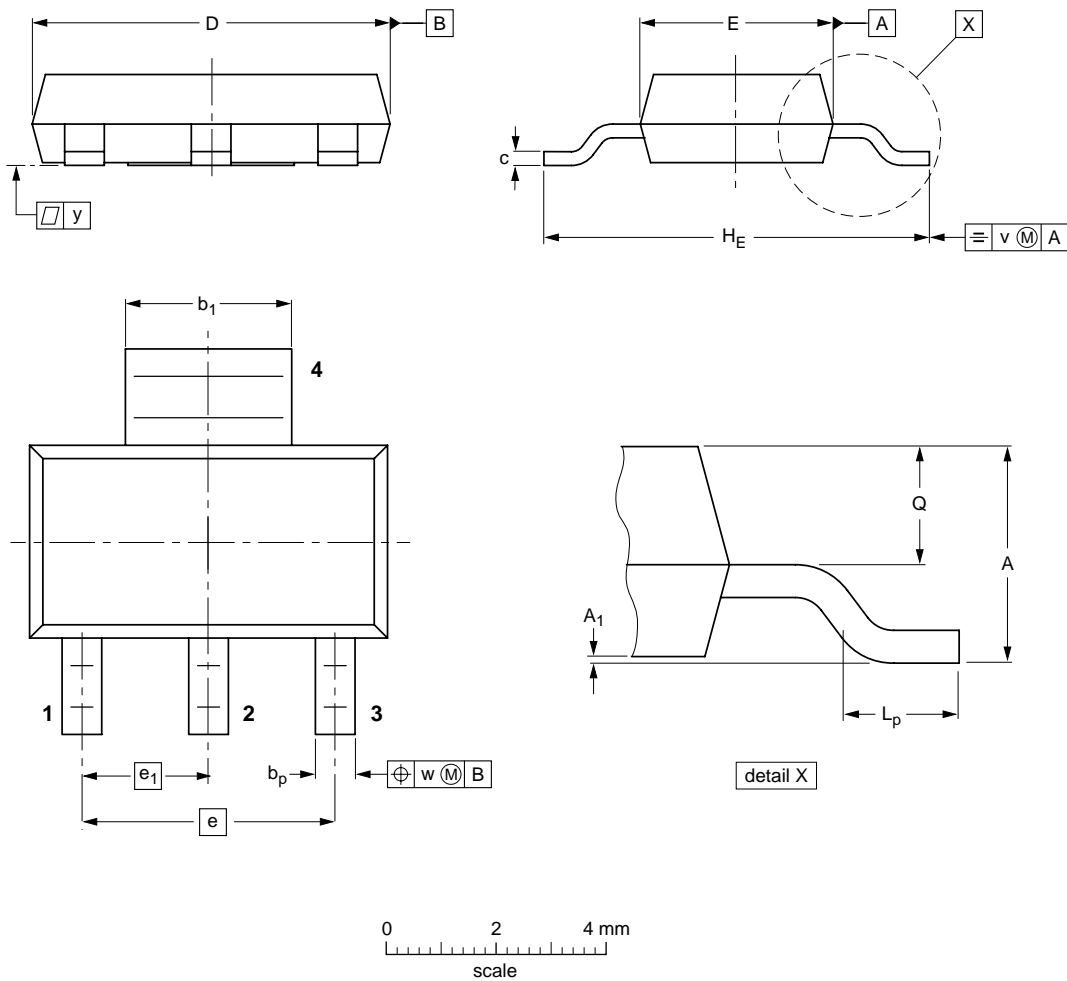
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ | b _p | b ₁ | c | D | E | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|----------------|----------------|----------------|--------------|------------|------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.8 1.5 | 0.10 0.01 | 0.80 0.60 | 3.1 2.9 | 0.32 0.22 | 6.7 6.3 | 3.7 3.3 | 4.6 | 2.3 | 7.3 6.7 | 1.1 0.7 | 0.95 0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT223 | | | | | | 96-11-11 97-02-28 |

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DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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Printed in The Netherlands

137107/00/01/pp12

Date of release: April 1995

Document order number: 9397 750 02469

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