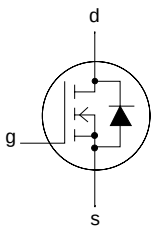
TrenchMOS™ transistor Logic level FET

PHN1015

FEATURES

- 'Trench' technology
- Low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low-profile surface mount package

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 25 V

I_D = 9 A

$R_{DS(ON)} \leq 18\ m\Omega$

$R_{DS(ON)} \leq 15\ m\Omega$

GENERAL DESCRIPTION

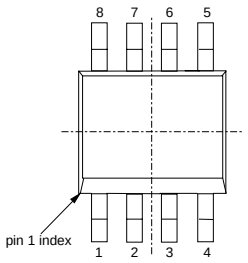
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHN1015 is supplied in the SOT96 (SO8) 8-leaded, low profile, surface mounting package.

PINNING

PIN	DESCRIPTION
1-3	source
4	gate
5-8	drain

SOT96 (SO8)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	25	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	25	V
V_{GS}	Gate-source voltage	-	-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150^{\circ}C$	-	± 20	V
I_D	Drain current (DC)	T_a = 25 ˚C, $t_p \leq 10$ s	-	9	A
		T_a = 100 ˚C, $t_p \leq 10$ s	-	5.7	A
I_{DM}	Drain current (pulse peak value)	T_a = 25 ˚C	-	36	A
P_{tot}	Total power dissipation	T_a = 25 ˚C	-	2.5	W
		T_a = 70 ˚C	-	1.6	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	FR4 board, minimum footprint, $t_p \leq 10$ s.	-	50	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	25	-	-	V
		T_j = -55˚C	22	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1	1.5	2	V
		T_j = 150˚C	0.6	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	-	9	14	mΩ
		V_{GS} = 5 V; I_D = 10 A	-	13	18	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 150˚C	-	-	31	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	8	20	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	10	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 25 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 150˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 20 A; V_{DD} = 24 V; V_{GS} = 10 V	-	52	-	nC
Q_{gs}	Gate-source charge		-	5.6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	14	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 15 V; I_D = 25 A;	-	8.4	20	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5 Ω	-	63	100	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	60	100	ns
t_f	Turn-off fall time		-	66	100	ns
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1300	-	pF
C_{oss}	Output capacitance		-	430	-	pF
C_{rss}	Feedback capacitance		-	228	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_a = 25 ˚C, $t_p \leq$ 10 s	-	-	9.2	A
I_{DRM}	Pulsed reverse drain current		-	-	37	A
V_{SD}	Diode forward voltage	I_F = 10 A; V_{GS} = 0 V	-	0.8	1.2	V
t_{rr}	Reverse recovery time	I_F = 10 A; -dI_F/dt = 100 A/µs;	-	70	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.1	-	µC

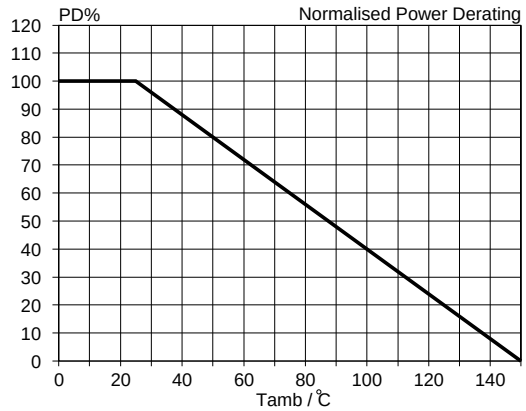


Fig.1. Normalised power dissipation.
PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_a)

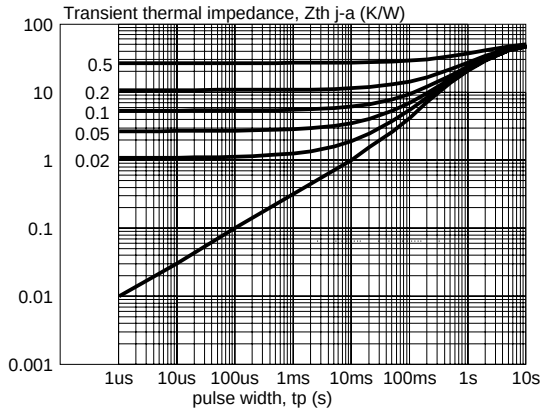


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}a}$ = f(t); parameter D = t_p/T

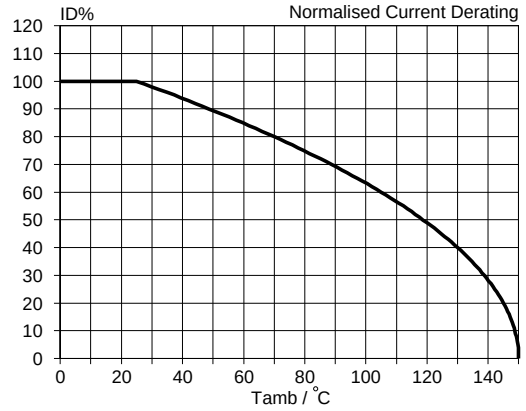


Fig.2. Normalised continuous drain current.
ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_a); conditions: V_{GS} ≥ 5 V

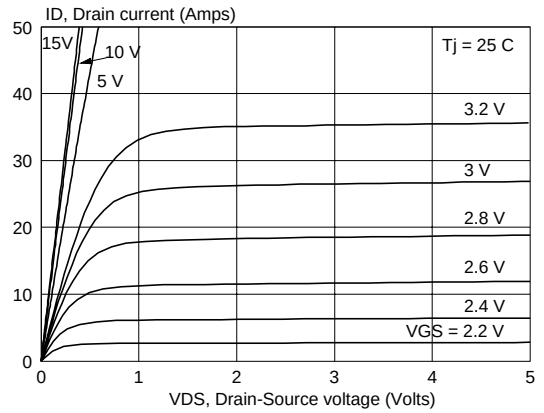


Fig.5. Typical output characteristics, T_j = 25 ˚C.
I_D = f(V_{DS}); parameter V_{GS}

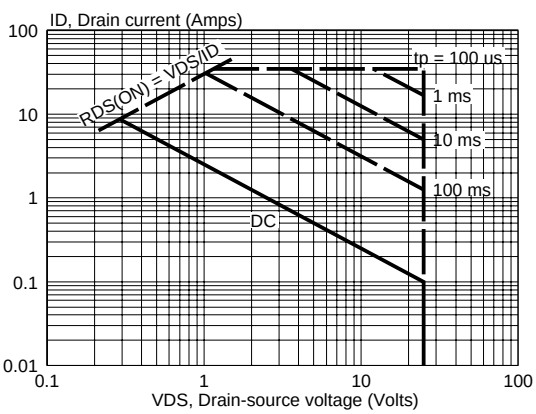


Fig.3. Safe operating area. T_a = 25 ˚C
I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

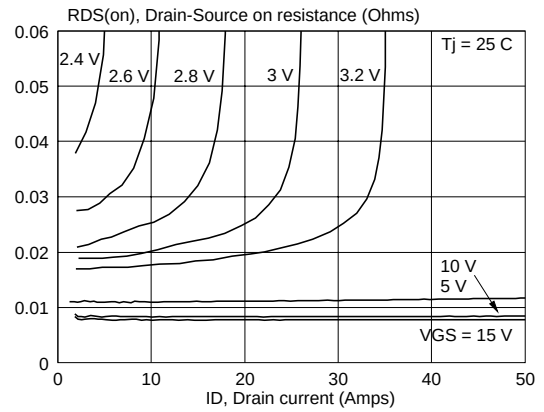


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)}$ = f(I_D); parameter V_{GS}

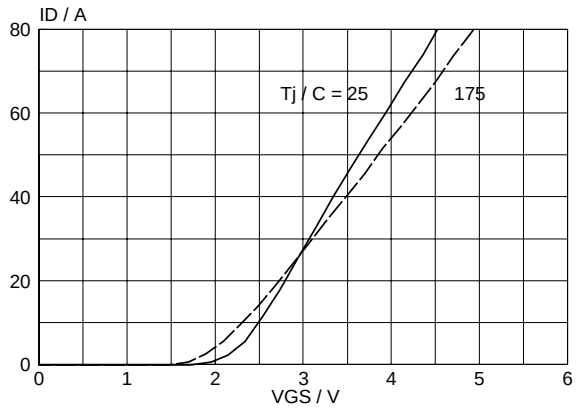


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$

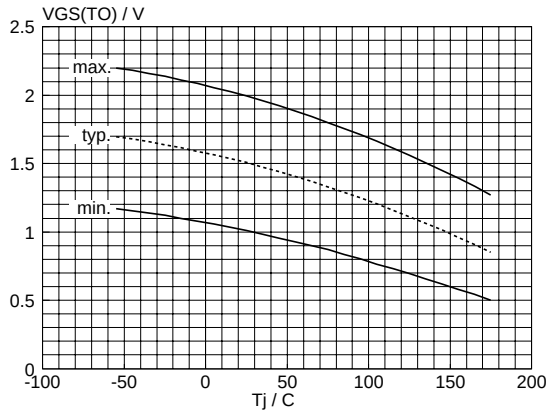


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

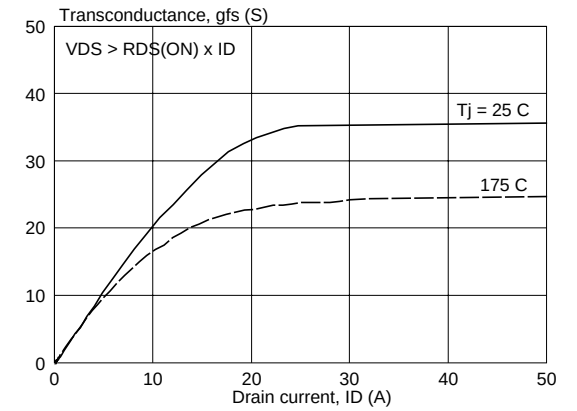


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$

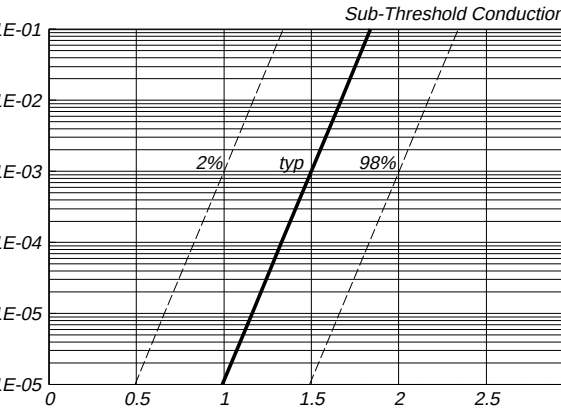


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

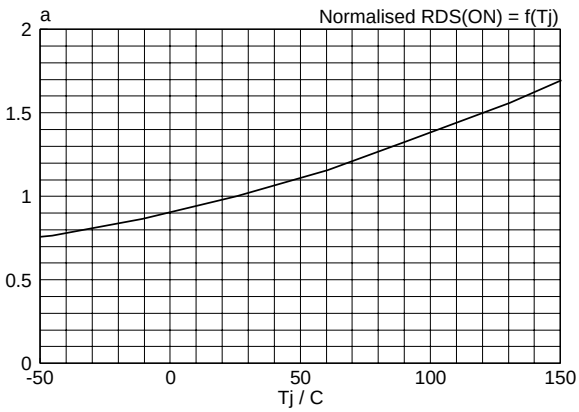


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$

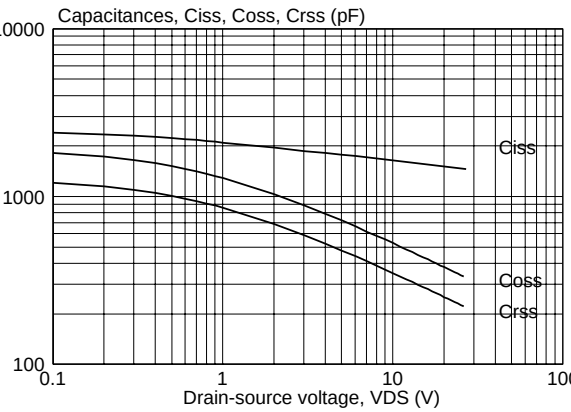


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

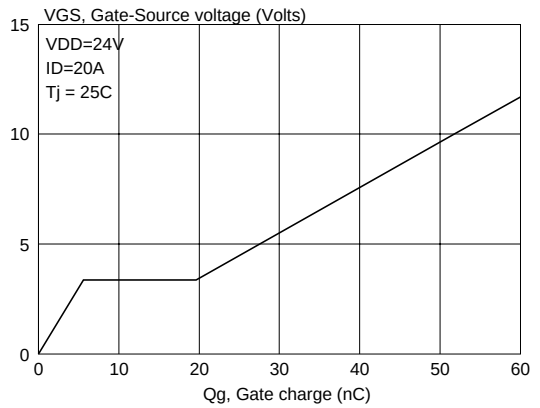


Fig.13. Typical turn-on gate-charge characteristics. $V_{GS} = f(Q_G)$

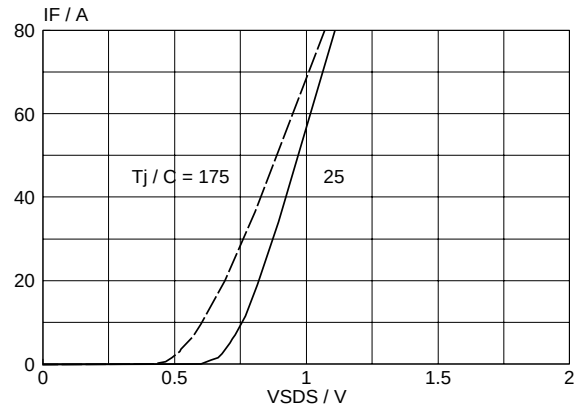


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

Dimensions in mm

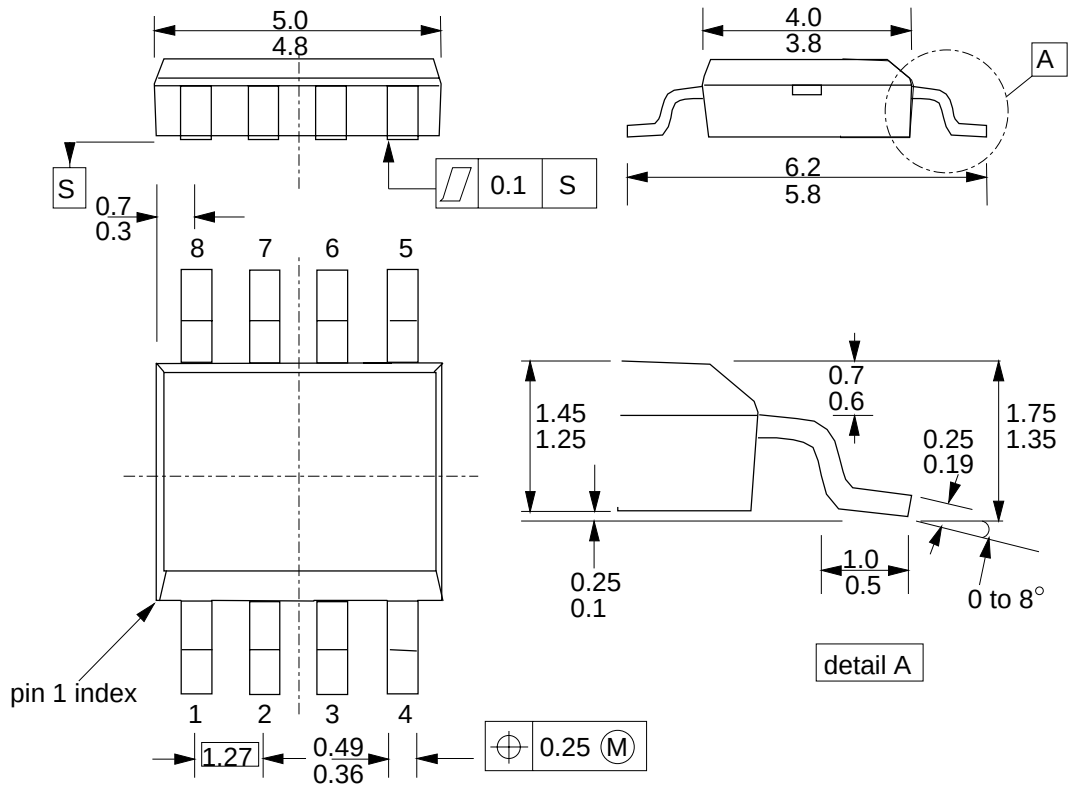


Fig.15. SOT96 (SO8).

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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