

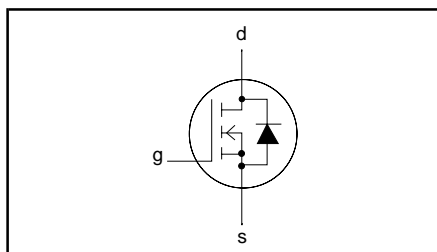
TrenchMOS™ transistor Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$V_{DSS} = 25\text{ V}$
$I_D = 48\text{ A}$
$R_{DS(ON)} \leq 21\text{ m}\Omega$ ($V_{GS} = 5\text{ V}$)
$R_{DS(ON)} \leq 16\text{ m}\Omega$ ($V_{GS} = 10\text{ V}$)

GENERAL DESCRIPTION

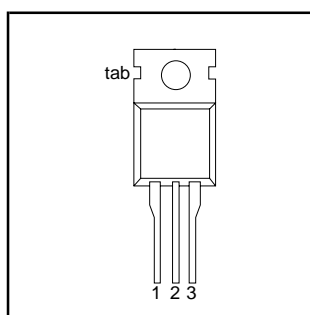
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The combination of very low on-state resistance and low switching losses make this device the optimum choice in high speed computer motherboard d.c. to d.c. converters.

The PHP50N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.
 The PHB50N03LT is supplied in the SOT404 surface mounting package.
 The PHD50N03LT is supplied in the SOT428 surface mounting package.

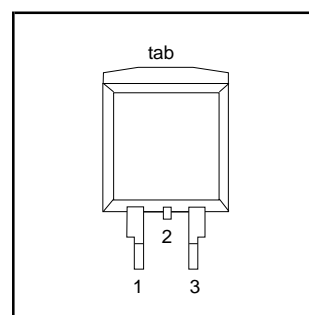
PINNING

PIN	DESCRIPTION
1	gate
2	drain ¹
3	source
tab	drain

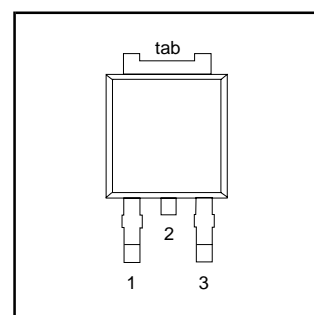
SOT78 (TO220AB)



SOT404



SOT428



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$	-	25	V
V_{DGR}	Drain-gate voltage	$T_j = 25\text{ }^\circ\text{C}$ to $175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	Gate-source voltage		-	± 15	V
V_{GSM}	Pulsed gate-source voltage	$T_j \leq 150\text{ }^\circ\text{C}$	-	± 20	V
I_D	Continuous drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	48	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$	-	34	A
I_{DM}	Pulsed drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	-	180	A
P_D	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	86	W
T_j, T_{stg}	Operating junction and storage temperature		-55	175	$^\circ\text{C}$

¹ It is not possible to make connection to pin 2 of the SOT428 or SOT404 packages.

TrenchMOS™ transistor
Logic level FET
PHP50N03LT, PHB50N03LT, PHD50N03LT
THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.75	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 and SOT428 packages, pcb mounted, minimum footprint	-	60	-	K/W
			-	50	-	K/W

ELECTRICAL CHARACTERISTICS
 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA};$ $T_j = -55^\circ\text{C}$	25 22	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1 0.5 -	1.5 - -	2 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ $V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ (SOT428 package) $V_{GS} = 5\text{ V}; I_D = 25\text{ A}$ $V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 175^\circ\text{C}$	- - - -	13 15 18 -	16 18 21 39	mΩ mΩ mΩ mΩ
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 25\text{ A}$	8	27	-	S
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 175^\circ\text{C}$	- -	0.05 -	10 500	μA μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$Q_{g(tot)}$	Total gate charge	$I_D = 20\text{ A}; V_{DD} = 24\text{ V}; V_{GS} = 10\text{ V}$	-	40	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	10	-	nC
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 25\text{ A};$	-	10	20	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_G = 5\ \Omega$	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	50	75	ns
t_f	Turn-off fall time		-	30	45	ns
L_d	Internal drain inductance	Measured tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1050	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Feedback capacitance		-	140	-	pF

TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

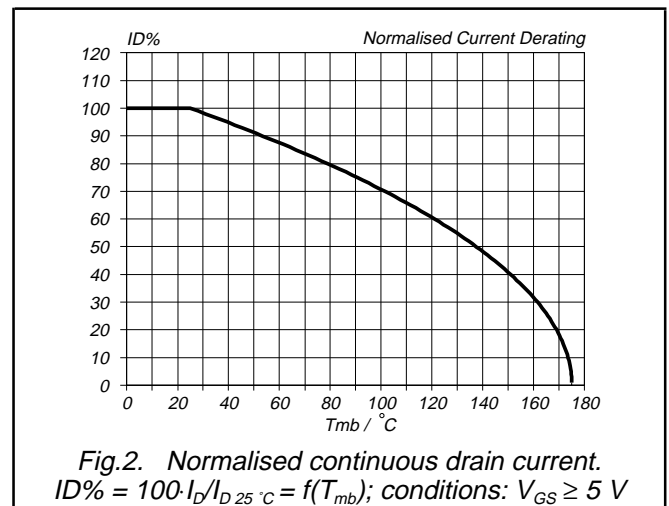
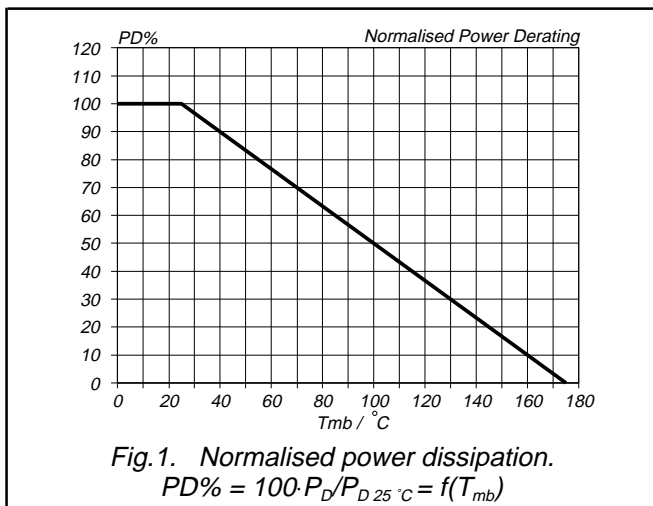
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _S	Continuous source current (body diode)		-	-	48	A
I _{SM}	Pulsed source current (body diode)		-	-	180	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 40 A; V _{GS} = 0 V	-	0.95 1.0	1.2 -	V
t _{rr}	Reverse recovery time	I _F = 40 A; -di _F /dt = 100 A/μs; V _{GS} = -10 V; V _R = 25 V	-	52	-	ns
Q _{rr}	Reverse recovery charge		-	0.08	-	μC

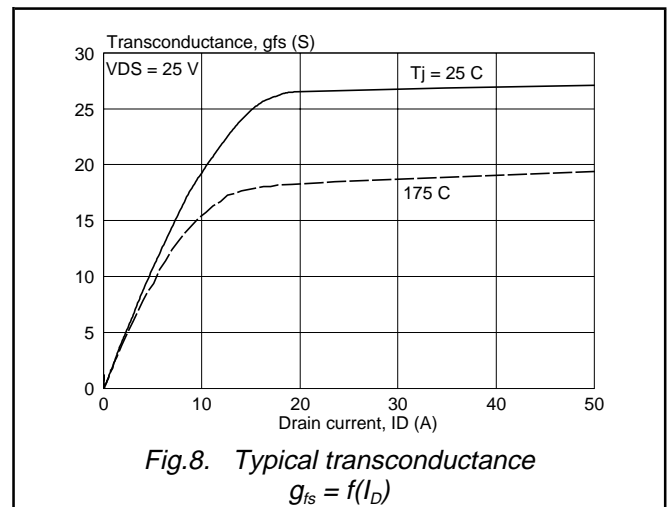
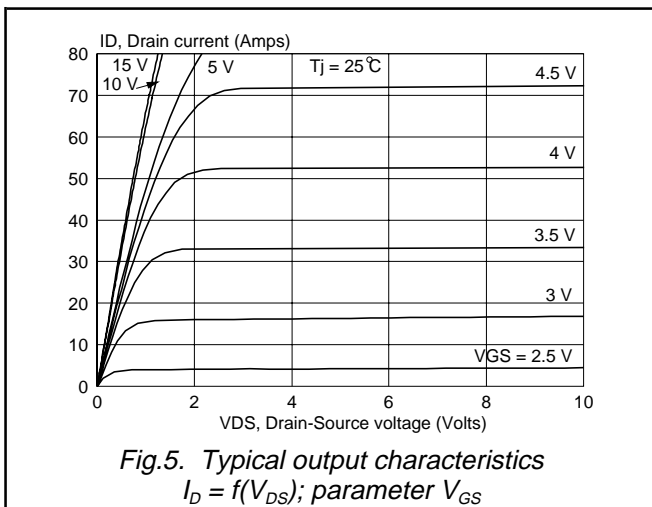
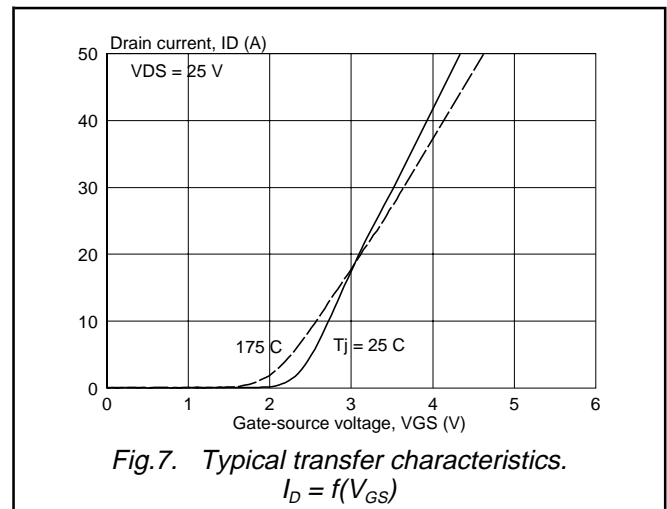
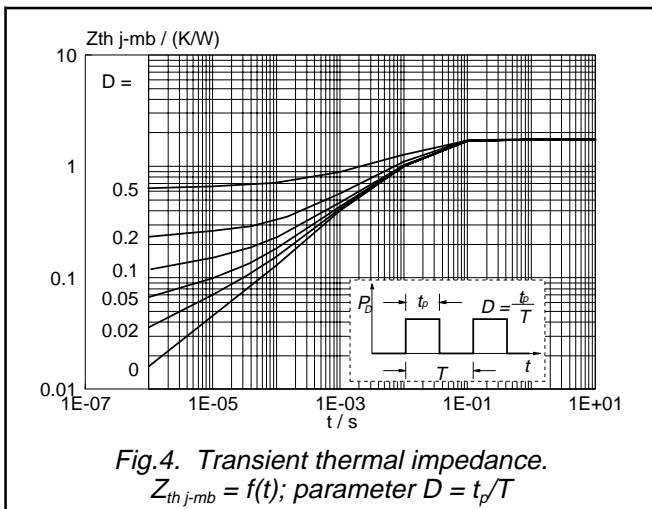
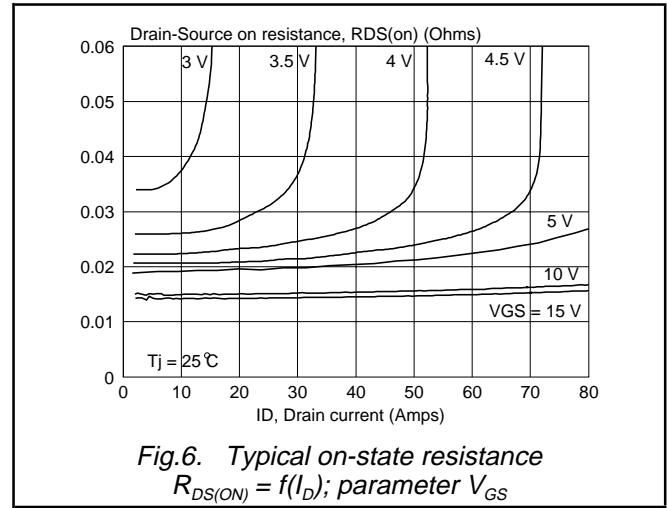
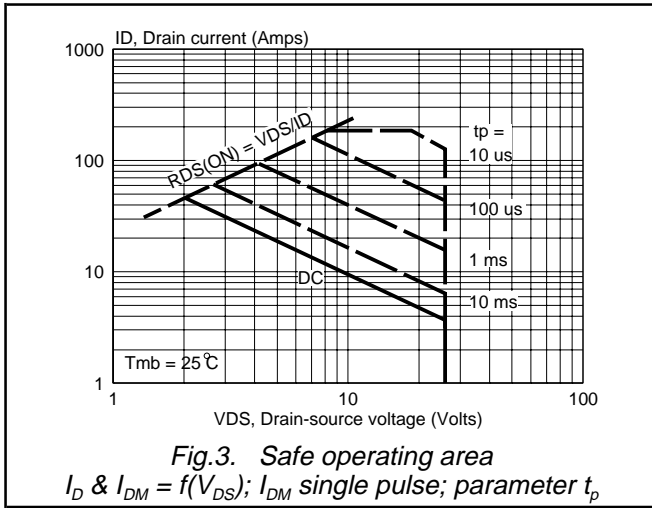
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 25 A; V _{DD} ≤ 15 V; V _{GS} = 10 V; R _{GS} = 50 Ω; T _{mb} = 25 °C	-	60	mJ



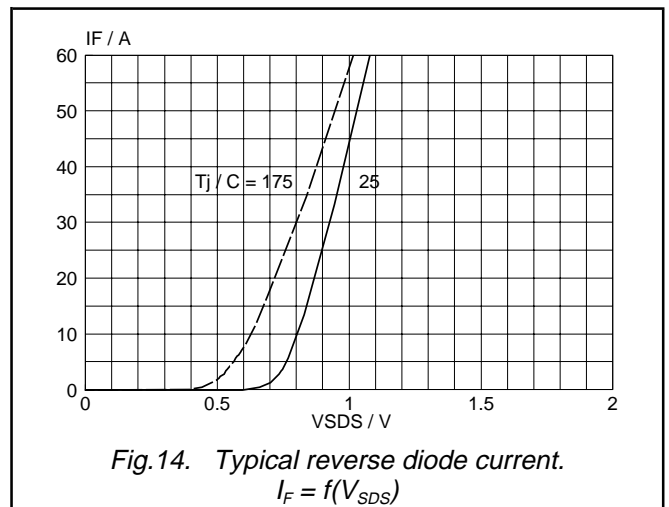
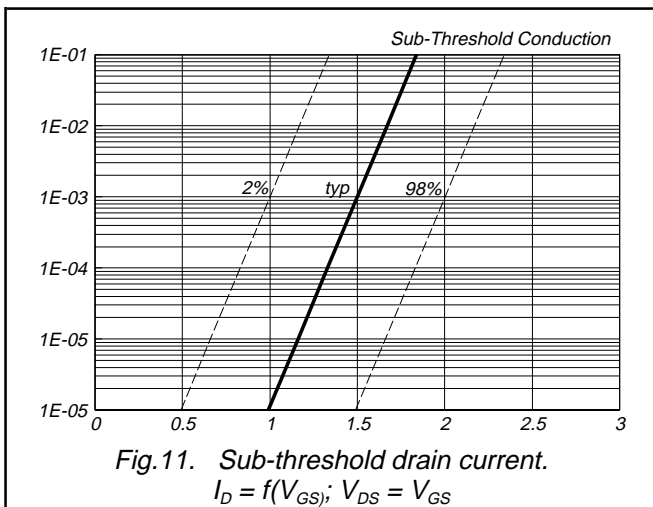
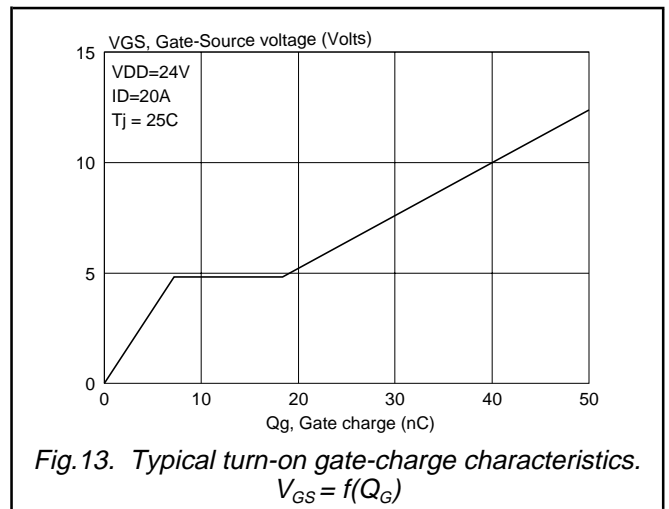
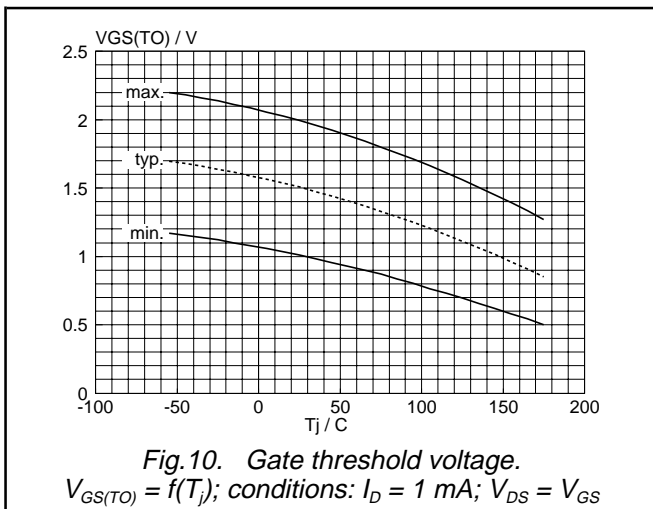
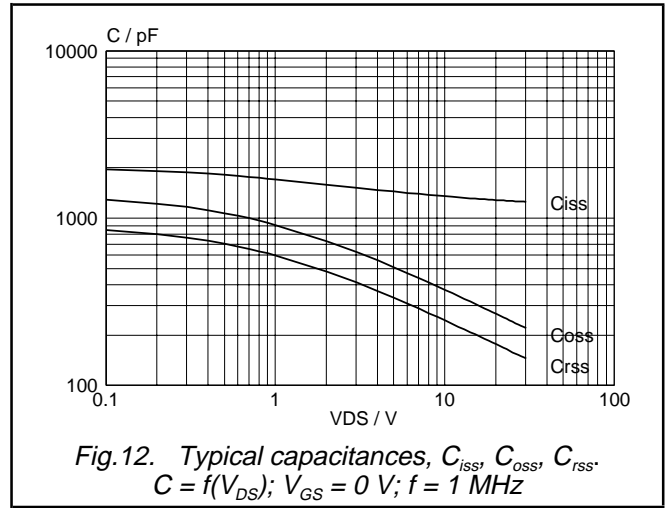
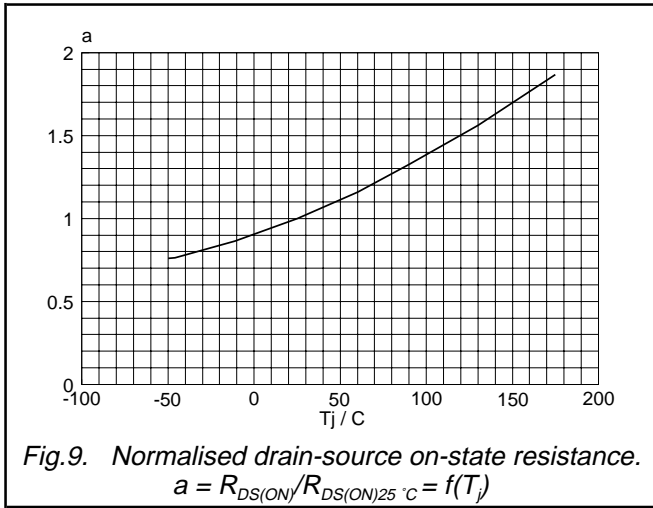
TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT



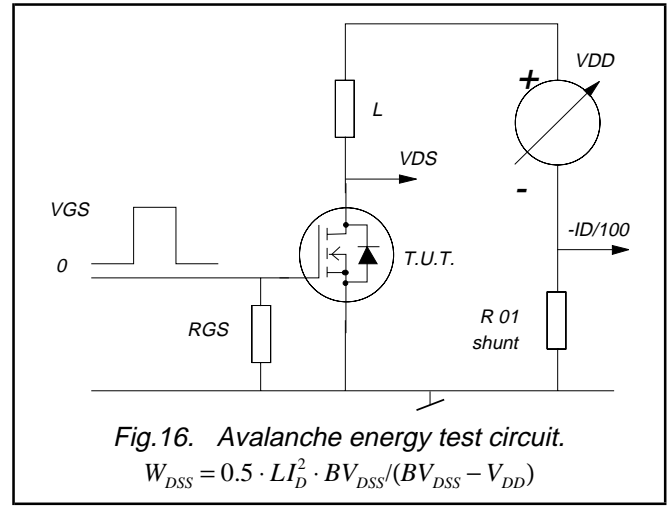
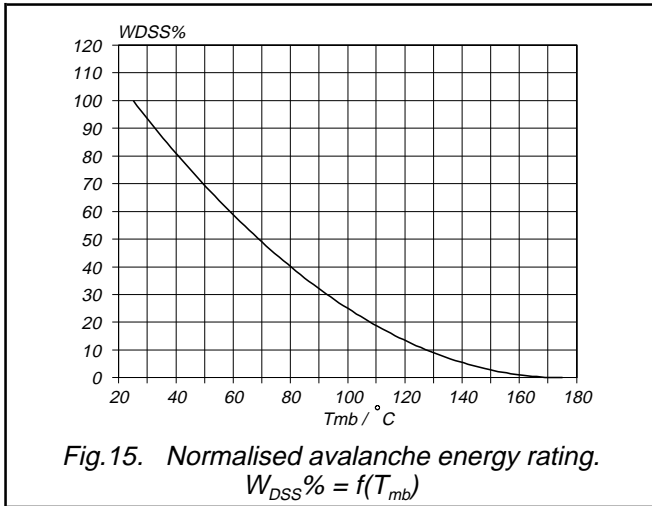
TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT



TrenchMOS™ transistor
Logic level FET

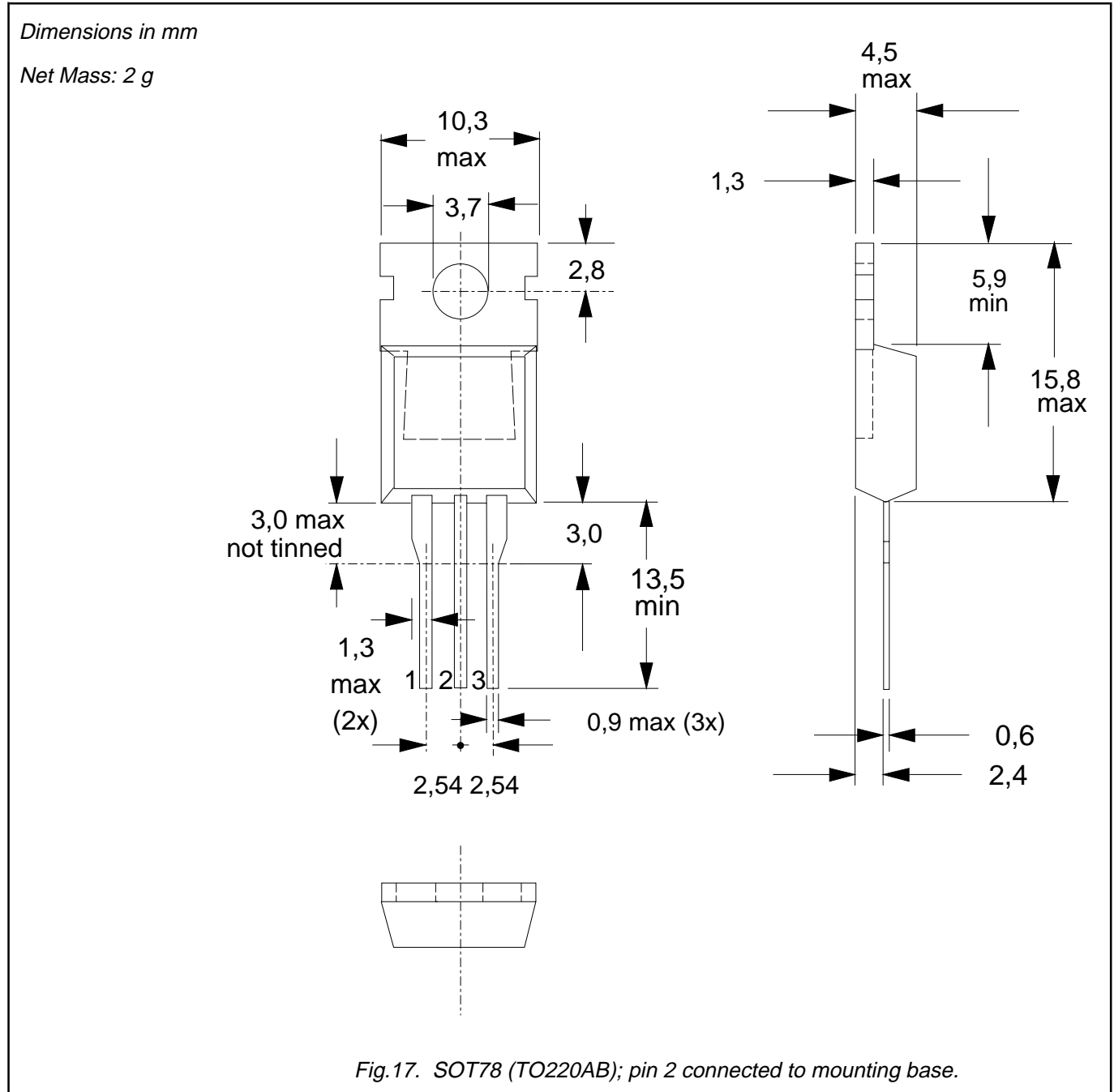
PHP50N03LT, PHB50N03LT, PHD50N03LT



TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

MECHANICAL DATA



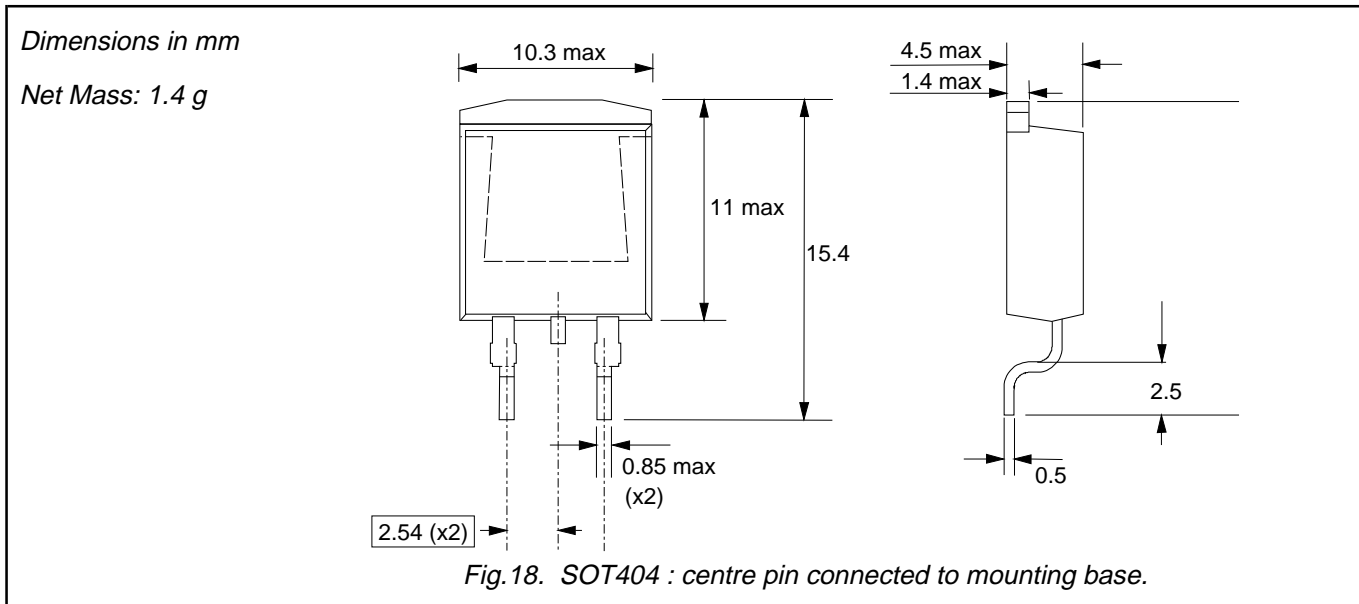
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

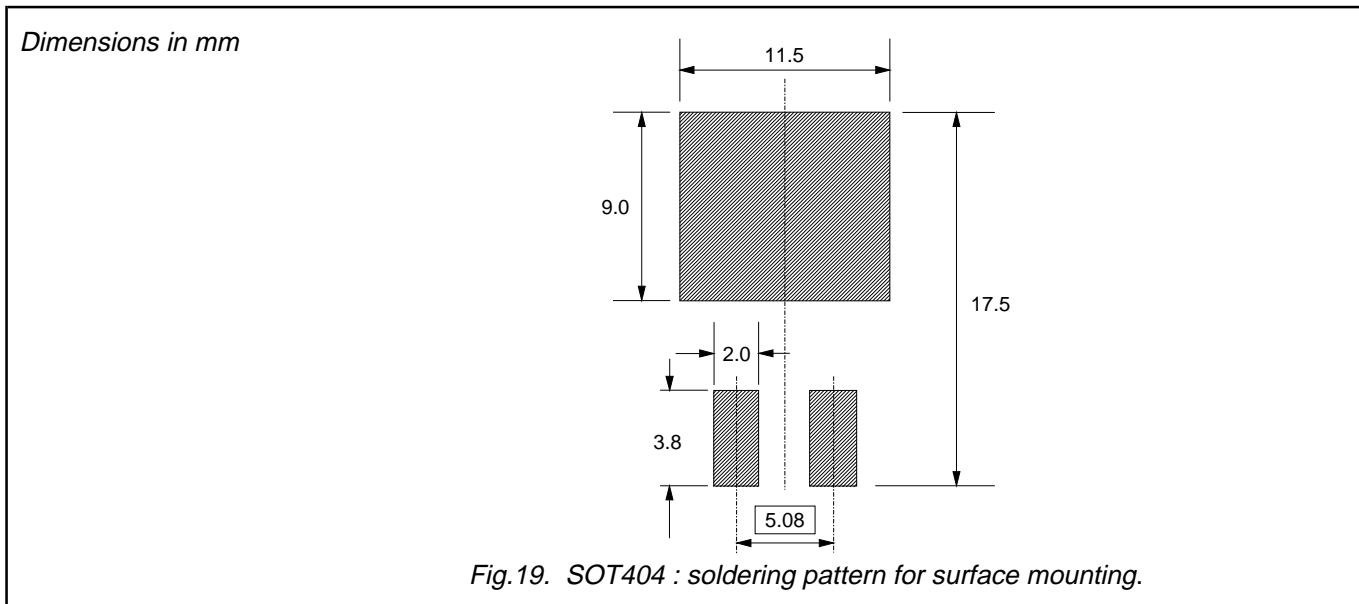
TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

MECHANICAL DATA



MOUNTING INSTRUCTIONS



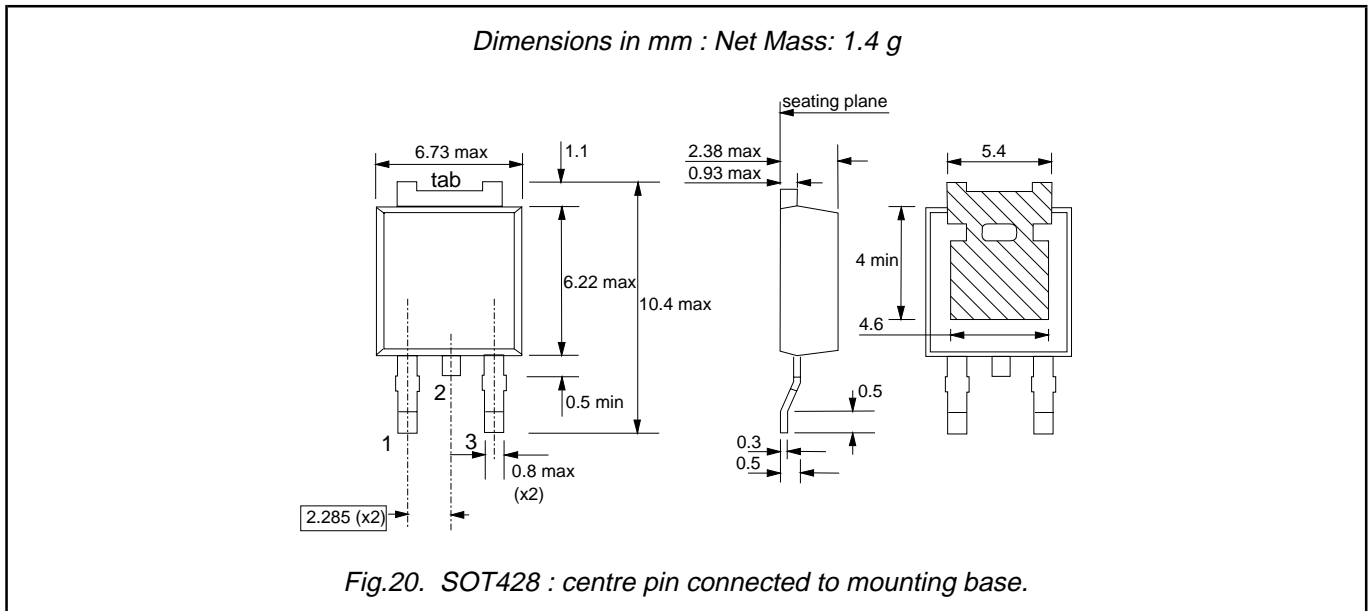
Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

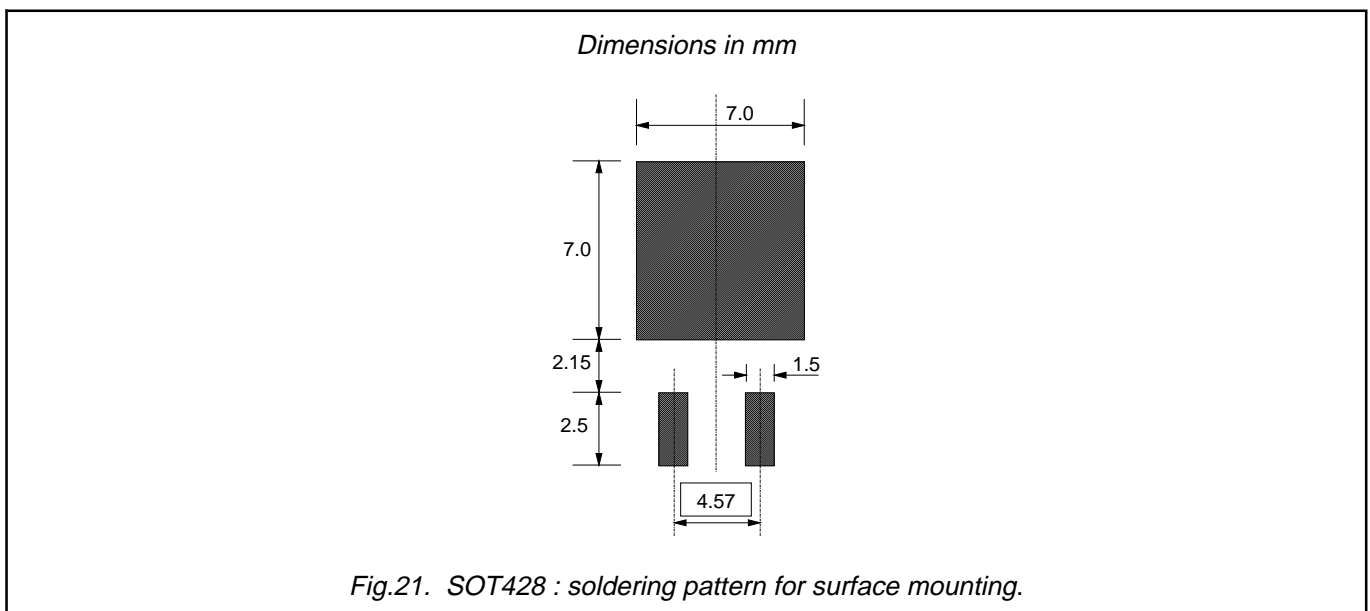
TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor
Logic level FET

PHP50N03LT, PHB50N03LT, PHD50N03LT

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1998	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.