

DATA SHEET

SA647 **Low-voltage digital IF receiver**

Product specification

1998 Aug 10

Low-voltage digital IF receiver

SA647

DESCRIPTION

The SA647 is a low-voltage high performance monolithic digital system with high-speed RSSI incorporating a mixer, oscillator with buffered output, two limiting intermediate frequency amplifiers, fast logarithmic received signal strength indicator (RSSI), voltage regulator, RSSI op amp and power down pin. The SA647 is available in TSSOP (thin shrink small outline package).

The SA647 was designed for portable digital communication applications and will function down to 2.7V. The limiter amplifier has differential outputs with 2MHz small signal bandwidth. The RSSI output has access to the feedback pin. This enables the designer to level adjust the outputs or add filtering.

FEATURES

- $V_{CC} = 2.7$ to $5.5V$
- Low power receiver ($5.3mA @ 3V$)
- Power down mode ($I_{CC} = 110\mu A$)
- Fast RSSI rise and fall times
- Extended RSSI range with temperature compensation
- RSSI op amp
- 2MHz limiter small signal bandwidth
- Filter matching ($1.5k\Omega$)
- Differential limiter output
- Oscillator buffer
- TSSOP-20 package

APPLICATIONS

- NADC (North American Digital Cellular)
- Digital receiver systems
- Cellular radio

PIN CONFIGURATION

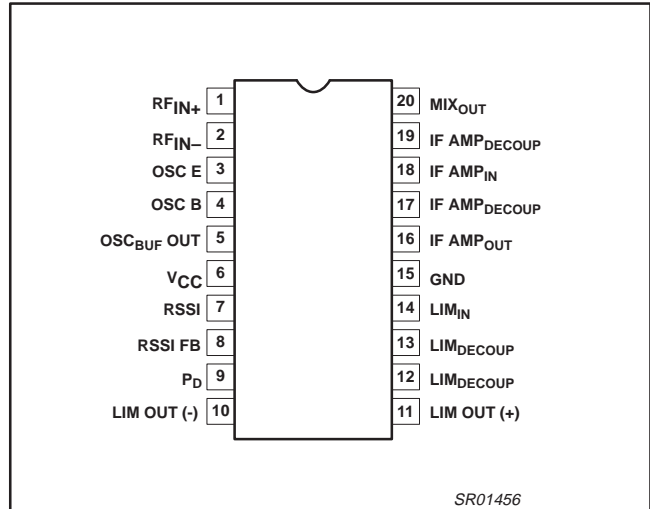


Figure 1. Pin Configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Thin Shrink Small Outline Package (Surface-mount)	-40 to +85°C	SA647DH	SOT360-1

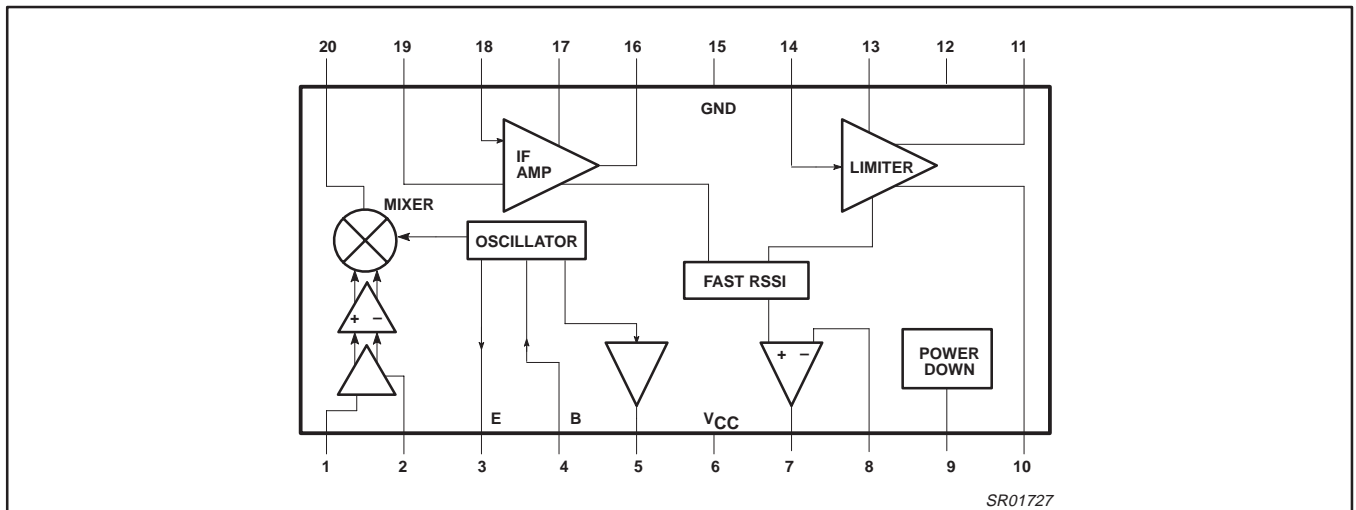


Figure 2. Block Diagram

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PIN DESCRIPTION

PIN NO.	SYMBOL	FUNCTION
1	RF _{IN}	RF input
2	RF BYPASS	RF bypass
3	OSC _E	Oscillator emitter
4	OSC _B	Oscillator base (input)
5	OSC _{BUF} OUT	Oscillator buffer output
6	V _{CC}	Supply voltage
7	RSSI	RSSI output
8	RSSI FB	RSSI Feedback
9	P _D	Power Down
10	LIM _{OUT(-)}	Limiter output (neg)
11	LIM _{OUT(+)}	Limiter output (pos)
12	LIM _{DECOUP}	Limiter decoupling
13	LIM _{DECOUP}	Limiter decoupling
14	LIM _{IN}	Limiter input
15	GND	Ground
16	IF AMP _{OUT}	IF amplifier output
17	IF AMP _{DECOUP}	IF amplifier decoupling
18	IF AMP _{IN}	IF amplifier input
19	IF AMP _{DECOUP}	IF amplifier decoupling
20	MIX _{OUT}	Mixer output

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	-0.3 to +6.0	V
V_{IN}	Voltage applied to any other pin	-0.3 to ($V_{CC} + 0.3$)	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range	-40 to +85	°C

NOTE: Thermal impedance (θ_{JA}) = 135°C/W

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +3.0V$, $T_A = 25^\circ C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.7		5.5	V
I_{CC}	DC current drain		4	5.3	7	mA
	Standby	Pin 9 = LOW		0.11		mA
	Input current	Pin 9 = LOW	-10		10	μA
		Pin 9 = HIGH	-10		10	
	Input level	Pin 9 = LOW	0		$0.3V_{CC}$	V
Pin 9 = HIGH		$0.7 V_{CC}$		V_{CC}		
τ_{on}	Power-up time	RSSI valid (10% to 90%)		10		μsec
τ_{off}	Power-down time	RSSI valid (90% to 10%)		5		μsec

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AC ELECTRICAL CHARACTERISTICS $V_{CC} = +3.0V$, Mixer input freq = 110.52MHz, LO input freq = 109.92MHz, $T_A = 25^{\circ}C$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Mixer/Osc section						
f_{IN}	Input signal frequency				200	MHz
f_{OSC}	Crystal oscillator frequency				200	MHz
NF	Noise figure at 110.52MHz	Matched input and output 50 Ω		4.5		dB
IIP3	Third-order input intercept point	Matched input and output to 50 Ω		-29.5		dBm
G_{CP}	Conversion power gain	Matched input and output to 50 Ω	17	20	23	dB
R_{IN}	Mixer input resistance	at 110.52 MHz		670		Ω
C_{IN}	Mixer input capacitance	at 110.52 MHz		3.0		pF
R_{OUT}	Mixer output resistance	at 600 kHz		1.5		k Ω
I_{SOL}	Mixer RF to LO isolation			32		dB
	Buffered LO output level, DC coupled	10k 3.9pF load	110	230	320	mV _{P-P}
	External input level	f = 110.52 MHz at Pin 4	250			mV _{P-P}
IF section						
	IF amp power gain	Matched input and output 50 Ω	30	36		dB
	Limiter power gain		51	60		dB
IF_{BW}	IF amp bandwidth			2		MHz
	RSSI output	Input power level = -113dBm, Pin 1		0.30		V
		Input power level = -68dBm, Pin 1		1.00		V
		Input power level = -29dBm, Pin 1		1.55		V
	RSSI range			85		dB
	RSSI accuracy			± 1.5		dB
	RSSI ripple			30		mV _{P-P}
	RSSI speed – (Rise Time) Input @ Pin 1	No filter		5		μs
	RSSI speed – (Fall time) Input @ Pin 1	No filter		25		μs
	IF input impedance			1.5		k Ω
	IF output impedance			1.5		k Ω
	Limiter input impedance			1.5		k Ω
	Limiter output impedance	(Pin 10, Pin 11)		230		Ω
	Limiter output (each pin)	Output load is 1.5K in parallel with 30 pF to GND each pin	240	350	420	mV _{P-P}
	Limiter output DC level			1.27		V
	Differential output matching			± 5		mV
	Limiter output offset			0.09		V

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CIRCUIT DESCRIPTION

Mixer

The mixer has a single-ended input. The input impedance is 670Ω in parallel with a 3.0pF cap at 110.52MHz RF. The mixer output can drive a 1500Ω ceramic filter without any matching required.

Oscillator and Buffer

The on-board oscillator supplies the signal for the mixer down-conversion. The internally biased transistor can be configured as a Colpitts or Butler overtone crystal oscillator. The transistor's bias current can be increased if desired by adding a shunt resistor from Pin 3 to ground. The oscillator's buffered output (Pin 5) can be used as a feedback signal to lock the oscillator to an appropriate reference.

IF Amplifier and IF Limiter

The IF strip provides more than 96dB of power gain for the down converted signal. Its bandwidth is 2MHz . The input and output impedance of the IF amplifier and the input impedance of the IF limiter are set to 1500Ω . A second filter is connected between the IF amplifier and the limiter for improved channel selectivity and reduced instability. The overall gain can be reduced if desired by adding an external attenuator after the IF amplifier. The differential limiter outputs (Pins 10 and 11) are available for demodulator circuits.

RSSI

The received signal strength indicator provides a linear voltage indication of the received signal strength in dB for a typical range of 85dB . The response time to a change in input signal is less than a few microseconds and the delay is kept to a minimum because of the use of a minimum phase shift circuit. Because of the speed of the RSSI circuit, the RSSI rise and fall time will be dominated by the bandwidth of the external bandpass filter that is placed between the mixer and the IF. Since the RSSI function requires the signal to propagate through the whole IF strip, and the rise and fall time of the filters are inversely proportional to their bandwidth, there is a trade-off between channel selectivity and RSSI response. Therefore, it is recommended that all channel selection filters be placed before the IF strip, just after the mixer. This will make the delay of the RSSI independent of the mixer input signal amplitude. Also, a 6dB insertion loss between the IF and limiter sections (Pins 16 and 14) will give optimum flatness of RSSI versus mixer input signal.

The RSSI curve is temperature compensated and in addition is designed for improved consistency from unit to unit.

DC Power Supply

The IC is designed for operation between 2.7 and 5.5V . A power supply dependent biasing scheme is used in the mixers to benefit from the large headroom available at higher V_{CCS} .

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PERFORMANCE CHARACTERISTICS

$V_{CC} = +3.0V$, Mixer input freq = 110.52MHz, LO input freq = 109.92MHz, $T_A = 25^{\circ}C$; unless otherwise stated.

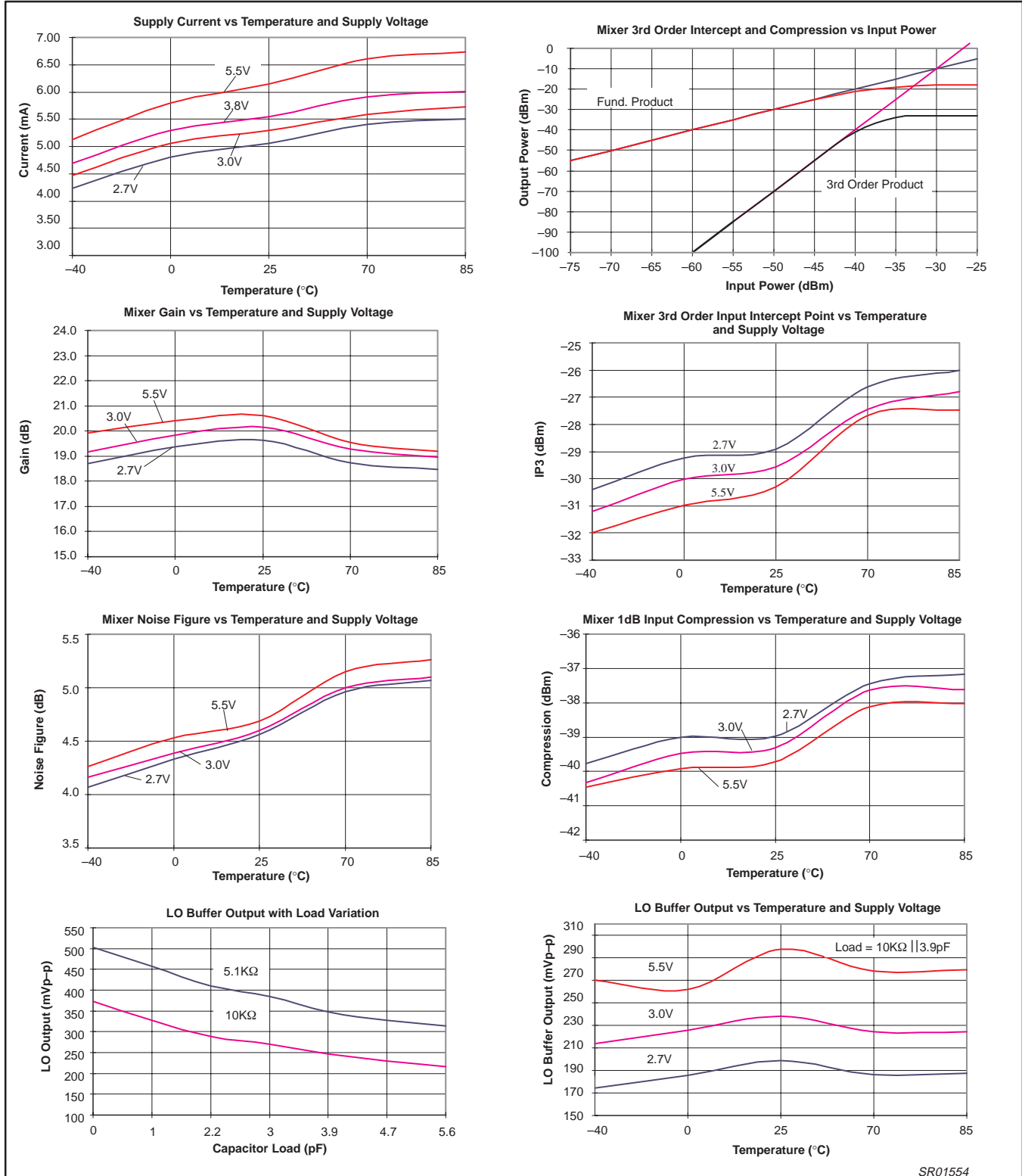
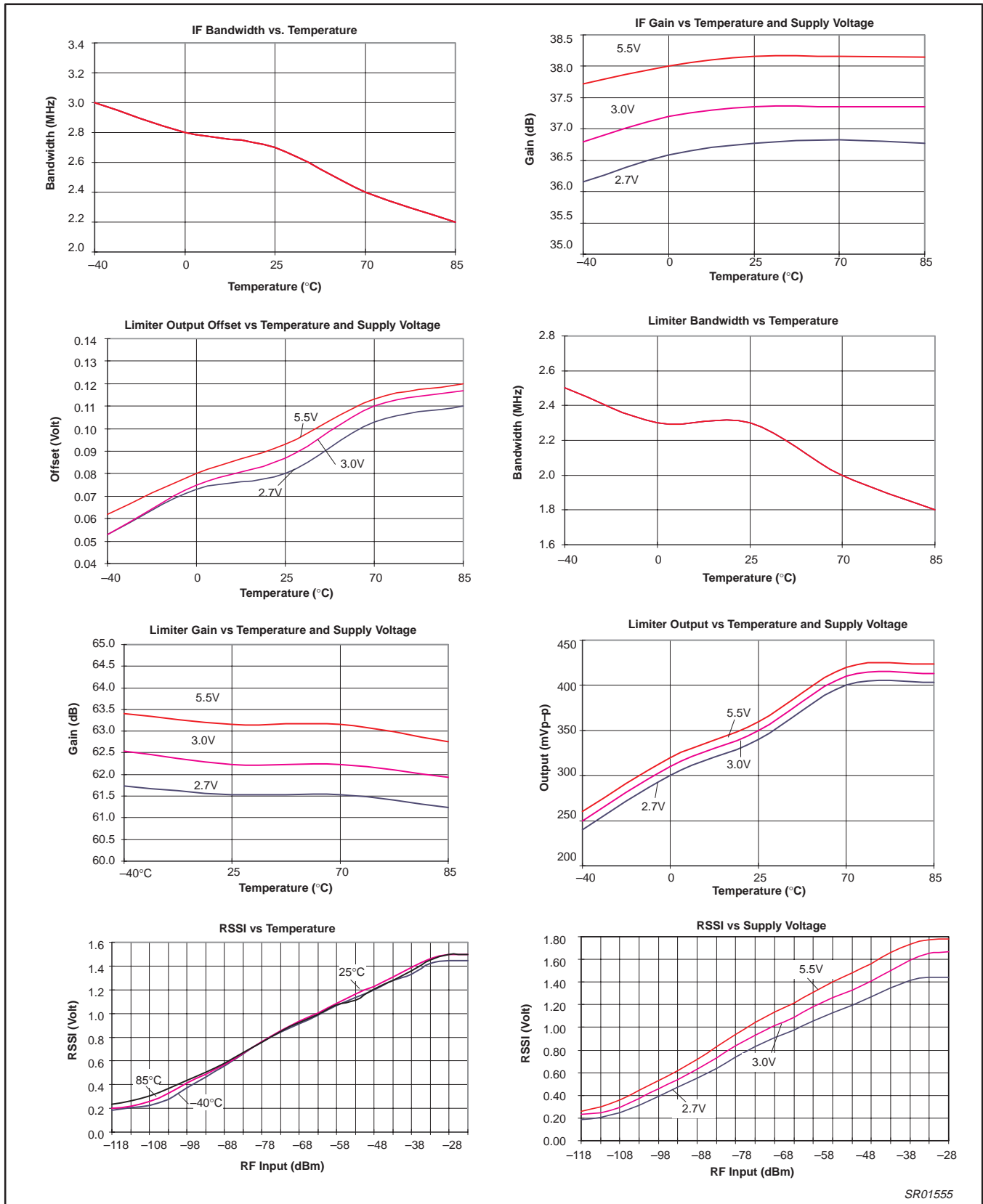


Figure 3.

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SR01555

Figure 4.

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GENERAL TEST CIRCUIT DESCRIPTION

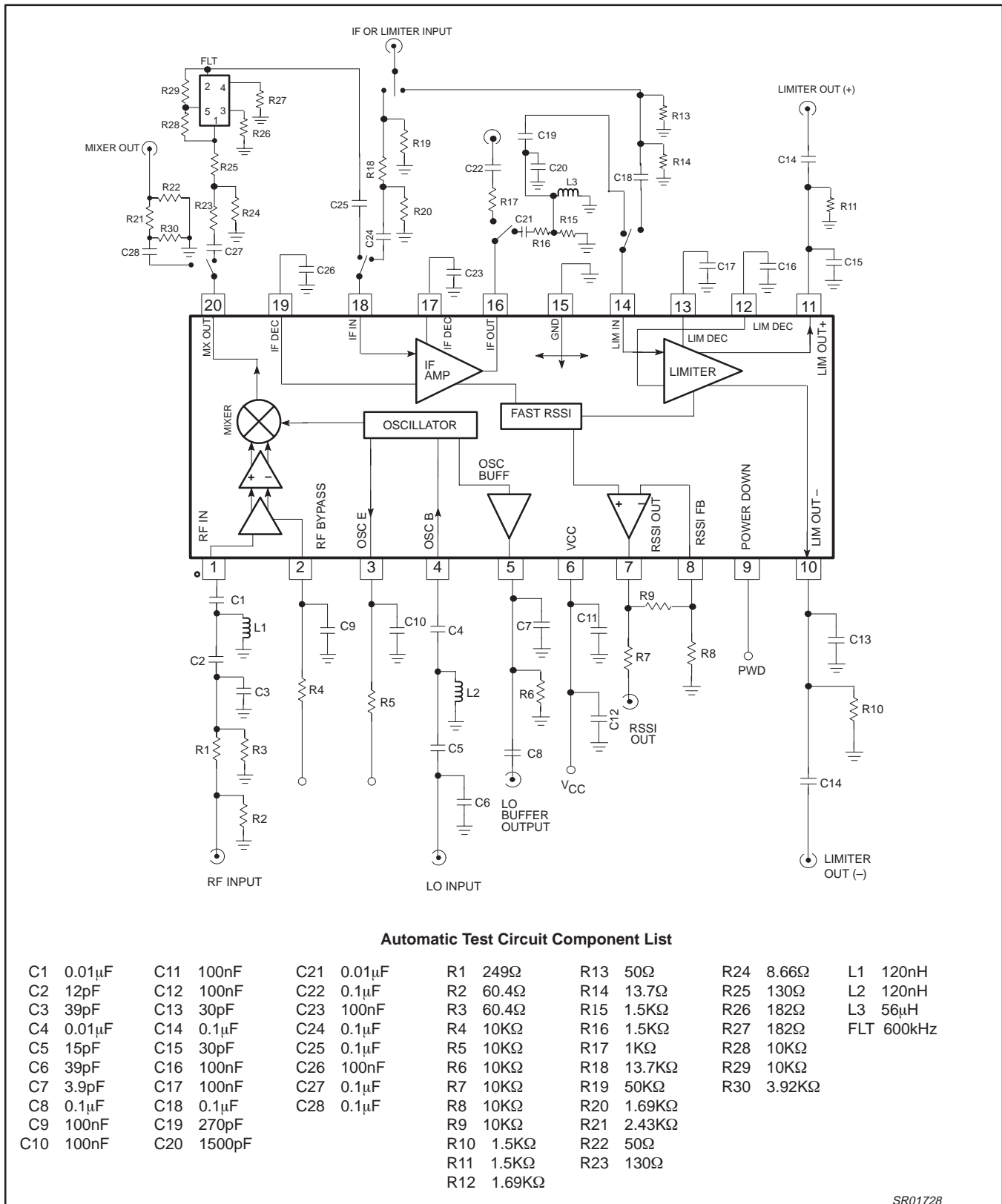


Figure 5.

SR01728

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PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
1	RF IN	+2.35		6	V _{CC}	+3.00	
2	RF BYPASS	+1.56			7	RSSI OUT	+0.20
3	OSC E	+2.21		8	RSSI FEEDBACK	+0.20	
4	OSC B	+2.78			9	POWER DOWN	+2.00
5	OSC BUFFER	+2.21					

SR01729

Figure 6.

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PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT	PIN No.	PIN MNEMONIC	DC V	EQUIVALENT CIRCUIT
10 11	LIMITER OUT	+1.25		16	IF AMP OUT	+1.28	
12	LIMITER DECOUP	+1.28		17	IF AMP DECOUP	+1.28	
13	LIMITER COUPLING	+1.28		18	IF AMP IN	+1.28	
14	LIMITER IN	+1.28		19	IF AMP DECOUP	+1.28	
15	GND	0		20	MIXER OUT	+2.03	

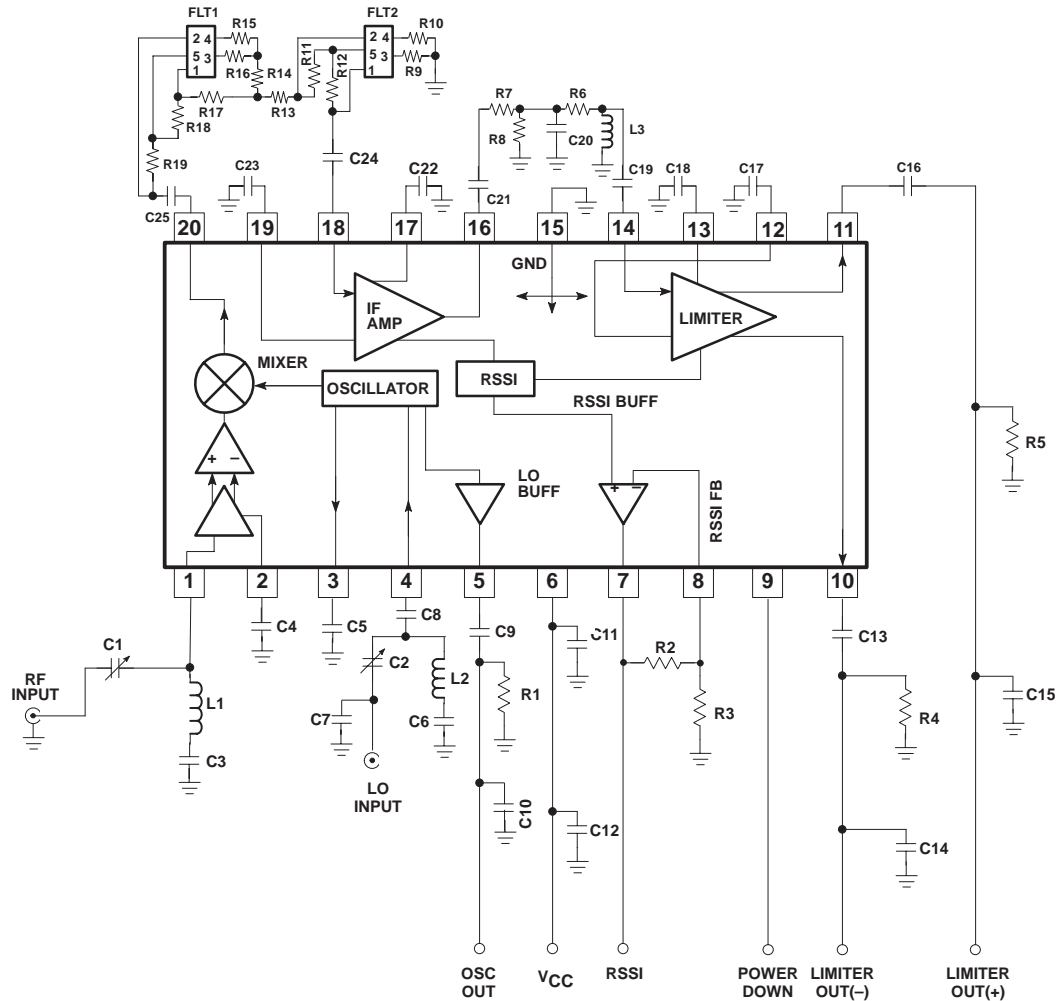
SR00509

Figure 7.

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GENERAL APPLICATIONS CIRCUIT



Component List

C1	5–30pF	C11	0.1μF	C21	10nF	R1	10KΩ	R13	240Ω	L1	180nH
C2	5–30pF	C12	6.8pF	C22	0.1μF	R2	0Ω (short)	R14	4.5KΩ	L2	180nH
C3	0.1μF	C13	0.1μF	C23	0.1μF	R3	OPEN	R15	180Ω	L3	56μH
C4	0.1μF	C14	30pF	C24	10nF	R4	5.1k	R16	180Ω	FLT1,2	600kHz
C5	0.1μF	C15	30pF	C25	10nF	R5	5.1k	R17	240Ω		
C6	0.1μF	C16	0.1μF			R6	0Ω (short)	R18	10KΩ		
C7	47pF	C17	0.1μF			R7	1.5KΩ	R19	10KΩ		
C8	1nF	C18	0.1μF			R8	1.5KΩ				
C9	10pF	C19	10nF			R9	180Ω				
C10	3.9pF	C20	1500pF			R10	180Ω				
						R11	10KΩ				
						R12	0KΩ				

NOTE: R2 and R3 set the RSSI buffer gain. For unity gain short R2 (Pin 7 to Pin 8) and leave R9 open.

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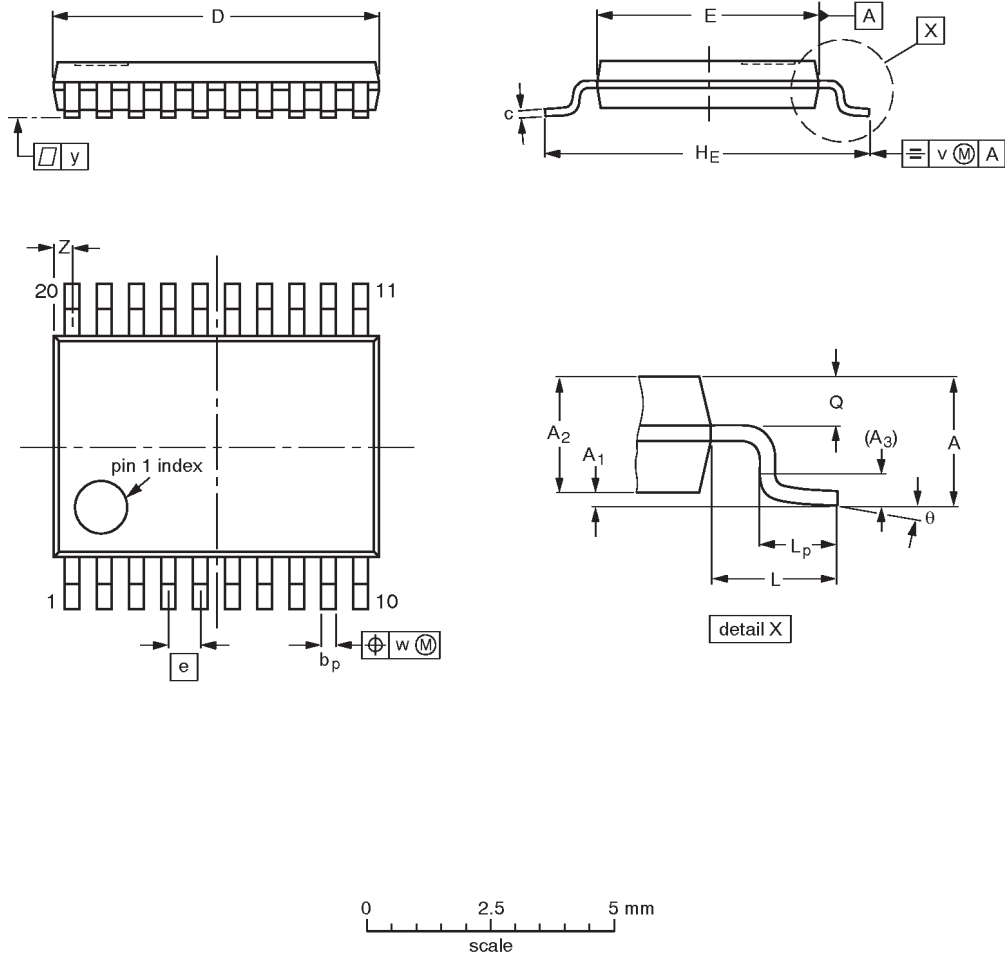
Figure 8.

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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