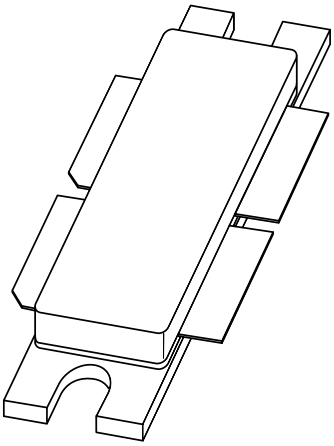
DISCRETE SEMICONDUCTORS

DATA SHEET



BLF2048
UHF push-pull power LDMOS transistor

Preliminary specification 1999 Nov 23

Philips Semiconductors

PHILIPS

UHF push-pull power LDMOS transistor — BLF2048

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 2.2 GHz).

APPLICATIONS

- Common source class-AB operation for PCN and PCS applications in the 1800 to 2200 MHz frequency range.

DESCRIPTION

Push-pull silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 4-lead flange package (SOT539A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT539A

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source connected to flange

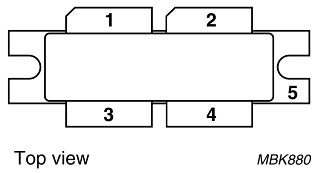


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
class-AB (2-tone)	f_1 = 2200; f_2 = 2200.1	26	120 (PEP)	>10	>30	≤–26
		28	140 (PEP)	typ. 11.2	typ. 31	typ. –25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	65	V
V_{GS}	gate-source voltage		–	±15	V
I_D	drain current (DC)		–	18	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_L = 120 W; T_{mb} = 50 °C, note 1	0.35	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink		0.15	K/W

Note

1. Thermal resistance is determined under nominal 2-tone RF operating conditions.

CHARACTERISTICS

T_j = 25 °C; per section; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 9 V; V_{DS} = 10 V	18	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	–	4	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 9 V; I_D = 5 A	–	0.17	–	Ω
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	3.4	–	pF

Notes

1. Capacitance of die only.

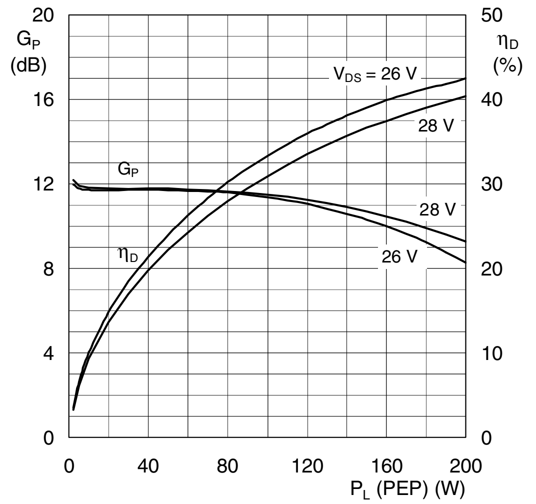
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 0.5 K/W; unless otherwise specified..

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
class-AB (2-tone)	f_1 = 2200; f_2 = 2200.1	26	2 x 400	120 (PEP)	>10	>30	≤–26
		28	2 x 400	140 (PEP)	typ. 11.2	typ. 31	typ. –25

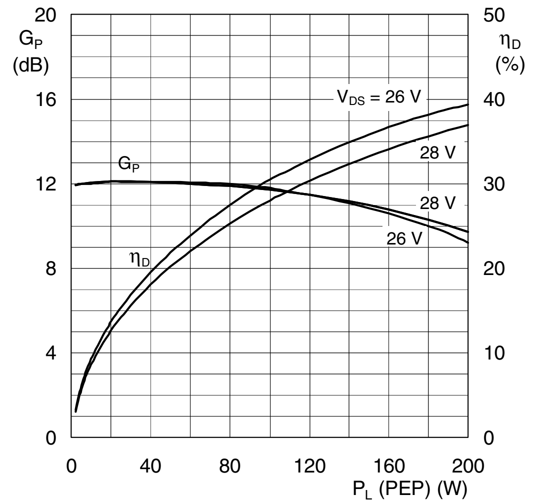
Ruggedness in class-AB operation

The BLF2048 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 2200 MHz, P_L = 120 W (CW).



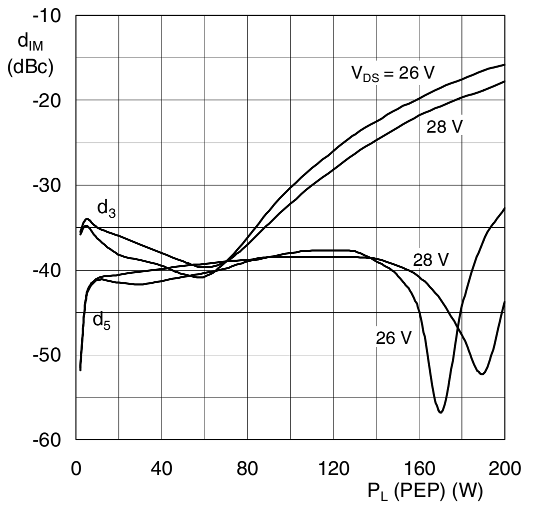
f_1 = 2000 MHz; f_2 = 2000.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.2 Power gain and drain efficiency as functions of peak envelope load power; typical values.



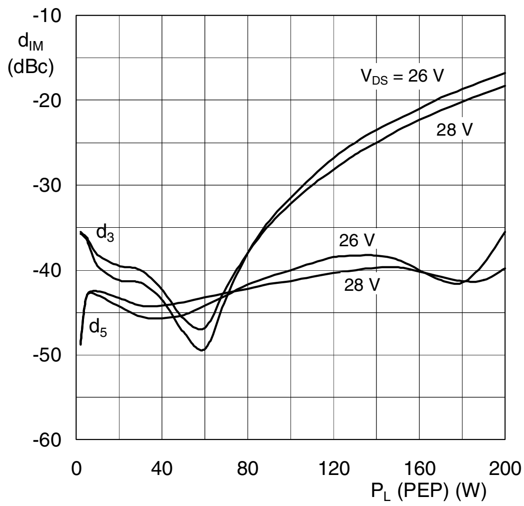
f_1 = 2200 MHz; f_2 = 2200.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.3 Power gain and drain efficiency as functions of peak envelope load power; typical values.



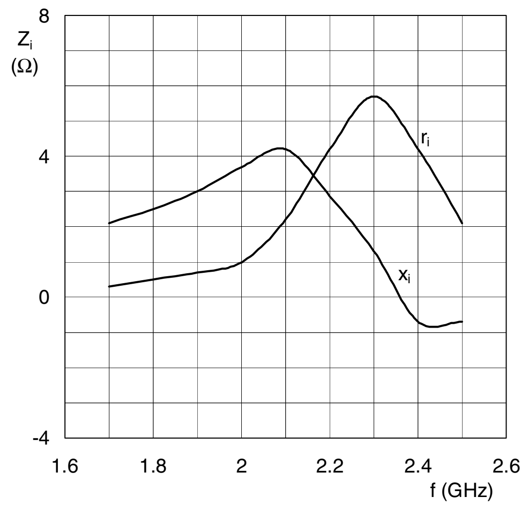
f_1 = 2000 MHz; f_2 = 2000.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



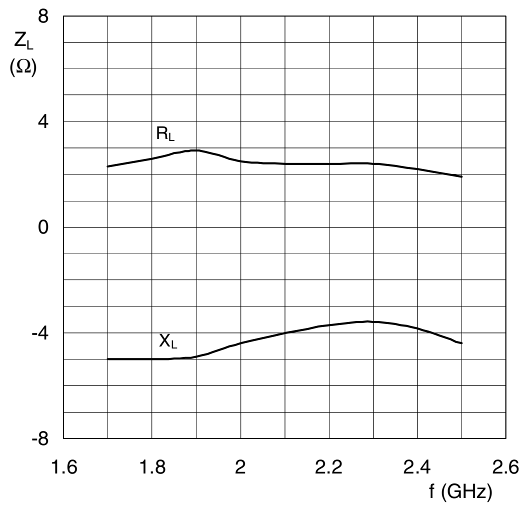
f_1 = 2200 MHz; f_2 = 2200.1 MHz;
I_{DQ} = 2 x 400 mA; $T_h \leq 25$ °C.

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 2 x 400 mA; P_L = 160 W (total device); $T_h \leq 25$ °C.

Fig.6 Input impedance per section as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 2 x 400 mA; P_L = 160 W (total device); $T_h \leq 25$ °C.

Fig.7 Load impedance per section as a function of frequency (series components); typical values.

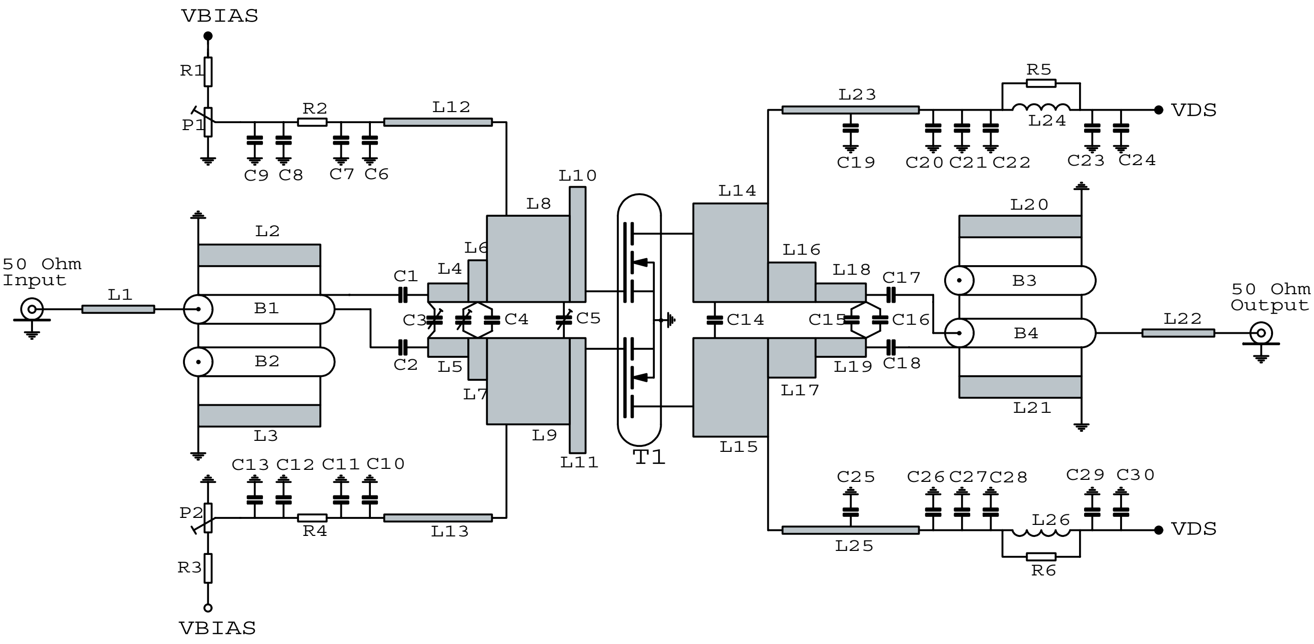


Fig.8 Testcircuit for 2.2 GHz.

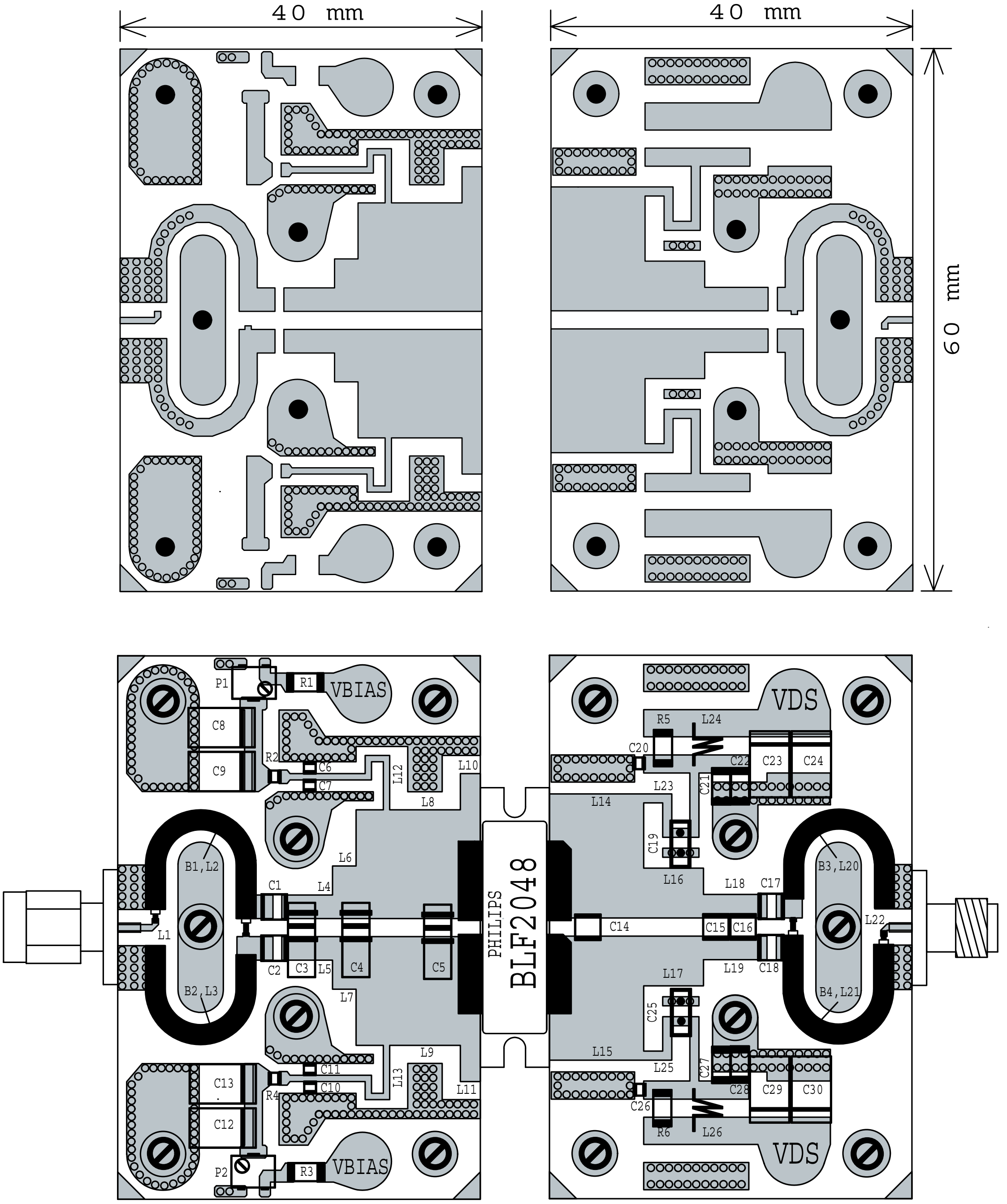
List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	5.1 pF		
C3, C5	Tekelec variable capacitor	0.6 to 4.5 pF		
C4	Tekelec variable capacitor + multilayer ceramic chip capacitor; note 1	0.6 to 4.5 pF + 2.4 pF		
C6, C10	multilayer ceramic chip capacitor; note 2	100 pF		
C7, C11	multilayer ceramic chip capacitor; note 2	18 pF		
C8, C12, C23, C29	tantal SMD capacitor	4.7 μF; 35 V		
C9, C13, C24, C30	tantal SMD capacitor	10 μF; 35 V		
C14	multilayer ceramic chip capacitor; note 3	0.5 pF		
C15	multilayer ceramic chip capacitor; note 3	1 pF		
C16	multilayer ceramic chip capacitor; note 1	1.5 pF		
C17, C18	multilayer ceramic chip capacitor; note 1	10 pF		
C19, C25	MKT ceramic chip capacitor	33 nF		2222 370 11333
C20, C26	multilayer ceramic chip capacitor; note 2	6.2 pF		
C21, C27	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C22, C28	multilayer ceramic chip capacitor; note 1	8.2 pF		

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
L1	stripline; note 4	47 Ω	4.5 × 1 mm	
L2, L3, L20, L21	stripline; note 4		15 × 2 mm	
L4, L5	stripline; note 4		5.6 × 2.6 mm	
L6, L7	stripline; note 4		2.6 × 5.8 mm	
L8, L9	stripline; note 4		11.5 × 12 mm	
L10, L11	stripline; note 4		2.2 × 16 mm	
L12, L13	stripline; note 4	57 Ω	1/4 λ @ 2.2 GHz	
L14, L15	stripline; note 4		10.4 × 13.7 mm	
L16, L17	stripline; note 4		6.6 × 5.5 mm	
L18, L19	stripline; note 4		7 × 2.6 mm	
L22	stripline; note 4	47 Ω	4 x 1 mm	
L23, L25	stripline; note 4	47 Ω	1/4 λ @ 2.2 GHz	
L24, L26	1 turn enamelled 0.7 mm copper wire		int.dia. 7 mm; length ...... mm	
B1, B4	balun of semi-rigid cable	50 Ω		
B2, B3	semi-rigid cable; note 5	50 Ω		
R1, R3, R5, R6	metal film resistor	5.6 Ω, 0.6 W		
R2, R4	metal film resistor	10 Ω, 0.6 W		
P1, P2	variable resistor (multiturn)	5 kΩ		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. American Technical Ceramics type 100A or capacitor of same quality.
3. American Technical Ceramics type 180R or capacitor of same quality.
4. Semi-rigid cable soldered along the stub to establish balance.
5. The striplines are on a double copper-clad PCB with Teflon dielectric (εr = 6.15); thickness 0.64 mm.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15), thickness 0.64 mm.

The other side is unetched and serves as a ground plane.

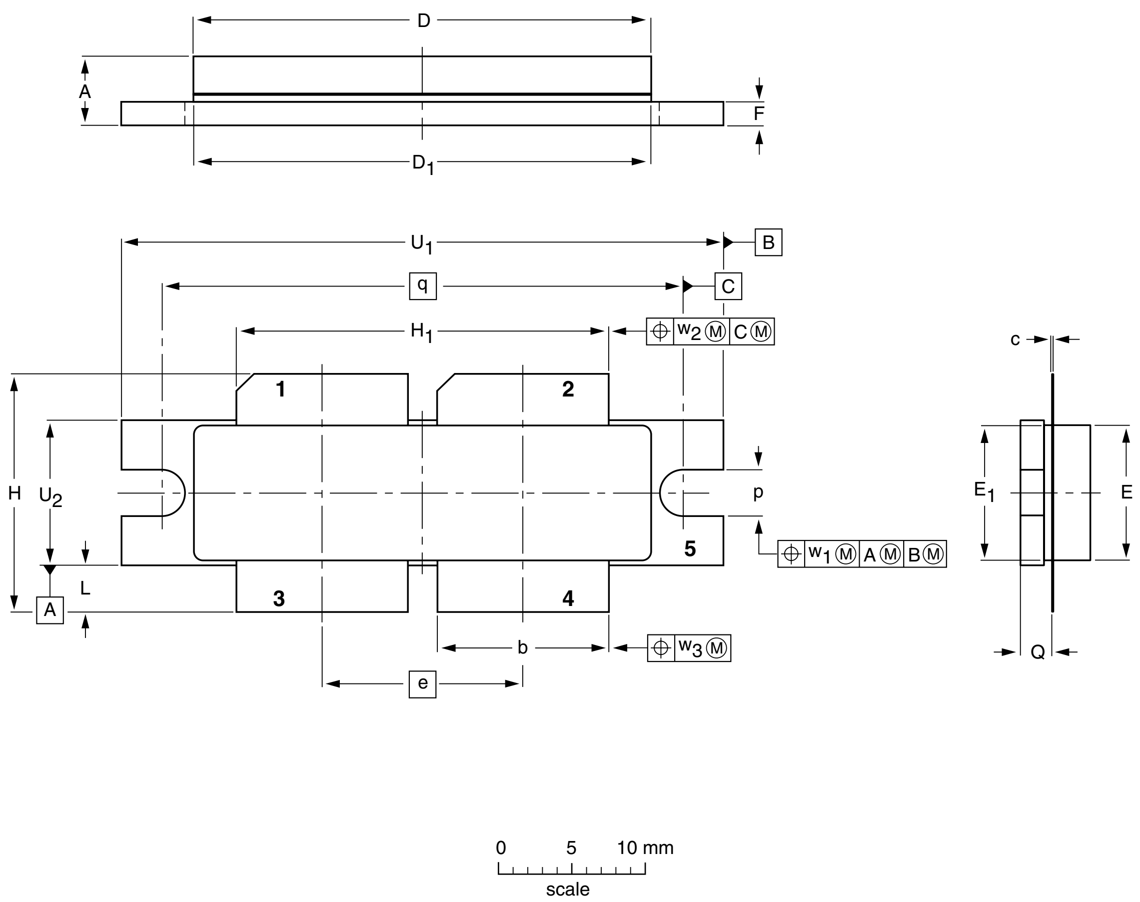
Fig.9 Component layout for 2.2 GHz class-AB testcircuit.

PACKAGE OUTLINE

Flanged balanced LDMOST package; 2 mounting holes; 4 leads **SOT539A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.33 3.96	11.81 11.56	0.15 0.08	31.55 30.94	31.65 30.96	13.72	9.50 9.20	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.73 2.72	3.30 3.05	2.31 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.210 0.156	0.465 0.455	0.006 0.003	1.242 1.218	1.246 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.147 0.107	0.130 0.120	0.091 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~99-05-10~~ 99-06-25

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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