

DATA SHEET

NE83C92

Low-power coaxial Ethernet transceiver

Product specification

1995 May 01

IC19 Data Handbook

Low-power coaxial Ethernet transceiver

NE83C92

DESCRIPTION

The NE83C92 is a low power BiCMOS coaxial transceiver interface (CTI) for Ethernet (10base5) and Thin Ethernet (10base2) local area networks. The CTI is connected between the coaxial cable and the Data Terminal Equipment (DTE) and consists of a receiver, transmitter, receive-mode collision detector, heartbeat generator and jabber timer (see Block Diagram). The transmitter output connects directly to a doubly terminated 50Ω cable, while the receiver output, collision detector output and transmitter input are connected to the DTE through isolation transformers. Isolation between the CTI and the DTE is an IEEE 802.3 requirement that can be met on signal lines by using a set of pulse transformers. Power isolation for the CTI is achieved using DC-to-DC conversion through a power transformer.

The part is fully pin compatible with the industry standard 8392, but has substantially lower current consumption, is fully compliant with the IEEE802.3 standard, and has additional features such as automatic selection between AUI and coaxial connections, and requires no external pull-down resistors for local integrated MAU application.

The NE83C92 is manufactured on an advanced BiCMOS process and is available with PLCC package which make it ideally suited to lap-top personal computers or systems where low power consumption, limited board space and jumperless design is required. Refer to selection flow chart for optimal application.

FEATURES

- Fully compliant with Ethernet II, IEEE 802.3 10BASE-5 and 10BASE-2, and ISO 8802/3 interface specifications
- 100% drop-in compatible with industry standard 8392 sockets
- Optimal implementation can use 1 Watt DC-DC converter and reduces external part count (local/integrated MAU requires no external pull-down resistors).
- High efficiency AUI drivers automatically power-down under idle conditions to minimize current consumption
- Automatically disabling AUI drivers when disconnecting coax cable, allowing hardwiring of AUI connection and local/integrated CTI connection
- Smart squelch on data inputs eliminates false activations
- Advanced BiCMOS process for extremely low power operation

PIN CONFIGURATION

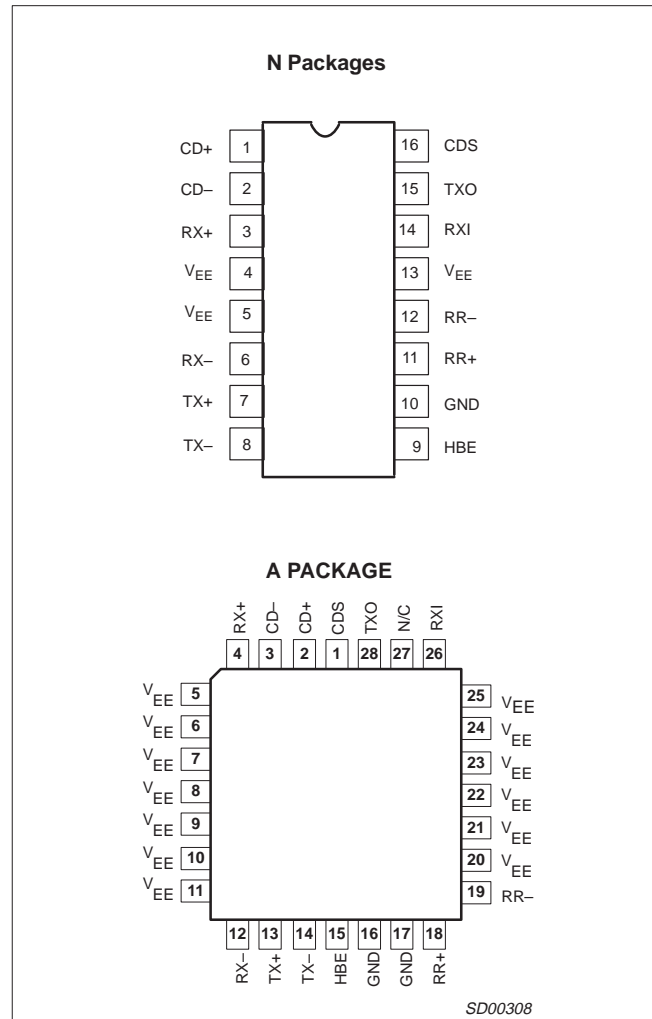


Figure 1. Pin Configurations

- Available in 16-pin DIP, and 28-pin PLCC packages
- Expanded version (NE83Q93) with 5 LED status drivers is available for repeater and advanced system applications
- Full ESD protection
- Power-on reset prevents glitches on coaxial cable during power-up

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package	0 to +70°C	NE83C92N	SOT38-4
28-Pin Plastic Leaded Chip Carrier	0 to +70°C	NE83C92A	SOT261-3

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PIN DESCRIPTIONS

PIN NO. N PKG	PIN NO. PLCC	SYMBOL	DESCRIPTION
1 2	2 3	CD+ CD-	Collision Outputs. Balanced differential line driver outputs which send a 10MHz signal to the DTE in the event of a collision, jabber interrupt or heartbeat test. External pull-down resistors are optional with local/integrated MAU application.
3 6	4 12	RX+ RX-	Receiver Outputs. Balanced differential line driver outputs which send the received signal to the DTE. External pull-down resistors are optional with local/integrated MAU application.
7 8	13 14	TX+ TX-	Transmitter Inputs. Balanced differential line receiver inputs which accept the transmission signal from the DTE and apply it to the coaxial cable at TXO, once it meets Tx squelch threshold.
9	15	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to V_{EE} and enabled when connected to GND or left floating.
11 12	18 19	RR+ RR-	External Resistor. A 1k Ω (1%) resistor connected between these pins establishes the signaling current at TXO.
14	26	RXI	Receiver Input. This pin is connected directly to the coaxial cable. Received signals are equalized, amplified, and sent to the DTE through the RX \pm pins, once it meets Rx squelch threshold.
15	28	TXO	Transmitter Output. This pin is connected directly (Thin Ethernet) or through an external isolating diode (Ethernet) to the coaxial cable.
16	1	CDS	Collision Detect Sense. Ground sense connection for the collision detection circuitry. This pin should be connected directly to the coaxial cable shield for standard Ethernet operation.
10	16 17	GND	Positive Supply Pin.
4 5 13	5 to 11 20 to 25	V_{EE}	Negative Supply Pins.

NOTE:

- The IEEE 802.3 name for CD is CI; for RX is DI; for TX is DO.

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BLOCK DIAGRAM

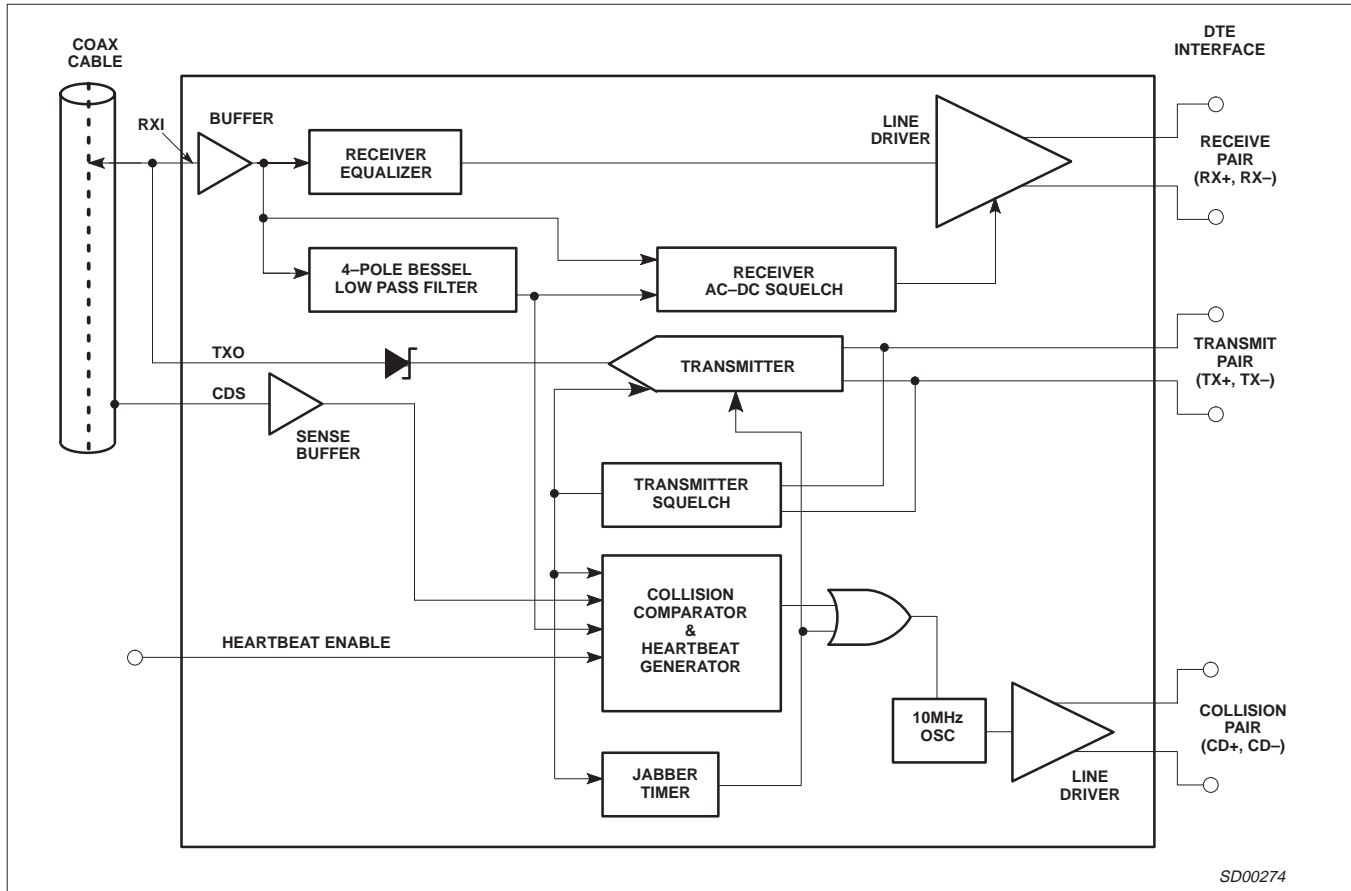


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{EE}	Supply voltage ¹	-12	V
V _{IN}	Voltage at any input ¹	0 to -12	V
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10sec.)	+300	°C
T _J	Recommended max junction temperature ²	+150	°C
θ _{JA}	Thermal impedance (N and A packages)	60	°C/W

NOTE:

- 100% measured in production.
- The junction temperature is calculated from the following expression:

$$T_J = T_A + \theta_{JA} [(V_{EE} \times 0.015 \times n_{IDL}) + (V_{EE} \times 0.018 \times n_{RX}) + (V_{EE} \times 0.066 \times n_{TX})]$$
 where
 T_A = Ambient temperature in °C.
 θ_{JA} = Thermal resistance of package.
 V_{EE} = Normal operating supply voltage in volts.
 n_{IDL} = Percentage of duty cycle idle
 n_{RX} = Percentage of duty cycle receiving
 n_{TX} = Percentage of duty cycle transmitting

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ELECTRICAL CHARACTERISTICS $V_{EE} = -9V \pm 6\%$; $T_A = 0^\circ C$ to $+70^\circ C$ unless otherwise specified^{1,2}. No external isolation

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
V_{UVL}	Under voltage lockout. Transceiver disabled for $ V_{EE} < V_{UVL} $			-7.5		V
I_{EE}	Supply current idle			-15	-20	mA
	Supply current transmitting (without collision)	Without external pull-down resistors		-70	-85	mA
I_{RXI}	Receive input bias current	$V_{RXI} = 0V$	-2		+25	μA
I_{CDS}	Cable sense input bias current	$V_{CDS} = 0V$		+1	+3	μA
V_{IH}	HBE input HIGH voltage		$V_{EE} + 2.4$			V
V_{IL}	HBE input LOW voltage				$V_{EE} + 1.6$	V
I_{IH}	HBE input HIGH current	$V_{HBE} = 0V$			+10	μA
I_{IL}	HBE input LOW current	$V_{HBE} = V_{EE}$	-30			μA
I_{TDC}	Transmit output DC current level ³		-37		-45	mA
I_{TAC}	Transmit output AC current level ³		± 28		$\pm I_{TDC}$	mA
I_{TX10}	Transmit current	$V_{TXO} = -10V$	-250		+250	μA
V_{TCOM}	Transmitter output voltage compliance ⁴				-3.7	V
V_{CD}	Collision threshold ⁵	Measured by applying DC voltage at RXI (CDS = 0V)	-1450	-1530	-1580	mV
V_{DIS}	AUI disable voltage at RXI	Measured as DC voltage at RXI		-3.5		V
V_{OD}	Differential output voltage – non idle at RX_{\pm} and CD_{\pm} ⁶		± 600		± 1100	mV
V_{OB}	Differential output voltage imbalance – idle at RX_{\pm} and CD_{\pm} ⁷				± 40	mV
V_{OC}	Output common mode voltage at RX_{\pm} and CD_{\pm}	$RXI = 0V$	-4.0	-5.5	-7.0	V
V_{RS}	Receiver squelch threshold	V_{RXI} average DC (CDS = 0V)	-150	-250	-350	mV
V_{TS}	Transmitter squelch threshold	$(V_{TX+} - V_{TX-})$ peak	-175	-225	-275	mV
R_{RXI}	Shunt resistance at RXI non-transmitting		100			k Ω
C_{RXI}	Input capacitance at RXI ⁸			1	2	pF
R_{TXO}	Shunt resistance at TXO transmitting		7.5	10		k Ω
R_{AUIZ}	Differential impedance at RX_{\pm} and CD_{\pm} with no coaxial cable connected			6		k Ω
R_{TX}	Differential impedance at TX_{\pm}			20		k Ω

NOTES:

1. Currents flowing into device pins are positive. All voltages are referenced to ground unless otherwise specified. For ease of interpretation, the parameter limit that appears in the MAX column is the largest value of the parameter, irrespective of sign. Similarly, the value in the MIN column is the smallest value of the parameter, irrespective of sign.
2. All typicals are for $V_{EE} = -9V$ and $T_A = 27^\circ C$.
3. I_{TDC} is measured as $(V_{MAX} + V_{MIN}) / (2 \times 25)$ where V_{MAX} and V_{MIN} are the max and min voltages at TXO with a 25 Ω load between TXO and GND. I_{TAC} is measured as $(V_{MAX} - V_{MIN}) / (2 \times 25)$.
4. The TXO pin shall continue to sink at least I_{TDC} min when the idle (no signal) voltage on this pin is -3.7V.
5. Collision threshold for an AC signal is within 5% of V_{CD} .
6. Measured on secondary side of isolation transformer. The transformer has a 1:1 turns ratio with an inductance between 30 and 100 μH at 5MHz.
7. Measured as the voltage difference between the RX pins or the CD pins with the transformer removed.
8. Not 100% tested in production.

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TIMING CHARACTERISTICS

$V_{EE} = -9V \pm 6\%$; $T_A = 0$ to 70°C , unless otherwise specified¹. No external isolation diode on TXO.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{RON}	Receiver start up delay RXI to RX \pm (Figure 5) First received bit on RX \pm	$V_{RXI} = -2V$ peak		3	5	bits
	First validly timed bit on RX \pm				$t_{RON} + 2$	bits
t_{RD}	Receiver prop. delay RXI to RX \pm	$V_{RXI} = -2V$ peak		20	50	ns
t_{RR}	Differential output rise time on RX \pm and CD \pm ^{2,3}			5	7	ns
t_{RF}	Differential output fall time on RX \pm and CD \pm ^{2,3}			5	7	ns
t_{OS}	Differential output settling time on RX \pm and CD \pm to $V_{OB} = 40mV^2$ (see Figure 6)			1		μs
t_{RJ}	Receiver and cable total jitter			± 2	± 6	ns
t_{RHI}	Receiver high to idle time	Measured to +210mV	200		850	ns
t_{RM}	Rise and fall time matching on RX \pm and CD \pm	$t_{RF} - t_{RR}$		0.1	± 2	ns
t_{TST}	Transmitter start-up delay TX \pm to TXO (Figure 7) First transmitted bit on TXO	$V_{TX\pm} = -1V$ peak		1	2	bits
	First validly timed bit				$t_{TST} + 2$	bits
t_{TD}	Transmitter prop delay TX \pm to TXO (see Figure 7)	$V_{TX\pm} = 1V$ peak	5	20	50	ns
t_{TR}	Transmitter rise time 10% to 90% (see Figure 7)		20	25	30	ns
t_{TF}	Transmitter fall time 10% to 90% (see Figure 7)		20	25	30	ns
t_{TM}	$t_{TF} - t_{TR}$ mismatch ⁵			0	± 2	ns
t_{TS}	Transmitter added skew ^{4,5}			0	± 2	ns
t_{TON}	Transmitter turn on pulse width (see Figure 7)	$V_{TX\pm} = 1V$ peak	10		35	ns
t_{TOFF}	Transmitter turn off pulse width (see Figure 7)	$V_{TX\pm} = 1V$ peak	125		200	ns
t_{CON}	Collision turn on delay (see Figure 8)	0V to -2V step at RXI			13	bits
t_{COFF}	Collision turn off delay (see Figure 8)	-2V to 0V step at RXI			16	bits
t_{CHI}	Collision high to idle time (see Figure 8)	Measured to +210mV	200		850	ns
f_{CD}	Collision frequency (see Figure 8)		8.5	10	11.5	MHz
t_{CP}	Collision signal pulse width (see Figure 8)		35		70	ns
t_{HON}	Heartbeat turn on delay (see Figure 9)		0.6		1.6	μs
t_{HW}	Heartbeat test duration (see Figure 9)		0.5		1.5	μs
t_{JA}	Jabber activation delay measured from TX \pm to CD \pm (see Figure 10)		20		60	ms
t_{JR}	Jabber reset delay measured from TX \pm to CD \pm (see Figure 10)		250		650	ms

NOTES:

- All typicals are for $V_{EE} = -9V$ and $T_A = 27^\circ\text{C}$.
- Measured on secondary side of isolation transformer (see Figure 4). The transformer has a 1:1 turn ratio with an inductance between 30 and $100\mu\text{H}$ at 5MHz.
- The rise and fall times are measured as the time required for the differential voltage to change from -225mV to $+225\text{mV}$, or $+225\text{mV}$ to -225mV , respectively.
- Difference in propagation delay between rising and falling edges at TXO.
- Not 100% tested in production.

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FUNCTIONAL DESCRIPTION

The NE83C92 is a low power BiCMOS coaxial Ethernet transceiver which complies with the IEEE 802.3 specification and offers the following features:

1. Low current consumption of typically 15mA when idling and 70mA while transmitting and no collision allows smaller DC-DC converter to be used for the isolated power supply. (No external pull-down resistors.)
2. Automatic selection of the AUI connector (for remote MAU) instead of the direct local (Thin) coaxial connection is possible by automatically placing the AUI drivers in high-impedance state when the local coaxial cable is disconnected. This eliminates the need for changing a jumper position on the Ethernet board when selecting either one of the connections. (Automatic selection of the local (Thin) connection is done by disconnecting the AUI cable and reconnecting the local coaxial one, which allows the NE83C92 to automatically activate itself.)
3. High-efficiency AUI drivers for the RX \pm and CD \pm ports automatically power down when idling and are powered up when a receive signal is detected. This is very important/useful for power sensitive applications such as lap-top computers or PCMCIA cards.
4. The NE83C92 advanced AUI driver (RX \pm and CD \pm) design does require external pull-down resistors (500 Ω) to drive a terminated (78 Ω) AUI cable. However, these drivers will operate correctly without the external resistors for integrated/local MAU applications where no AUI cable is used. Hence, they can be retro-fitted into existing 8392 designs with or without external pull-down resistors depending on the application. An extra current of 7mA/output (for 500 Ω resistors) would be generated, by these resistors, regardless of whether the transceiver is idle or responding to traffic.

Receiver Functions

The receiver consists of an input buffer, a cable equalizer, a 4-pole Bessel low pass filter, a squelch circuit and a differential line driver.

The buffer provides high input resistance and low input capacitance to minimize loading and reflections on the coaxial cable.

The equalizer is a high pass filter that compensates for the low pass effect of the coaxial cable and results in a flatband response over all signal frequencies to minimize signal distortion.

The 4-pole Bessel low pass filter extracts the average DC voltage level on the coaxial cable for use by the receiver squelch and collision detection circuits.

The receiver squelch circuit prevents noise on the coaxial cable from falsely triggering the receiver in the absence of a true signal. At the beginning of a packet, the receiver turns on when the DC level from the low pass filter exceeds the DC squelch threshold and the received packet has started with a 01 bit sequence with acceptable timing parameters. For normal signal levels this will take less than 500ns, or 5 bits. However, at the end of a packet, a fast receiver turn off is needed to reject both dribble bits on the coaxial cable and spurious responses due to settling of the on-chip bandpass filter. This is accomplished by an AC timing circuit that disables the receiver if the signal level on the coaxial cable remains high for typically 250ns and only enables the receiver again after approximately .5 μ s. Figures 5 and 6 illustrate receiver timing.

The differential line driver provides typically \pm 900mV signals to the DTE with less than 7ns rise and fall times. When in idle state (no received signal) its outputs provide <20mV differential voltage offset to minimize DC standing current in the isolation transformer.

Transmitter Functions

The transmitter has differential inputs and an open collector current driver output. The differential input common mode voltage is established by the CTI and should not be altered by external circuitry. Controlled rise and fall times of 25ns (\pm 5ns) minimize higher harmonic components in the transmitted spectrum, while matching of these rise and fall times to typically 2ns minimizes signal jitter. The drive current levels of the CTI are set by an on-chip bandgap voltage reference and an external 1% resistor. An on-chip isolation diode is provided to reduce the transmitter's coaxial cable load capacitance. For Thin Ethernet applications, no further external isolation diode is required, since the NE83C92 meets the capacitive loading specifications. For Ethernet applications a further external diode should be added to reduce loading capacitance.

The transmitter squelch circuit ensures that the transmitter can only be enabled if the transmitted packet begins with a 01 bit sequence where the negative-going differential signals are typically greater than 225mV in magnitude and 25ns in duration.

The transmitter will be disabled at the end of a packet if there are no negative going signals of greater than 225mV for more than typically 150ns. Figure 7 illustrates transmitter timing.

Collision Functions

The collision detection scheme implemented in the NE83C92 is receive mode detection, which detects a collision between any two stations on the network with certainty at all times, irrespective of whether or not the local DTE is producing one of the colliding signals. This is the only detection scheme allowed by the IEEE 802.3 standard for both repeater and non-repeater nodes.

The collision circuitry consists of the 4-pole Bessel low pass filter, a comparator, a precision voltage reference that sets up the collision threshold, a heartbeat generator, a 10MHz oscillator, and a differential line driver.

The collision comparator monitors the DC level at the output of the low pass filter and enables the line driver if it is more negative than the collision threshold. A collision condition is indicated to the DTE by a 10MHz oscillation signal at the CD outputs and typically occurs within 700ns of the onset of the collision. The collision signal begins with a negative-going pulse and ends with a continuous high-to-idle state longer than 170ns. Figure 8 illustrates collision timing.

At the end of every transmission, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. This pseudo collision consists of a 1 μ s burst of 10MHz oscillation at the line driver outputs approximately 1 μ s after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to V_{EE}. This allows the CTI to be used in repeater applications. Figure 9 illustrates heartbeat timing.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 30ms. The jabber circuit then enables the collision outputs for the remainder of the data packet and for typically 450ns (unjab time) after it has ended. At this point the transmitter becomes uninhibited. Figure 10 illustrates jabber timing.

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POR/Under Voltage Lockout/AUI Selection

The transmit and receive squelch circuits of the NE83C92 remain active if the absolute value of V_{EE} is less than the threshold for under voltage lockout, V_{UVL} . This prevents glitches from appearing on either the AUI or coaxial cable during power up and power down.

There is no collision announcement during power up and the transceiver waits for 400ms before becoming enabled.

If RXI is disconnected from the coaxial cable after power-up, its voltage will fall towards VEE. If the absolute value of this voltage exceeds the AUI disable voltage, V_{DIS} , for longer than 800ms, the transmit and receive squelch circuits remain active and, in addition, the AUI drivers become high impedance. This permits AUI connections to be hard wired together, e.g., the coaxial transceiver and 10BASE-T transceiver, with the signal path determined by which transceiver is connected to its external cable.

There is a 400ms collision announcement on disconnecting RXI, but there is no announcement on re-connection. This feature can be disabled by pulling RXI up with a 200kΩ to ground.

Detection of Coaxial Cable Faults

In the NE83C92 there is no internal loopback path from the TX inputs to the RX outputs. This means that, when the local DTE is transmitting, the signal will only be present at the receiver outputs RX+ and RX- if it appears on the coaxial cable and is larger than the receiver squelch threshold V_{RS} . If a short circuit fault condition occurs at the cable connector to the CTI, then no signal will appear at the receiver outputs.

In the case of an open circuit at the coaxial cable connector there will also be no signal at the receiver outputs due to the AUI disabling mode of the NE83C92. However, a heartbeat signal will be present following a transmission attempt for the short circuit condition, but not for the open circuit.

A coaxial cable with only a single 50Ω termination will generate a collision not only at every transmission attempt, but also for every reception attempt due to the receive mode collision detection of the NE83C92.

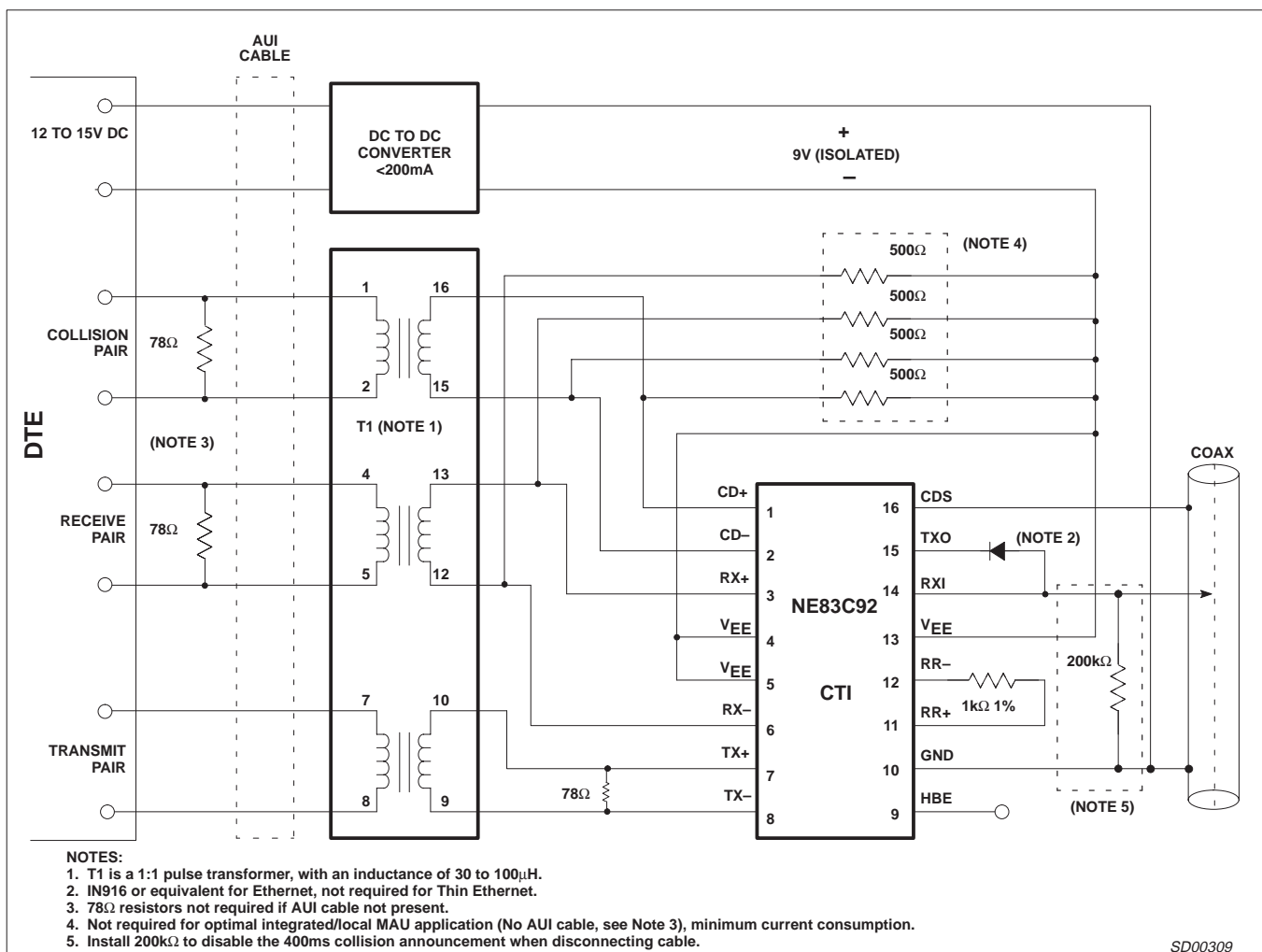


Figure 3. Connection Diagram for Standard 8392 Applications

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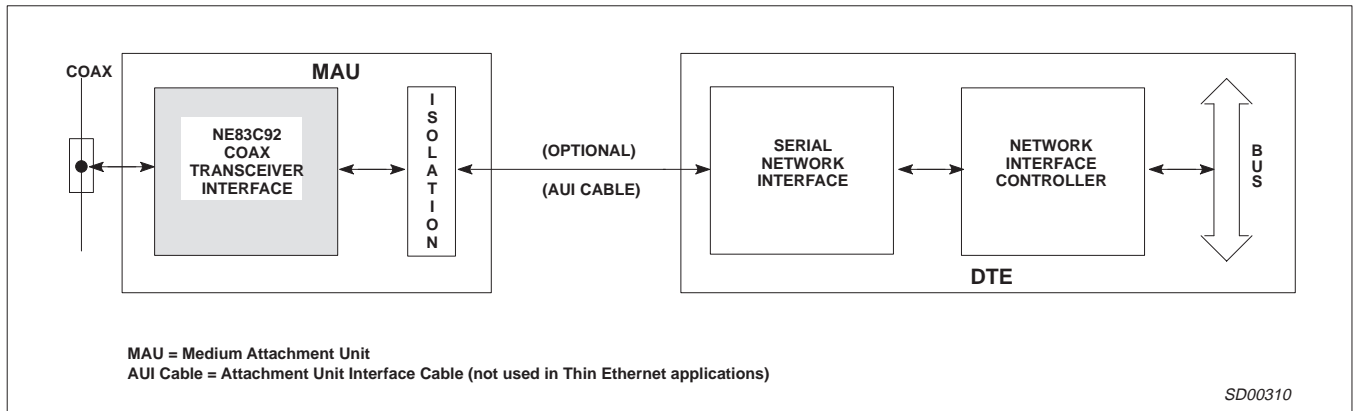


Figure 4. Interface Diagram for Ethernet/Thin Ethernet Local Area Network

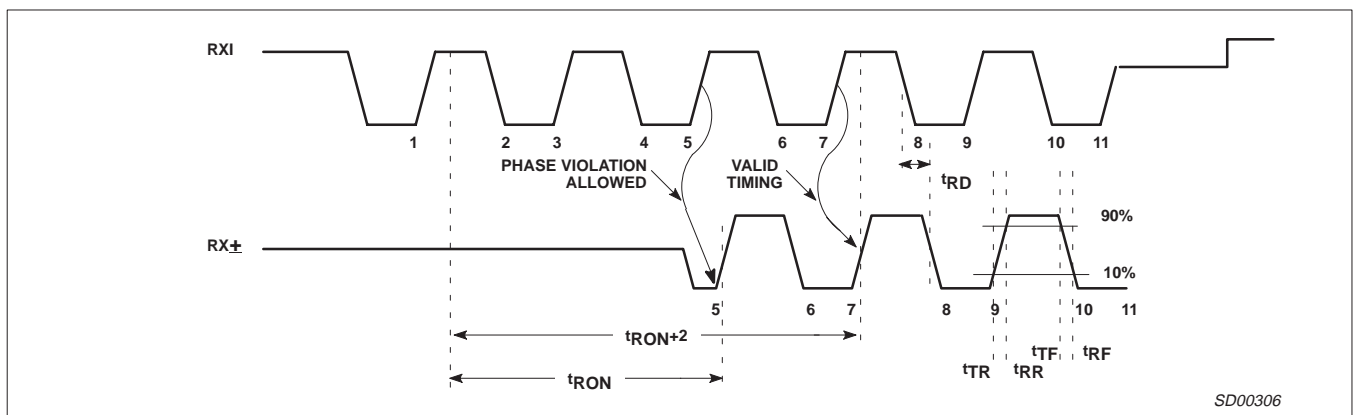


Figure 5. Receiver Timing

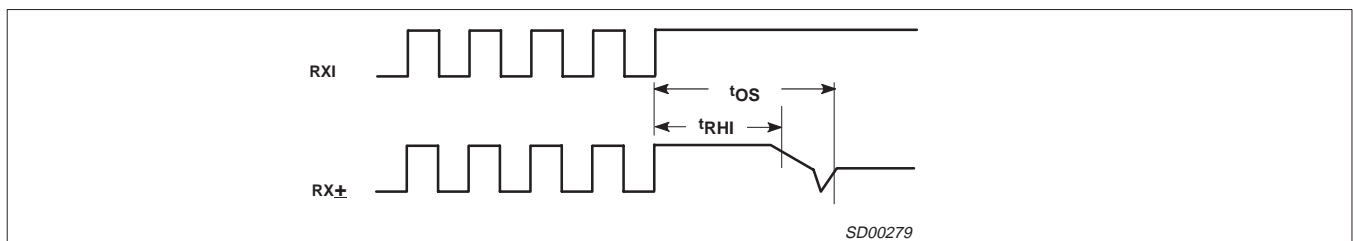


Figure 6. Receiver End-of-Packet Timing

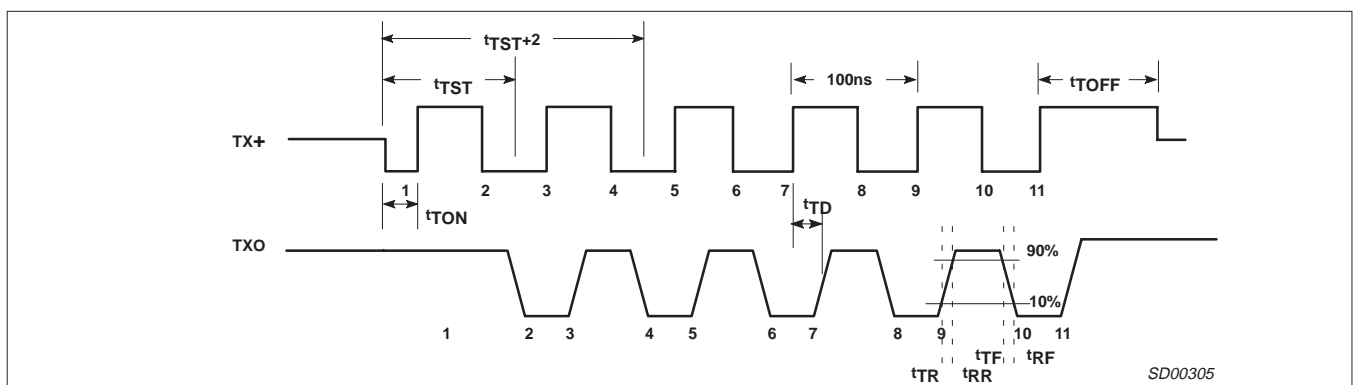


Figure 7. Transmitter Timing

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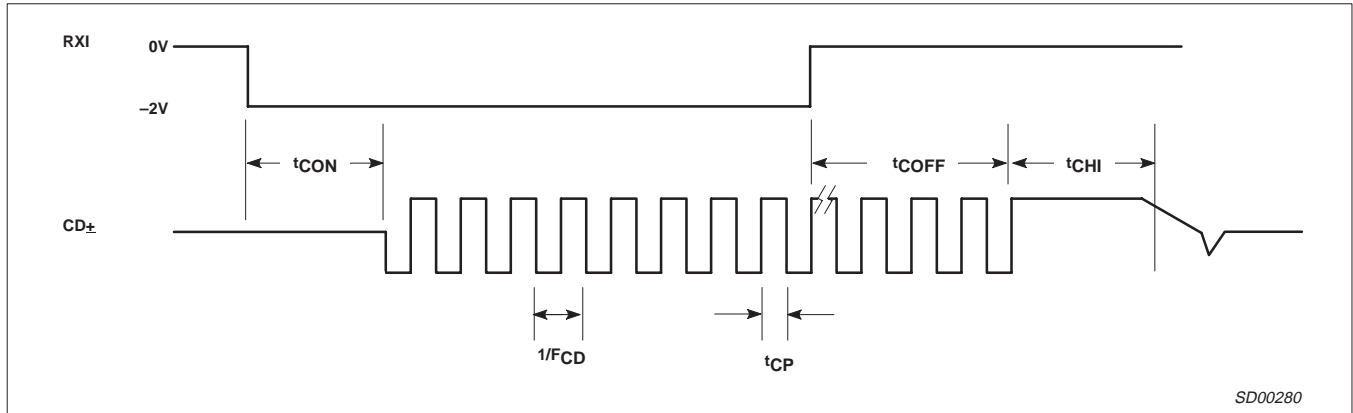


Figure 8. Collision Timing

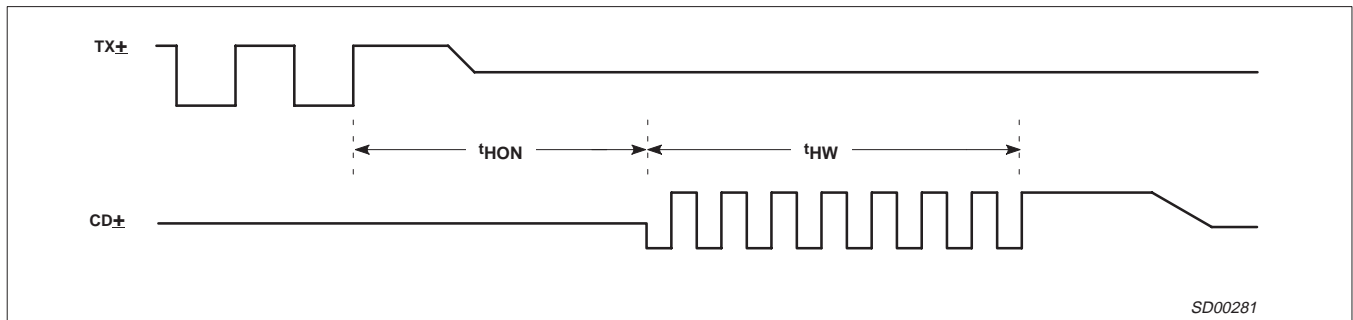


Figure 9. Heartbeat Timing

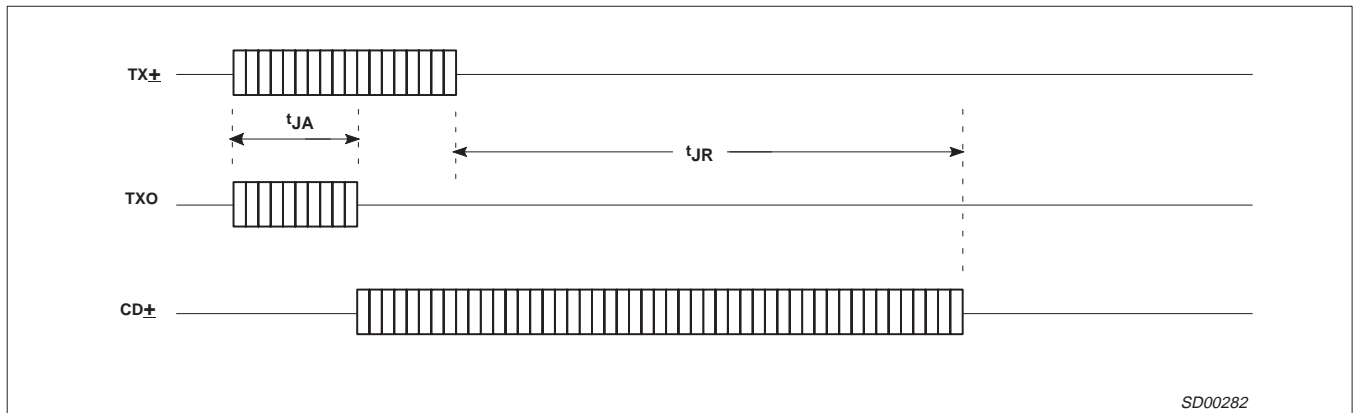


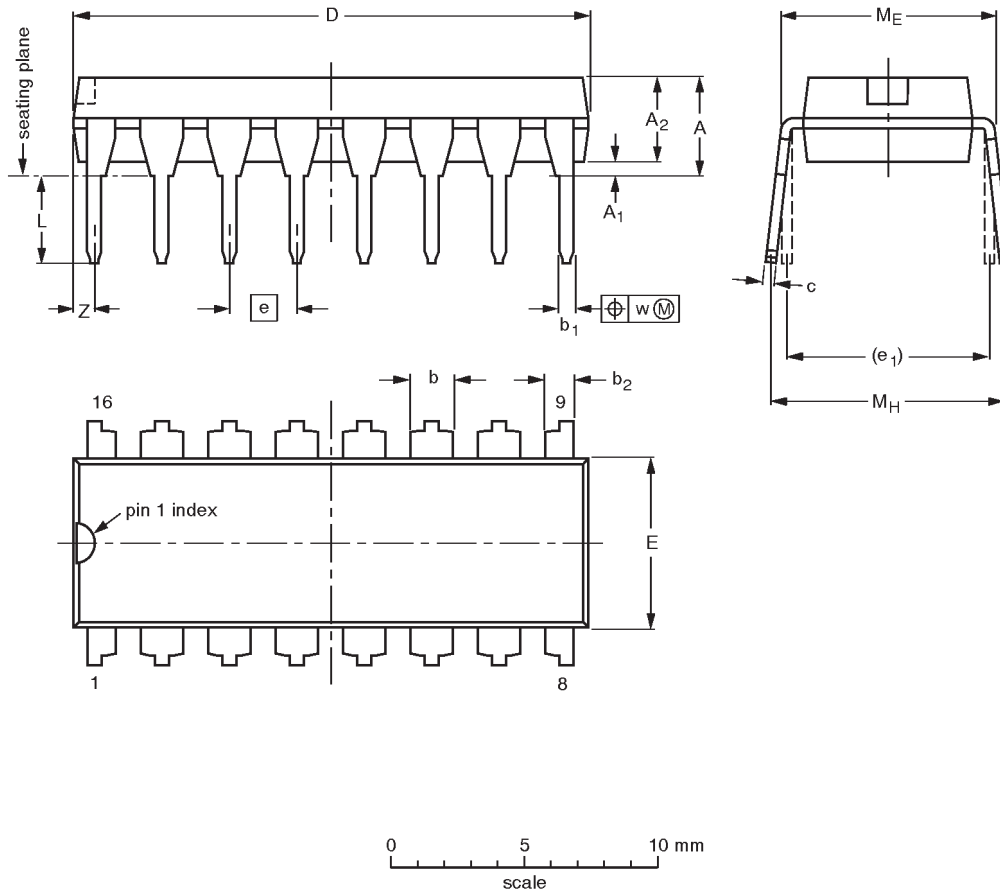
Figure 10. Jabber Timing

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

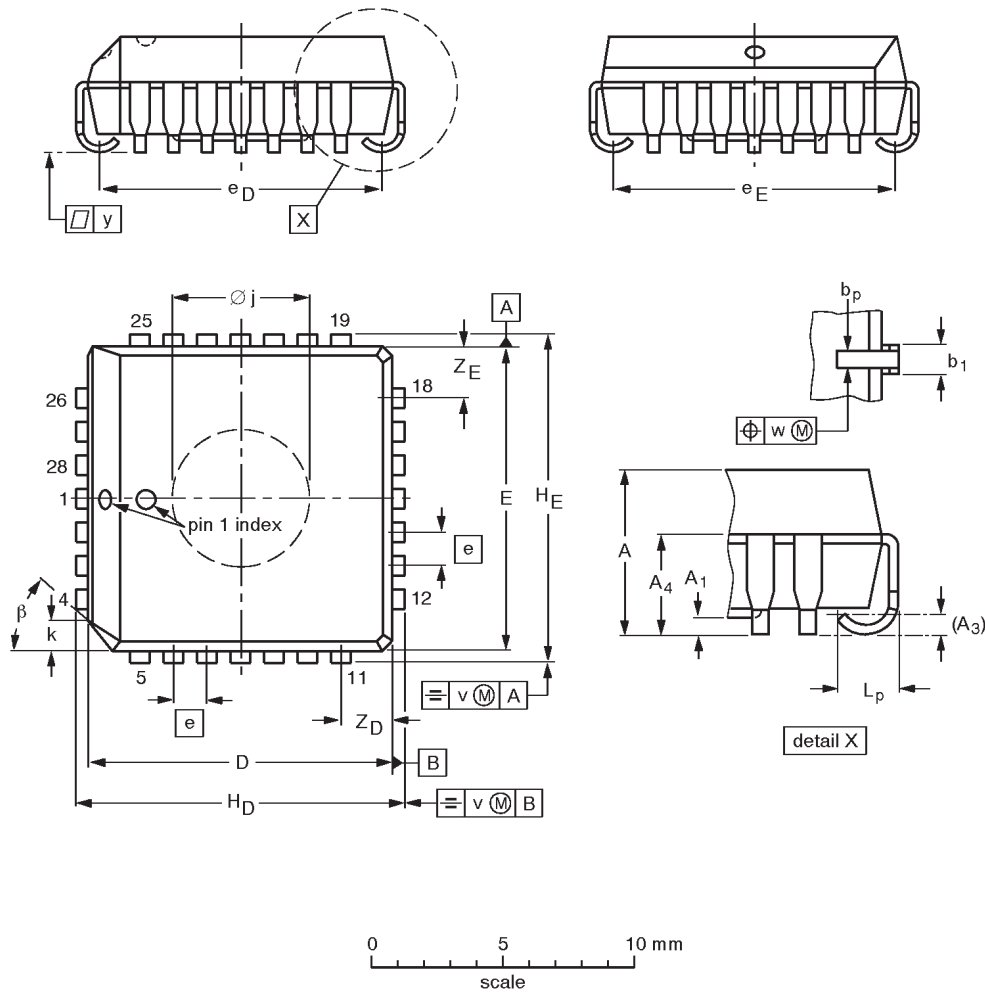
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						-92-11-17 95-01-14

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PLCC28: plastic leaded chip carrier; 28 leads; pedestal

SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A ₁ min.	A ₃	A ₄ max.	b _p	b ₁	D ⁽¹⁾	E ⁽¹⁾	e	e _D	e _E	H _D	H _E	k	∅ _j	L _p	v	w	y	Z _D ⁽¹⁾ max.	Z _E ⁽¹⁾ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT261-3		MO-047AB			95-02-25- 97-12-16

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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