DATA SHEET

TZA3043
Gigabit Ethernet/Fibre Channel transimpedance amplifier

Objective specification
File under Integrated Circuits, IC19

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Gigabit Ethernet/Fibre Channel transimpedance amplifier TZA3043

FEATURES

- Wide dynamic range, typically 2.5 μA to 1.5 mA
- Differential transimpedance of 14 kΩ
- Wide bandwidth of 950 MHz
- Differential outputs
- On-chip AGC (Automatic Gain Control)
- No external components required
- Single supply voltage from 3.0 to 5.5 V
- Bias voltage for PIN diode
- Pin compatible with TZA3023 and SA5223.

APPLICATIONS

- Digital fibre optic receiver in medium and long haul optical telecommunications transmission systems or in high speed data networks
- Wideband RF gain block.

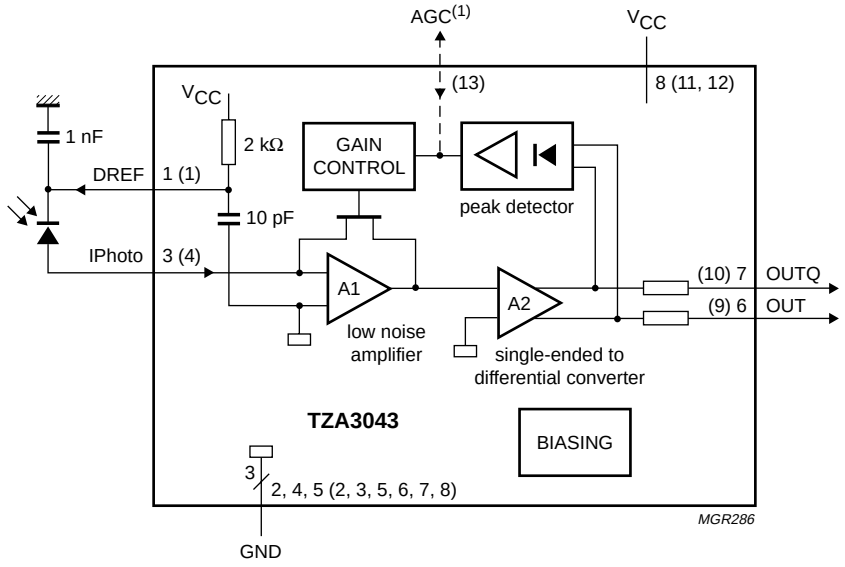
DESCRIPTION

The TZA3043 is a high speed transimpedance amplifier with AGC designed to be used in Gigabit Ethernet/Fibre Channel optical links. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and converts it to a differential output voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3043T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TZA3043U	naked die	die in waffle pack carriers; die dimensions 0.960 × 1.210 mm	–

BLOCK DIAGRAM



(1) AGC analog I/O is only available on the TZA3043U (pad 13).
The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
DREF	1	analog output	bias voltage for PIN diode (V_{CC}); cathode should be connected to this pin
GND	2	ground	ground
IPhoto	3	analog input	current input; anode of PIN diode should be connected to this pin; DC bias level of 822 mV is one diode voltage above ground
GND	4	ground	ground
GND	5	ground	ground
OUT	6	data output	data output; OUT goes HIGH when current flows into IPhoto (pin 3)
OUTQ	7	data output	compliment of OUT (pin 6)
V_{CC}	8	supply	supply voltage

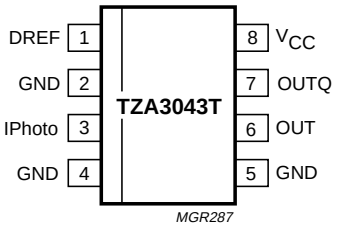
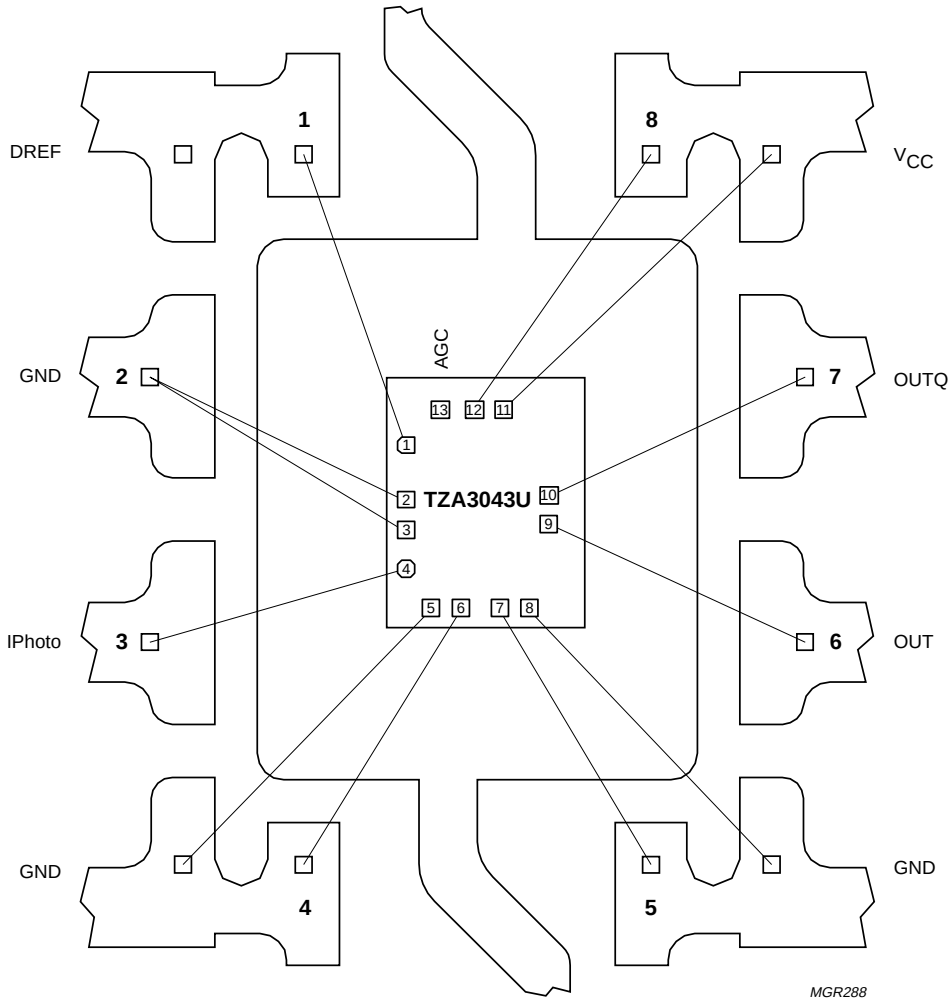


Fig.2 Pin configuration.

PAD CONFIGURATION

Bonding pad locations



Pad 13 (AGC) is not bonded.

Fig.3 Bonding diagram TZA3043U.

Pad centre locations

SYMBOL	PAD	COORDINATES(1)	
		x	y
DREF	1	95	881
GND	2	95	618
GND	3	95	473
IPhoto	4	95	285
GND	5	215	95
GND	6	360	95
GND	7	549	95
GND	8	691	95
OUT	9	785	501
OUTQ	10	785	641
V_{CC}	11	567	1055
V_{CC}	12	424	1055
AGC	13	259	1055

Note

1. All coordinates (μm) are measured with respect to the bottom left-hand corner of the die.

FUNCTIONAL DESCRIPTION

The TZA3043 is a transimpedance amplifier intended for use in fibre optic links for signal recovery in Fibre Channel applications. It amplifies the current generated by a photo detector (PIN diode or avalanche photodiode) and transforms it into a differential output voltage. The most important characteristics of the TZA3043 are high receiver sensitivity and wide dynamic range. High receiver sensitivity is achieved by minimizing noise in the transimpedance amplifier.

Input circuit

The signal current generated by a PIN diode can vary between 2.5 μA to 1.5 mA (peak-to-peak value).

An AGC loop (see Fig.1) is implemented to make it possible to handle such a wide dynamic range.
The AGC loop increases the dynamic range of the receiver by reducing the feedback resistance of the preamplifier. The AGC loop hold capacitor is integrated on-chip, so an external capacitor is not needed for AGC.

AGC monitoring

The AGC voltage can be monitored at pad 13 on the naked die (TZA3043U). Pad 13 is not bonded in the packaged device (TZA3043T). This pad can be left unconnected during normal operation. It can also be used to force an external AGC voltage. If pad 13 (AGC) is connected to GND, the internal AGC loop is disabled and the receiver gain is at a maximum. The maximum input current is then about 75 μA.

Output circuit

The differential amplifier A2 converts the output of the preamplifier A1 to a differential voltage (see Fig.4).

The logic level symbol definitions for the differential outputs are shown in Fig.5.

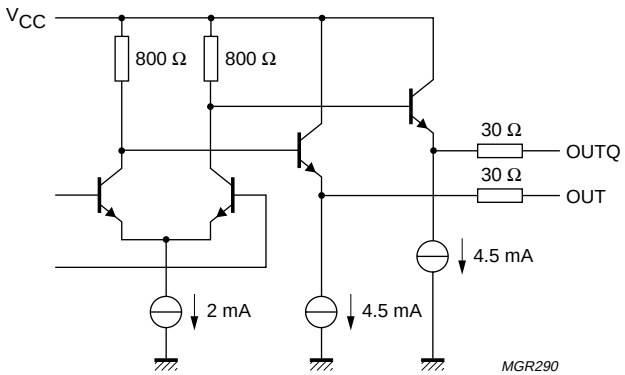


Fig.4 Differential data output circuit.

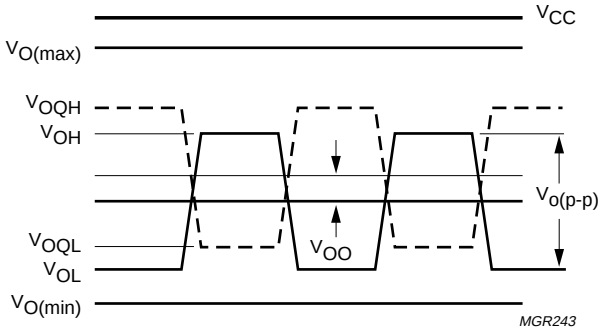


Fig.5 Logic level symbol definitions for data outputs OUT and OUTQ.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+5.5	V
V_n	DC voltage			
	pin 3/pad 4: IPhoto	–0.5	+1	V
	pins 6 and 7/pads 9 and 10: OUT and OUTQ	–0.5	V_{CC} + 0.5	V
	pad 13: AGC (TZA3043U only)	–0.5	V_{CC} + 0.5	V
	pin 1/pad 1: DREF	–0.5	V_{CC} + 0.5	V
I_n	DC current			
	pin 3/pad 4: IPhoto	–2.5	+2.5	mA
	pins 6 and 7/pads 9 and 10: OUT and OUTQ	–15	+15	mA
	pad 13: AGC (TZA3043U only)	–0.2	+0.2	mA
	pin 1/pad 1: DREF	–2.5	+2.5	mA
P_{tot}	total power dissipation	–	300	mW
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	150	°C
T_{amb}	ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	tbf	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	tbf	K/W

CHARACTERISTICS

For typical values T_{amb} = 25 °C and V_{CC} = 5 V; minimum and maximum values are valid over the entire ambient temperature range and process spread.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		3	5	5.5	V
I_{CC}	supply current	AC coupled; R_L = 50 Ω	–	35	62	mA
P_{tot}	total power dissipation	V_{CC} = 5 V	–	175	341	mW
		V_{CC} = 3.3 V	–	112	212	mW
T_j	junction temperature		–40	–	+110	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
R_{tr}	small-signal transresistance of the receiver	measured differentially; AC coupled				
		R_L = ∞	–	29	–	kΩ
		R_L = 50 Ω	–	14.5	–	kΩ
$f_{-3dB(h)}$	high frequency –3 dB point	V_{CC} = 5 V; C_i = 0.7 pF	–	920	–	MHz
		V_{CC} = 3.3 V; C_i = 0.7 pF	–	800	–	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{n(tot)}$	total integrated RMS noise current over bandwidth	referred to input; Δf = 920 MHz; note 1	–	200	–	nA
$\Delta R_{tr}/\Delta t$	AGC loop constant		–	1	–	dB/ms
PSRR	power supply rejection ratio	measured differentially; note 2				
		f = 1 to 100 MHz	–	2	–	μA/V
		f = 1 GHz	–	66	–	μA/V
Input: IPhoto						
$V_{bias(IPhoto)}$	input bias voltage on pin IPhoto		650	822	970	mV
$I_{i(IPhoto)(p-p)}$	input current on pin IPhoto (peak-to-peak value)	V_{CC} = 5 V	–2000	+4	+2000	μA
		V_{CC} = 3.3 V	–1000	+4	+1000	μA
Data outputs: OUT and OUTQ						
$V_{O(CM)}$	common mode output voltage	AC coupled; R_L = 50 Ω	V_{CC} – 1.800	V_{CC} – 1.700	V_{CC} – 1.600	V
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	AC coupled; R_L = 50 Ω	150	200	260	mV
V_{OO}	differential output offset voltage		–30	–	+30	mV
R_o	output resistance	single-ended; DC tested	42	50	58	Ω
t_r	rise time	20% to 80%	–	200	tbf	ps
t_f	fall time	80% to 20%	–	200	tbf	ps

Notes

1. All $I_{n(tot)}$ measurements were made with an input capacitance of C_i = 1 pF. This was comprised of 0.5 pF for the photodiode itself, with 0.3 pF allowed for the printed-circuit board layout and 0.2 pF intrinsic to the package.
2. PSRR is defined as the ratio of the equivalent current change at the input (ΔI_{IPhoto}) to a change in supply voltage:

$$PSRR = \frac{\Delta I_{IPhoto}}{\Delta V_{CC}}$$

For example, a disturbance of +10 mV on V_{CC} at 10 MHz will typically add an extra 20 nA to the photodiode current. The external capacitor between pin DREF and pin GND has a large impact on PSRR. The specification is valid with an external capacitor of 1 nF.

APPLICATION INFORMATION

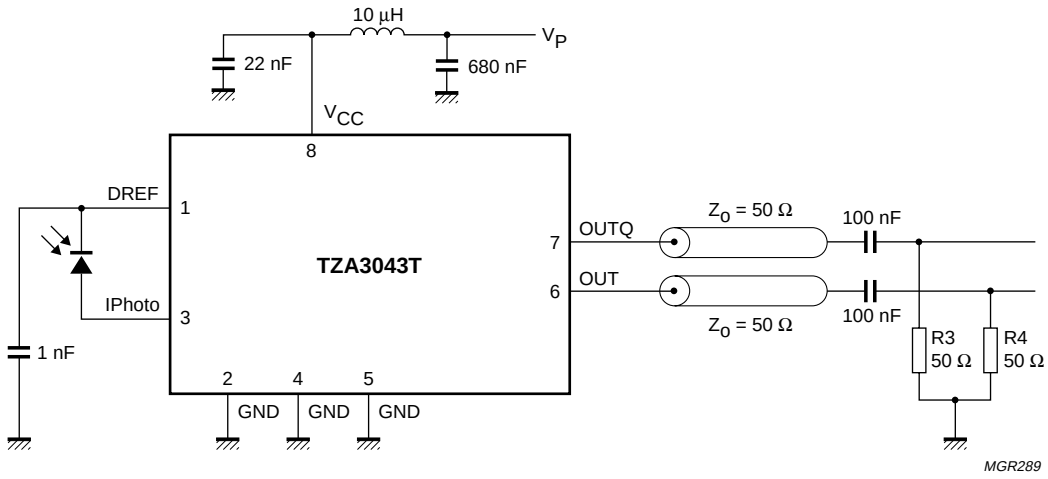
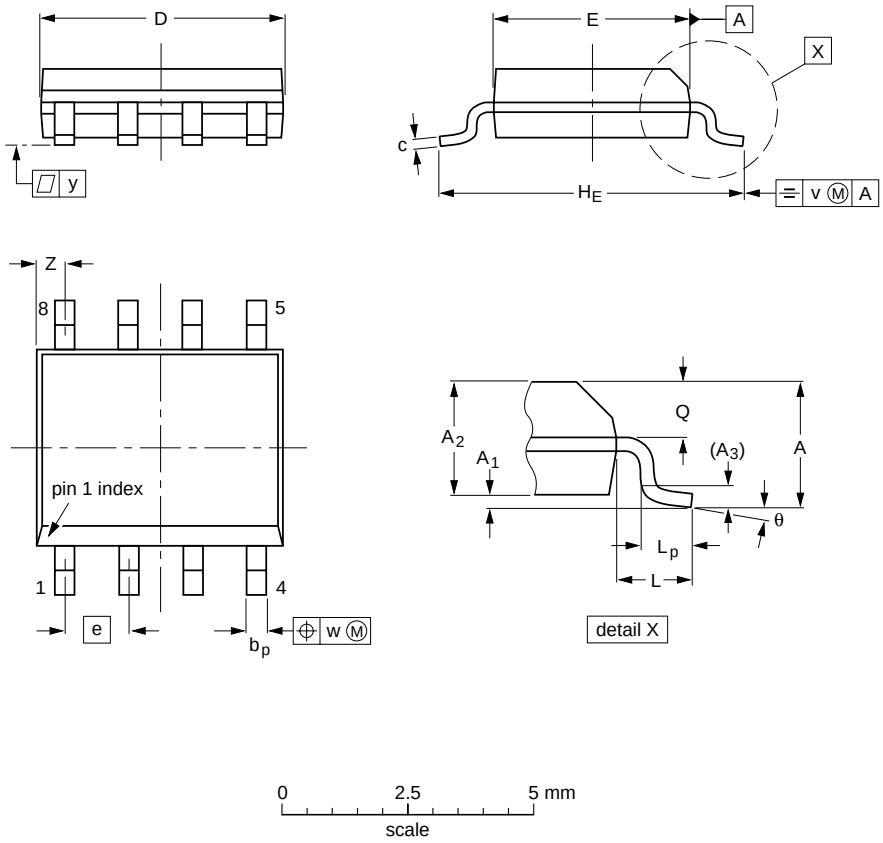


Fig.6 Application diagram.

PACKAGE OUTLINE

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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