DATA SHEET

TZA3044T; TZA3044U
1.25 Gbits/s Gigabit Ethernet postamplifiers

Objective specification
File under Integrated Circuits, IC19

1998 Jul 07

Philips
Semiconductors

PHILIPS

1.25 Gbits/s Gigabit Ethernet postamplifiers TZA3044T; TZA3044U

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 1.25 GHz typical
- Applicable in 1.25 Gbits/s Gigabit Ethernet receivers
- Single supply voltage from 3.0 to 5.5 V
- PECL (Positive Emitter Coupled Logic) compatible data outputs
- Programmable input signal level-detection to be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor
- Fully differential for excellent PSRR.

APPLICATIONS

- Digital fibre optic receiver for Gigabit Ethernet applications
- Wideband RF gain block.

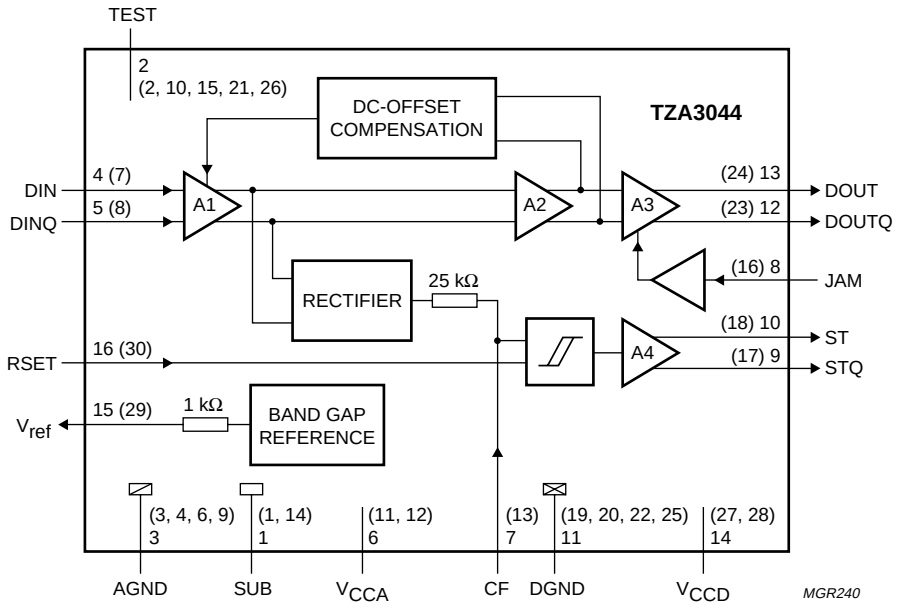
GENERAL DESCRIPTION

The TZA3044 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers like the TZA3043. It is pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range, and needs less external components. Capable of operating at 1.25 Gbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level-detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3044T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3044U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM



The numbers in brackets refer to the pad numbers of the naked die version.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
SUB	1	substrate	substrate pin; must be at the same potential as AGND (pin 3)
TEST	2	test pin	for test purpose only; to be left open in the application
AGND	3	ground	analog ground; must be at the same potential as DGND (pin 11)
DIN	4	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DINQ (pin 5)
DINQ	5	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DIN (pin 4)
V_{CCA}	6	supply	analog supply voltage; must be at the same potential as V_{CCD} (pin 14)
CF	7	analog input	filter capacitor for input signal level detector; capacitor should be connected between this pin and V_{CCA} (pin 6)
JAM	8	PECL input	PECL-compatible input; controls the output buffers DOUT and DOUTQ (pins 13 and 12). When a LOW signal is applied, the outputs will follow the input signal. When a HIGH signal is applied, the DOUT and DOUTQ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled LOW (JAM OFF).
STQ	9	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complimentary to ST (pin 10)
ST	10	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complimentary to STQ (pin 9)
DGND	11	ground	digital ground; must be at the same potential as AGND (pin 3)
DOUTQ	12	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a HIGH condition; complimentary to DOUT (pin 13)
DOUT	13	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a LOW condition; complimentary to DOUTQ (pin 12)
V_{CCD}	14	supply	digital supply voltage; must be at the same potential as V_{CCA} (pin 6)
V_{ref}	15	analog output	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 kΩ
RSET	16	analog input	input signal level detector programming; nominal DC voltage is V_{CCA} − 1.5 V; threshold level is set by connecting an external resistor between RSET and V_{CCA} or by forcing a current into RSET; default value for this resistor is 180 kΩ which corresponds with approximately 4 mV (p-p) differential input signal

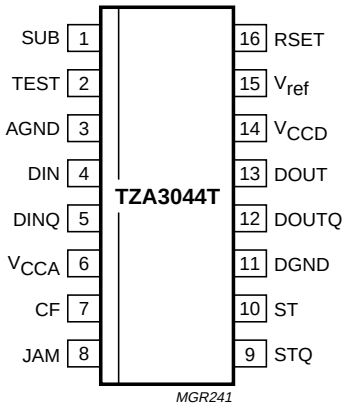


Fig.2 Pin configuration.

PAD CONFIGURATION

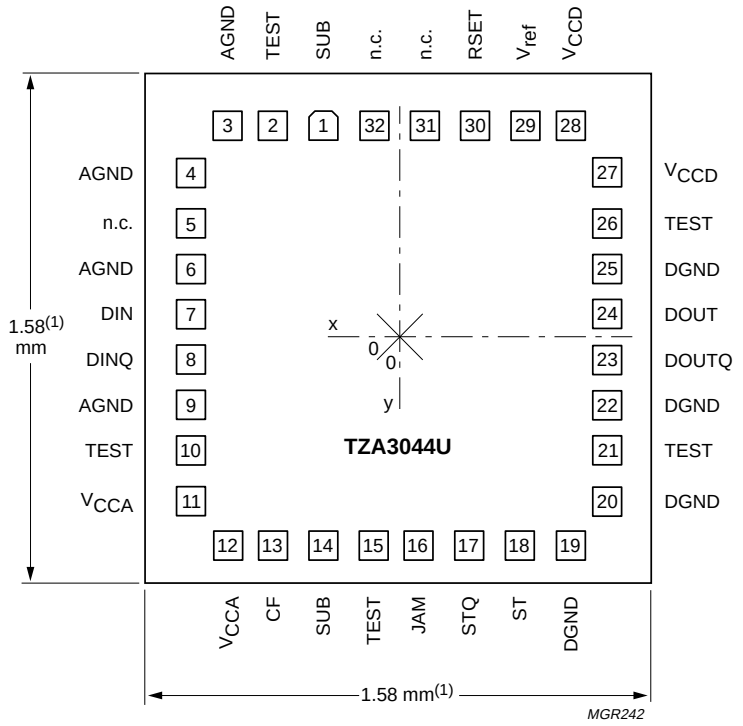
Pad centre locations

SYMBOL	PAD	COORDINATES(1)	
		x	y
SUB	1	–235.7	+647.8
TEST	2	–392.8	+647.8
AGND	3	–532.8	+647.8
AGND	4	–647.8	+507.1
n.c.	5	–647.8	+350.0
AGND	6	–647.8	+210.0
DIN	7	–647.8	+70.0
DINQ	8	–647.8	–70.0
AGND	9	–647.8	–210.0
TEST	10	–647.8	–350.0
V_{CCA}	11	–647.8	–507.1
V_{CCA}	12	–532.8	–647.8
CF	13	–392.8	–647.8
SUB	14	–235.7	–647.8
TEST	15	–78.6	–647.8
JAM	16	+61.4	–647.8
STQ	17	+218.5	–647.8
ST	18	+375.6	–647.8
DGND	19	+532.7	–647.8
DGND	20	+647.8	–507.1
TEST	21	+647.8	–350.0
DGND	22	+647.8	–210.0
DOUTQ	23	+647.8	–70.0
DOUT	24	647.8	70.0
DGND	25	647.8	210.0
TEST	26	647.8	350.0
V_{CCD}	27	647.8	507.1
V_{CCD}	28	532.7	647.8
V_{ref}	29	392.7	647.8
RSET	30	235.6	647.8
n.c.	31	78.5	647.8
n.c.	32	–78.6	+647.8

Note

1. Coordinates represent the position of the centre of the pad, in μm, with respect to the centre of the die.

Bonding pad locations



(1) Typical value.
Pad size: 90 × 90 μm.

Fig.3 Bonding pad locations: TZA3044U.

FUNCTIONAL DESCRIPTION

The TZA3044 accepts up to 1.25 Gbits/s Gigabit Ethernet data streams, with amplitudes from 2 mV (p-p) up to 1 V (p-p) single-ended. The input signal will be amplified and limited to differential PECL output levels (see Fig.1).

The input buffer A1 presents an impedance of approximately 4.5 kΩ to the data stream on the inputs DIN and DINQ. The input can be used both single-ended and differential, but differential operation is preferred for better performance.

Because of the high gain of the postamplifier, a very small offset voltage would shift the decision level in such a way that the input sensitivity decreases drastically. Therefore a DC offset compensation circuit is implemented in the TZA3044, which keeps the input of buffer A3 at its toggle point in the absence of any input signal.

An input signal level detection is implemented to check if the input signal is above the user-programmed level. The outcome of this test is available at the PECL outputs ST and STQ. This flag can also be used to prevent the PECL outputs DOUT and DOUTQ from reacting to noise in the absence of a valid input signal, by connecting the output STQ to the input JAM. This insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation.

PECL logic

The logic level symbol definitions for PECL are shown in Fig.4.

Input biasing

The input pins DIN and DINQ are DC biased at approximately 2.55 V by an internal reference generator (see Fig.5). The TZA3044 can be DC coupled, but AC coupling is preferred. In case of DC coupling, the driving source must operate within the allowable input signal range (2.0 V to V_{CCA} + 0.5 V). Also a DC offset voltage of

more than a few millivolt should be avoided, since the internal DC offset compensation circuit has a limited correction range.

If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors must be large enough to pass the lowest input frequency of interest. For example, 1 nF coupling capacitors react with the internal 4.5 kΩ input bias resistors to yield a lower −3 dB frequency of 35 kHz. This then sets a limit on the maximum number of consecutive pulses that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation must be included for an accurate calculation.

DC-offset compensation

A control loop connected between the inputs of buffer A3 and amplifier A1 (see Fig.1) will keep the input of buffer A3 at its toggle point in the absence of any input signal. Because of the active offset compensation which is integrated in the TZA3044, no external capacitor is required. The loop time constant determines the lower cut-off frequency of the amplifier chain, which is set at approximately 850 Hz.

Input signal level-detection

The TZA3044 allows for user-programmable input signal level-detection and can automatically disable the switching of the PECL outputs if the input signal is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the signal-to-noise ratio of the input signal is sufficient for low bit-error-rate system operation. Complementary PECL flags (ST and STQ) indicate whether the input signal is above or below the programmed threshold level.

The input signal is amplified and rectified before being compared to a programmable threshold reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1 μs time constant and additional filtering can be achieved by using an external capacitor between pin CF and V_{CCA} (the internal driving impedance nominally is 25 kΩ). The resultant signal is then compared to a threshold current through pin RSET (see Fig.6). This current can be set by connecting an external resistor R_{DETECT} between pin RSET and V_{CCA}, or by forcing a current into pin RSET.

The relationship between the threshold current and the detected input voltage is approximately:

$$I_{RSET} = 0.002 \times (V_{DIN} - V_{DINQ})\ [A] \quad (1)$$

Since the voltage on pin RSET is held constant at 1.5 V below V_{CCA}, the current flowing into this pin will be:

$$I_{RSET} = \frac{1.5}{R_{DETECT}}\ [A] \quad (2)$$

Combining these two formulas results in a general formula to calculate R_{DETECT} for a given input signal level-detection:

$$R_{DETECT} = \frac{750}{(V_{DIN} - V_{DINQ})}\ [\Omega] \quad (3)$$

In this formula, V_{DIN} and V_{DINQ} are in V (p-p).

Example: Detection should occur if the differential voltage of the input signals drops below 4 mV (p-p). In this case, a reference current of $0.002 \times 0.004 = 8$ μA should flow into pin RSET. This can be set using a current source or simply by connecting a resistor of the appropriate value. The resistor must be connected between V_{CCA} and pin RSET. In this example the resistor would be:

$$R_{DETECT} = \frac{750}{0.004} = 187.5\ k\Omega$$

The hysteresis is fixed internally at 3 dB electrical. In the example of above, a differential level below 4 mV (p-p) of the input signal will drive pin ST to LOW, and an input signal level above 5.7 mV (p-p) will drive pin ST to HIGH.

Since a JAM function is provided which forces the data outputs to a predetermined state (DOUT = LOW and DOUTQ = HIGH), the pins STQ and JAM can be connected to automatically disable the signal transmission when the chip senses that the input signal is below the programmed threshold.

Response time of the input signal level-detection circuit is determined by the time constant of the input capacitors, together with the filter time constant (1 μs internal plus the additional capacitor at pin CF).

PECL output circuits

The output circuit of ST and STQ is given in Fig.7

The output circuit of DOUT and DOUTQ is given in Fig.8.

Some PECL termination schemes are given in Fig.9.

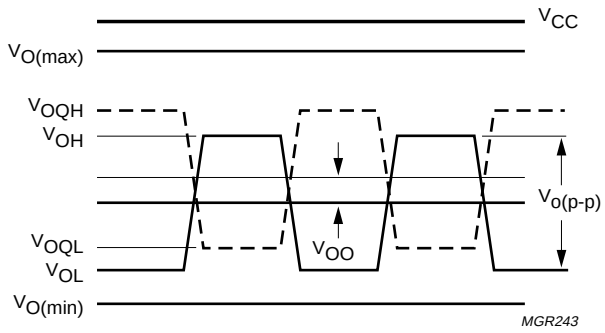


Fig.4 Logic level symbol definitions for PECL.

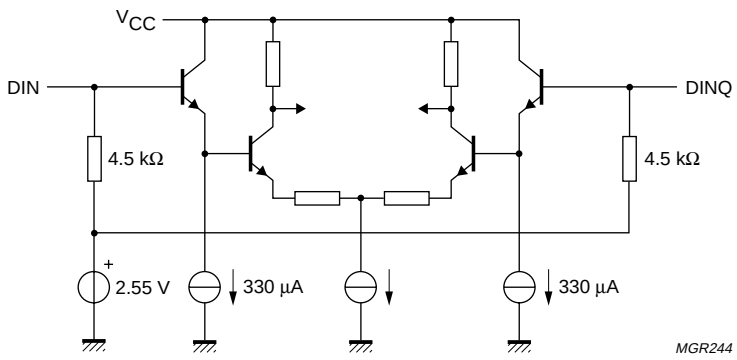


Fig.5 Data input circuit DIN and DINQ.

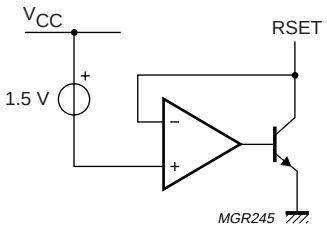


Fig.6 Level-detect input circuit RSET.

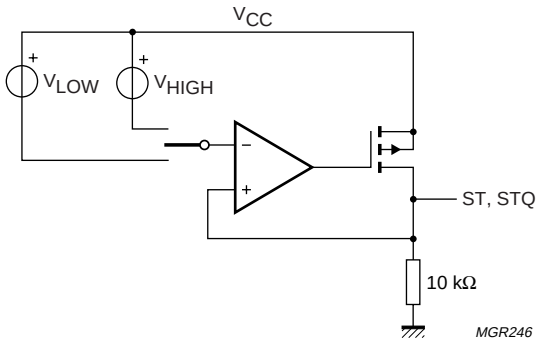


Fig.7 PECL output circuit ST and STQ.

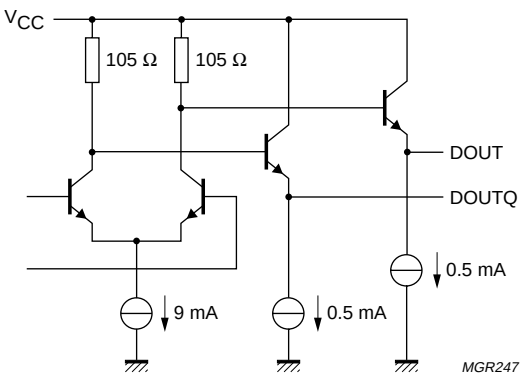
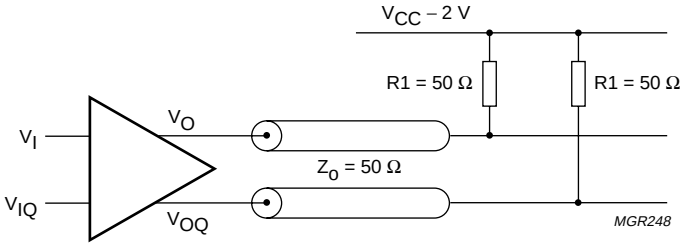
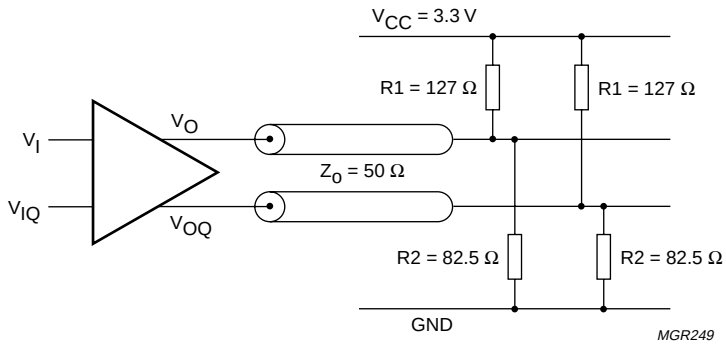


Fig.8 PECL output circuit DOUT and DOUTQ.





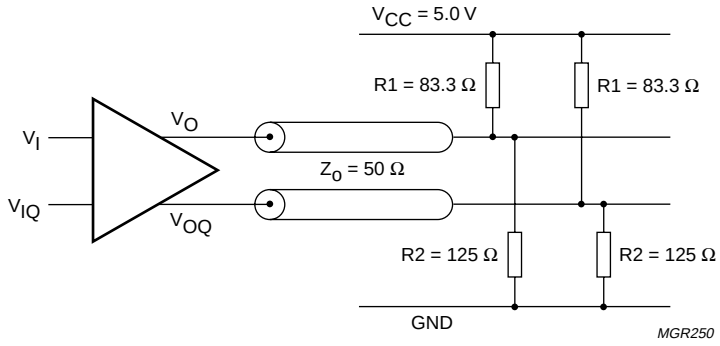


Fig.9 PECL output termination schemes.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6	V
V_n	DC voltage	note 1			
	pins 4 and 5 (7 and 8): DIN and DINQ		–0.5	V_{CC} + 0.5	V
	pin 7 (13): CF		–0.5	V_{CC} + 0.5	V
	pin 8 (16): JAM		–0.5	V_{CC} + 0.5	V
	pins 9, 10, 12 and 13 (17, 18, 23 and 24): STQ, ST, DOUTQ and DOUT		V_{CC} – 2	V_{CC} + 0.5	V
	pin 15 (29): V_{ref}		–0.5	+3.2	V
	pin 16 (30): RSET		–0.5	V_{CC} + 0.5	V
I_n	DC current	note 1			
	pin 4 and 5 (7 and 8): DIN and DINQ		–1	+1	mA
	pin 7 (13): CF		–1	+1	mA
	pin 8 (16): JAM		–1	+1	mA
	pins 9, 10, 12 and 13 (17, 18, 23 and 24): STQ, ST, DOUTQ and DOUT		–25	+10	mA
	pin 15 (29): V_{ref}		–2	+2.5	mA
	pin 16 (30): RSET		–2	+2	mA
P_{tot}	total power dissipation		–	tbf	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–40	+85	°C

Note

1. The numbers in brackets refer to the pad numbers of the naked die version.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	tbf	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	tbf	K/W

CHARACTERISTICS

For typical values T_{amb} = 25 °C and V_{CC} = 3.3 V; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages with respect to ground; unless otherwise specified.

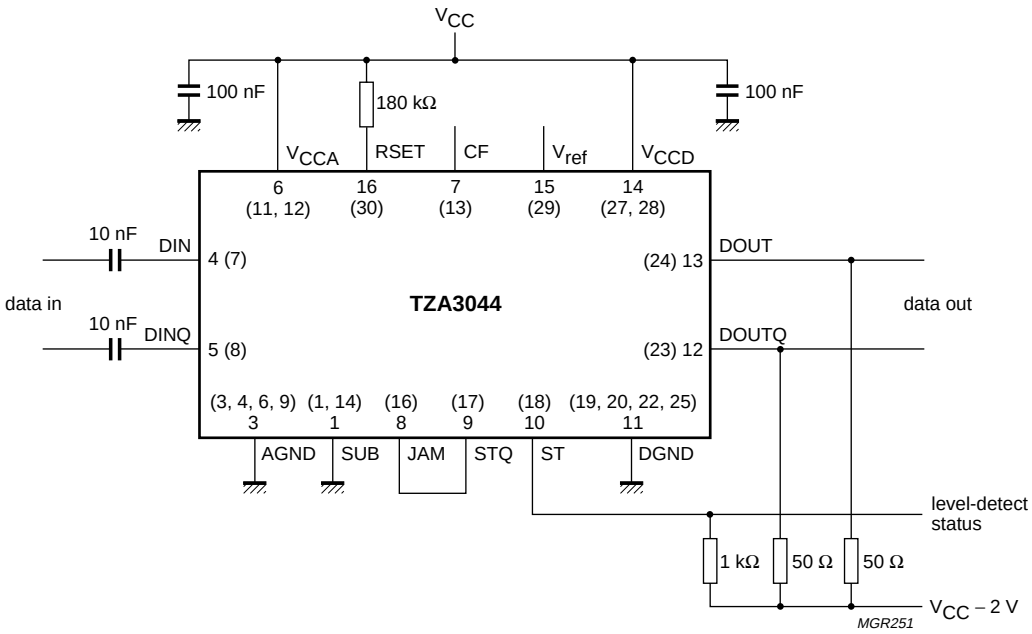
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		3	3.3	5.5	V
I_{CCD}	digital supply current	note 1	–	18	27	mA
I_{CCA}	analog supply current		–	15	22	mA
P_{tot}	total power dissipation	note 1	–	110	270	mW
T_j	junction temperature		–40	–	+120	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
Inputs: DIN and DINQ						
$V_{i(se)(p-p)}$	input signal voltage single-ended (peak-to-peak)		0.002	–	1.0	V
$V_{i(dif)(p-p)}$	input signal voltage differential (peak-to-peak)		0.004	–	2.0	V
V_I	absolute input signal voltage		2.1	2.55	V_{CCA} + 0.5	V
$V_{IO(eq)}$	equivalent input signal offset voltage		–	–	50	µV
$V_{IO(cor)}$	input offset voltage correction range	note 2	–5	–	+5	mV
R_i	input resistance	single-ended	2.9	4.5	7.6	kΩ
C_i	input capacitance	single-ended	–	–	2.5	pF
$V_{n(i)(rms)}$	equivalent input RMS noise voltage	note 3	–	115	145	µV
Input signal level-detect: RSET						
I_{ref}	reference current	note 4	5	–	60	µA
V_{ref}	reference voltage	referred to V_{CCA}	–1.55	–1.5	–1.45	V
$V_{th(p-p)}$	programmability (single-ended, peak-to-peak)	V_i = 200 kHz square wave	2	–	12	mV
hys	hysteresis	electrically measured	2	3	4	dB
R_F	filter resistance		14	25	41	kΩ
t_F	filter time constant	CF = 0	0.5	1.0	2.0	µs
PECL outputs: DOUT and DOUTQ						
V_{OL}	LOW-level output voltage	R_L = 50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OH}	HIGH-level output voltage	R_L = 50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
t_r	rise time	20% to 80%	–	150	250	ps
t_f	fall time	80% to 20%	–	100	200	ps
$t_{w(p-p)}$	pulse width distortion		–	–	30	ps
$f_{-3dB(l)}$	low frequency –3 dB point		–	0.85	1.5	kHz
$f_{-3dB(h)}$	high frequency –3 dB point		1000	1300	1600	MHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PECL outputs: ST and STQ						
V_{OL}	LOW-level output voltage	R_L = 50 Ω to V_{CC} – 2 V	V_{CC} – 1840	–	V_{CC} – 1620	mV
V_{OH}	HIGH-level output voltage	R_L = 50 Ω to V_{CC} – 2 V	V_{CC} – 1100	–	V_{CC} – 900	mV
t_r	rise time	20% to 80%	–	–	600	ns
t_f	fall time	80% to 20%	–	–	200	ns
PECL input: JAM						
V_{IL}	LOW-level input voltage		–	–	V_{CC} – 1490	mV
V_{IH}	HIGH-level input voltage		V_{CC} – 1165	–	–	mV
$I_{I(JAM)}$	JAM input current	note 5	–10	–	+10	µA
Reference voltage output: V_{ref}						
V_{ref}	reference voltage	note 6	1.165	1.20	1.235	V

Notes

1. DOUT, DOUTQ, ST and STQ outputs are left unconnected.
2. If the input is DC coupled, the preceding amplifier's output offset voltage should not exceed these limits, in order to avoid malfunctioning of the DC offset compensation circuit.
3. $\text{Input RMS noise} = \frac{\text{total output RMS noise}}{\text{low frequency gain}}$
4. The reference currents can be set by a resistor between V_{CCA} and pin RSET. The corresponding input signal level-detect range is from 2 to 12 mV (p-p) single-ended. See section "Input signal level-detection" for detailed information.
5. Internal pull-down resistor of 500 kΩ to DGND.
6. Internal series resistor of 1 kΩ.

APPLICATION INFORMATION



The numbers in brackets refer to the pad numbers of the naked die version.

Fig.10 Application diagram.

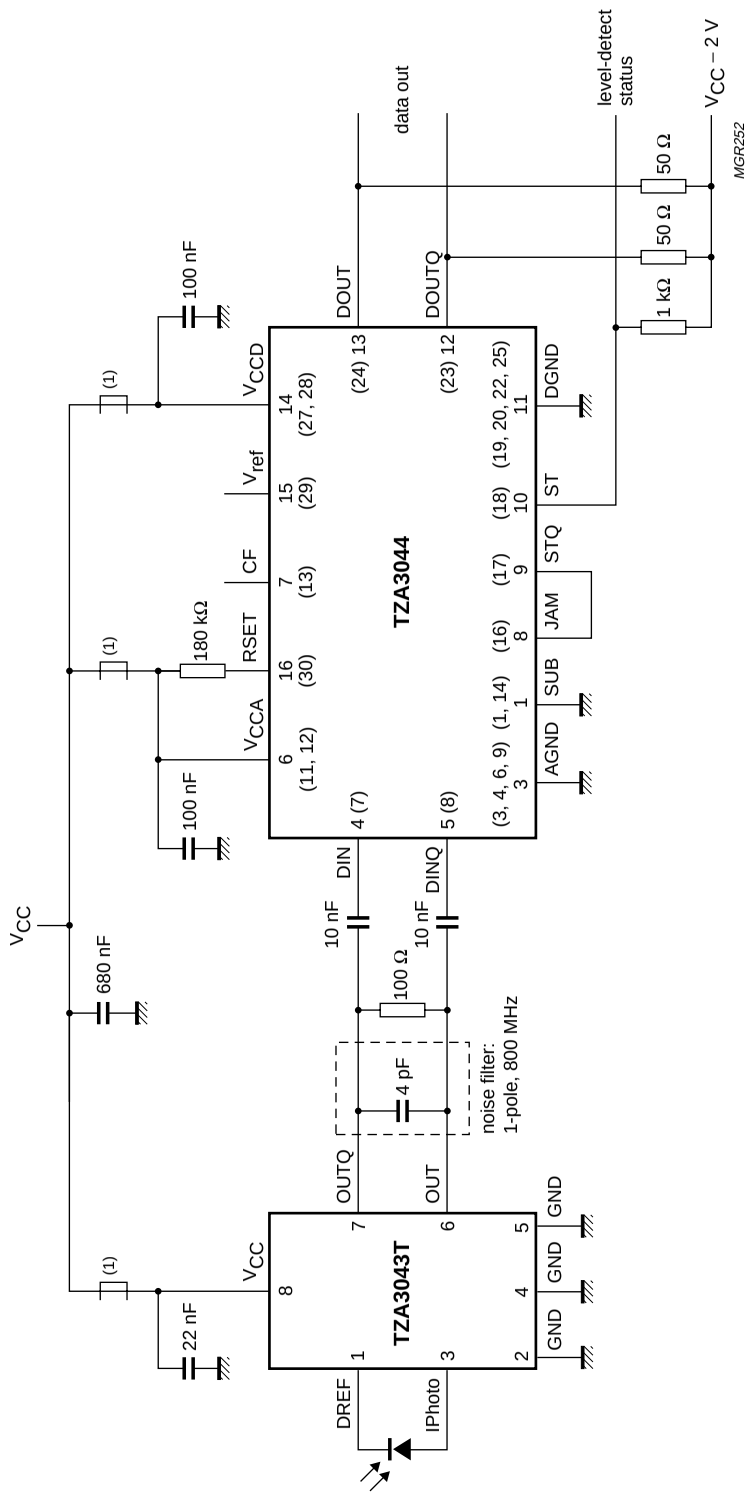
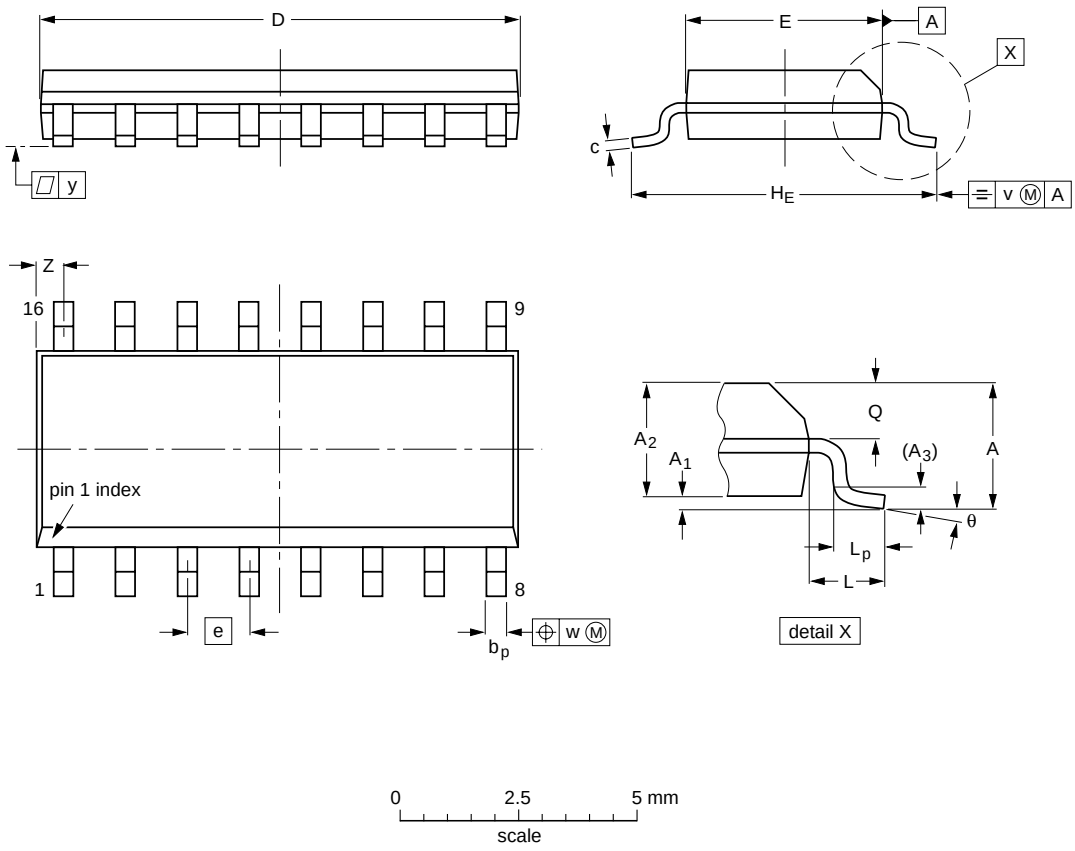


Fig.11 STM1 receiver using the TZA3043T and TZA3044.

(1) ferrite bead e.g. Murata BLM31A601S.
The numbers in brackets refer to the pad numbers of the naked die version.

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 425102/200/01/pp20 Date of release: 1998 Jul 07 Document order number: 9397 750 03816

Let's make things better.

Philips Semiconductors

PHILIPS