DATA SHEET

UMA1016xT
Frequency synthesizer for radio communication equipment

Product specification
Supersedes data of June 1992
File under Integrated Circuits, IC03

1995 Jul 12

Philips
Semiconductors

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Frequency synthesizer for radio communication equipment

UMA1016xT

FEATURES

- RF input frequencies to 1 GHz
- Fully programmable RF divider
- 3-wire serial bus interface
- On-chip 3 to 16 MHz crystal oscillator
- Mask programmable ÷2 to ÷31 reference divider ratio
- Up to 1 MHz channel spacing
- Crystal frequency buffered output
- Dual register architecture for fast Tx/Rx switching in TDD single synthesizer systems
- Phase detector compensated for supply and temperature variations
- Power-down mode.

GENERAL DESCRIPTION

The UMA1016xT is a low power synthesizer for radio communications. Manufactured in bipolar technology, it is designed for a 70 to 1000 kHz channel spacing in the 500 to 1000 MHz band. The channel is programmed via a 3-wire serial bus. The internal dual register architecture allows a single synthesizer to be used in TDD systems. Fast switching between transmit and receive frequencies is achieved without the need for bus overhead. It also incorporates a sensitive, low power RF divider and a dead-zone-eliminated 3-state phase comparator.
A power-down mode enables the circuit to be idled.

APPLICATIONS

- 900 MHz cordless telephones
- Portable battery-powered radio equipment.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		4.5	–	5.5	V
V_{DD}	supply voltage		4.5	–	5.5	V
$I_{CC} + I_{DD}$	supply current		–	12	–	mA
$I_{DD(pd)}$	digital supply current in power-down		–	0.8	–	mA
f_{ref}	phase comparator frequency		70	250	1000	kHz
RF_I	RF input frequency	T_{amb} = –10 to +70°C	500	–	800	MHz
		T_{amb} = 0 to +70°C	500	–	1000	MHz
T_{amb}	operating ambient temperature		–10	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	PIN POSITION	VERSION
UMA1016AT(1)	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UMA1016BT(2)	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
UMA1016xT(3)	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

Notes

1. UMA1016AT has a Reference Division Factor of 27.
2. UMA1016AT has a Reference Division Factor of 16.
3. UMA1016xT is a customized version.

BLOCK DIAGRAM

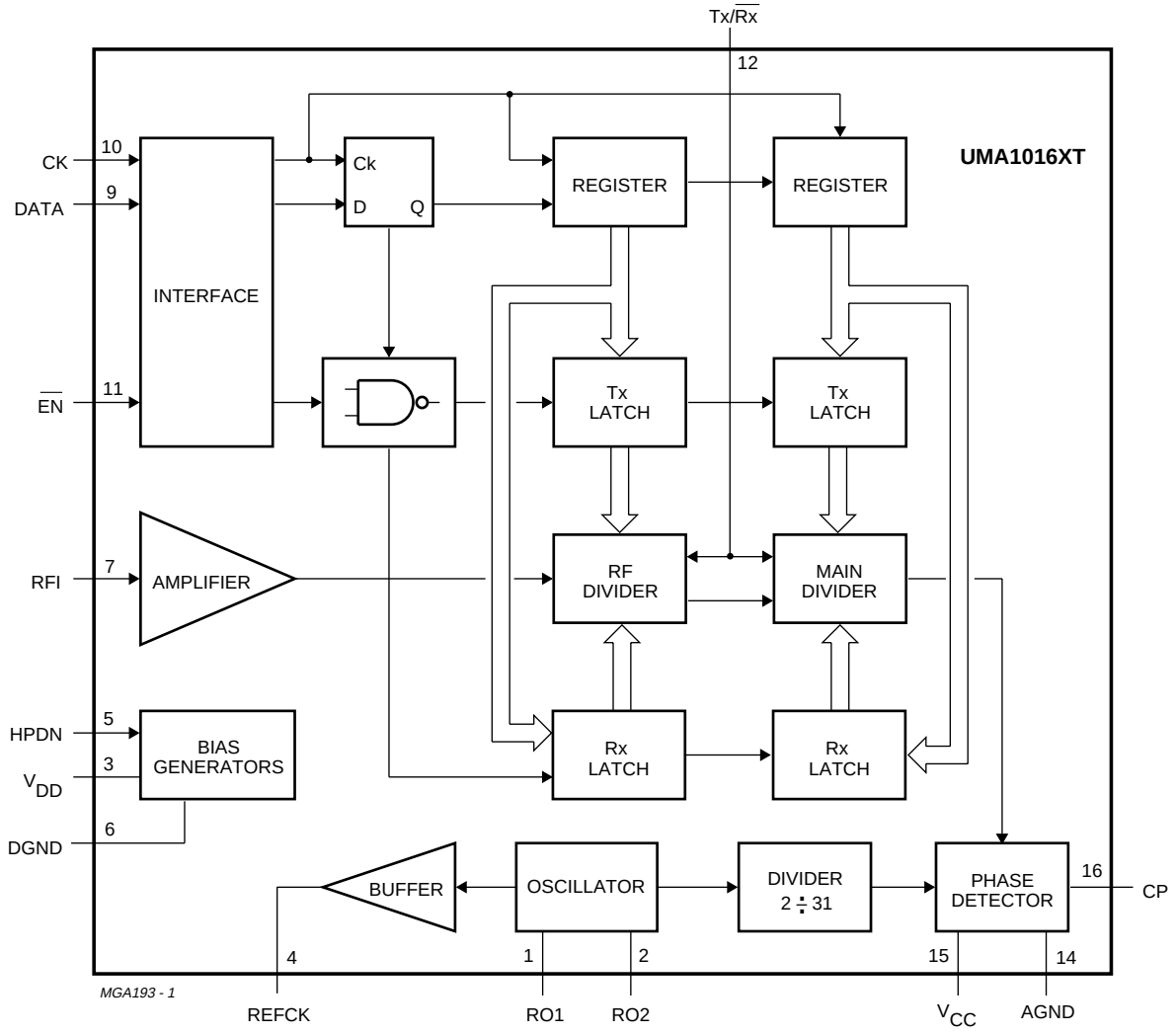


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RO1	1	crystal oscillator input or TCXO input
RO2	2	oscillator output to crystal circuit
V_{DD}	3	5 V supply to digital section
REFCK	4	reference crystal frequency buffered output
HPDN	5	Hardware Power-Down Not; IC operates when pin is HIGH
DGND	6	digital ground
RFI	7	1 GHz RF signal input
i.c.	8	internally connected
DATA	9	programming bus data input
CK	10	programming bus clock input
$\overline{EN}$	11	programming bus enable input (active LOW)
TX/$\overline{RX}$	12	transmit (HIGH)/receive (LOW) mode select input
i.c.	13	internally connected
AGND	14	analog ground
V_{CC}	15	5 V supply to charge pump circuit
CP	16	charge pump output

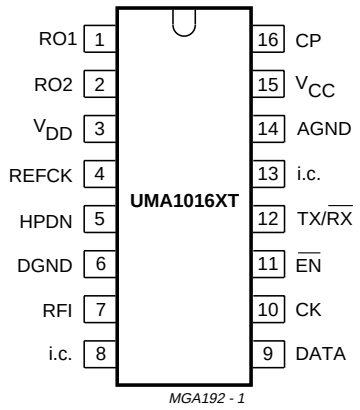


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

General

The UMA1016xT is a low power synthesizer for radio communications in the range 500 to 1000 MHz. It includes an oscillator circuit, reference divider, RF divider, 3-state phase and frequency comparator, charge pump and main control circuit for the transfer of serial data into two internal registers.

V_{DD} supplies power to the digital circuits while V_{CC} powers the charge pump. V_{DD} and V_{CC} are nominally 5 V but will operate in the range 4.5 V to 5.5 V.

Reduced noise coupling is facilitated by separate digital and analog ground pins which must always be externally connected to the same DC potential to prevent the flow of large currents across the die.

The synthesizer is placed in idle mode during power-down but the oscillator and buffer remain operative and may be used as a clock for system timing.

Main divider

The main divider is a fully programmable pulse-swallow type. Following a sensitive (50 mV, –13 dBm) input amplifier, the RF signal is applied to a 13-bit divider (MD13 to MD1). The division ratio is provided via the serial bus to two 13-bit latches, corresponding to transmit and receive frequencies. The serial programming register is written to under processor control, independently of divider operation. This removes difficulty if using a low data bus transmission speed. The new ratio is transferred to the appropriate latch when the programming enable signal ($\overline{EN}$) returns HIGH.

The last register bit (PB0) is used to determine whether the new value is loaded into the transmit (PB0 = 1) or receive (PB0 = 0) frequency latch. To avoid spurious phase changes, the divider incorporates the new ratio only at the end of the on-going reference period. The minimum division ratio is 512. One reference cycle is required to update a new ratio. Internal power-on occurs rapidly.

Oscillator

External capacitive feedback is applied to the common collector Colpitts oscillator which has high voltage supply rejection and negligible temperature drift. It is designed to function as an input buffer without the need for external components when a TCXO or other clock is used.
A separate output buffer, which remains active during power-down (HPDN taken LOW), provides a TTL compatible signal to drive external logic circuits (REFCK).

Reference divider

The reference divider has a fixed divider ratio set by metal masking between 2 and 31. For example, a 4 MHz crystal connected to the oscillator and a ÷16 ratio allows a channel spacing of 250 kHz. Other frequencies and ratios are possible.

Phase comparator

The phase comparator combines a phase and frequency detector and charge pump (see Fig.3). The charge pump current is internally fixed and determined for fast switching. It is compensated against power supply and temperature variation.

The detector is assembled from dual D-type flip-flops which, together with feedback, remove the ‘dead’ zone. Upon the detection of a phase error, either UP or DO go HIGH. This gates the appropriate current generator to source or sink 1.75 mA at the output pin. When no phase error is detected, CP becomes 3-state. The tuning voltage of the VCO is established from the sum of the current pulses into the loop filter.

A simple passive loop filter may be used to offer high performance without requiring an operational-amp.
The phase comparator function is summarized in Table 2.

Main control interface

The programming control interface permits access to two internal latches, denoted Tx and Rx. The serial input bits on DATA, entered MSB first, are converted to a parallel word and stored in the appropriate latch under the control of the last entered register bit (PB0). When this is set HIGH, data serially fed to the register is loaded into the transmit (Tx) latch; when PB0 is LOW, the data is transferred to the receive latch (Rx).

The data sent to the synthesizer is loaded in bursts framed by the signal $\overline{EN}$. Programming clock edges, together with their appropriate data bits, are ignored until $\overline{EN}$ becomes active (LOW). The internal latches are updated with the latest programming data when $\overline{EN}$ returns inactive (HIGH). Only the last 15 bits serially clocked into the device are retained within the programming register. One extra shift register bit (PB7) can be internally added via metal masking to allow direct software compatibility with a 7-bit swallow counter and a 64/65 dual-modulus prescaler. No check is made on the number of clock pulses received during the time that programming is enabled. $\overline{EN}$ going HIGH while CLOCK is still LOW generates an active clock edge causing a shift of the data bits.

Data programmed into the register is lost during power-down (HPDN taken LOW). The maximum serial bus clock speed is specified as 5 MHz. Minimum speed is limited by the clock edge rise and fall times to ensure that no data transparency condition can exist.

Independent of any serial programming activity, the RF divider chain uses the data previously stored within the selected latch to determine the synthesized channel frequency. The Tx/$\overline{Rx}$ signal controls which latch is read to preload the counter bits at each division cycle. When new data is updated into the device, it is used during the cycle following latch selection by the Tx/$\overline{Rx}$ control line.

If the Tx/$\overline{Rx}$ line is tied LOW, only data loaded into the Rx latch is used. In this event the serial data stream clocked into the synthesizer must terminate with an ‘0’. The logic diagram for the first bits of the programming interface is shown in Fig.3. The other bits are processed in a similar manner by a further 9 stages of the shift register-latches-multiplexer.

The signals supplied to the circuit are described by the timing diagram. The table of values has been specified for maximum bus speed. Under slow clocking conditions, rise and fall times must not be excessively slow.

Table 1 Main divider division ratio

MAIN COUNTER							
MD1	MD2	../..	MD7	MD8	../..	MD12	MD13
LSB							MSB

Table 2 Operation of phase comparator

SYMBOL	$F_{ref} < F_{var}$	$F_{ref} > F_{var}$	$F_{ref} = F_{var}$
UP	0	1	0
DO	1	0	0
I_{pcd}	−1.75 mA	+1.75 mA	<±5 nA

Table 3 Register and latch bit allocations

FIRST	REGISTER AND LATCH BIT ALLOCATIONS													LAST IN
pb14	pb13	pb12	pb11	pb10	pb9	pb8	pb7(1)	pb6	pb5	pb4	pb3	pb2	pb1	pb0
md13	md12	md11	md10	md9	md8	md7	X	md6	md5	md4	md3	md2	md1	address

Note

1. pb7; see Section “Main control interface”.

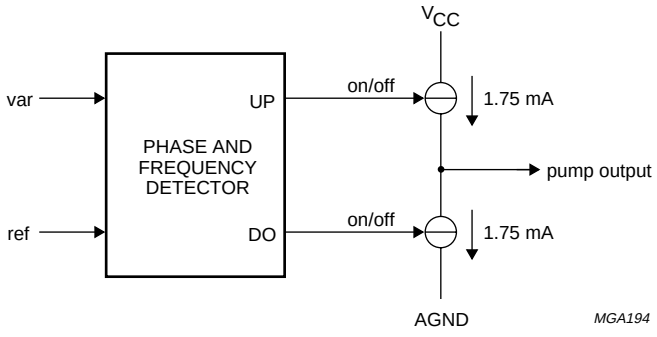


Fig.3 Phase comparator block diagram.

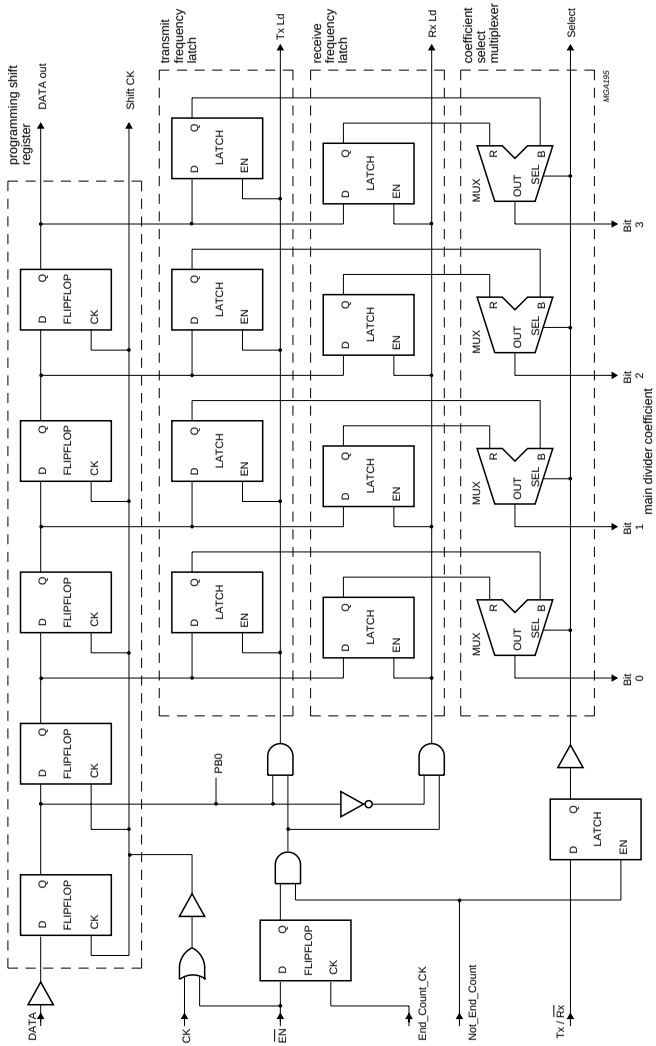


Fig.4 Simplified interface logic diagram.

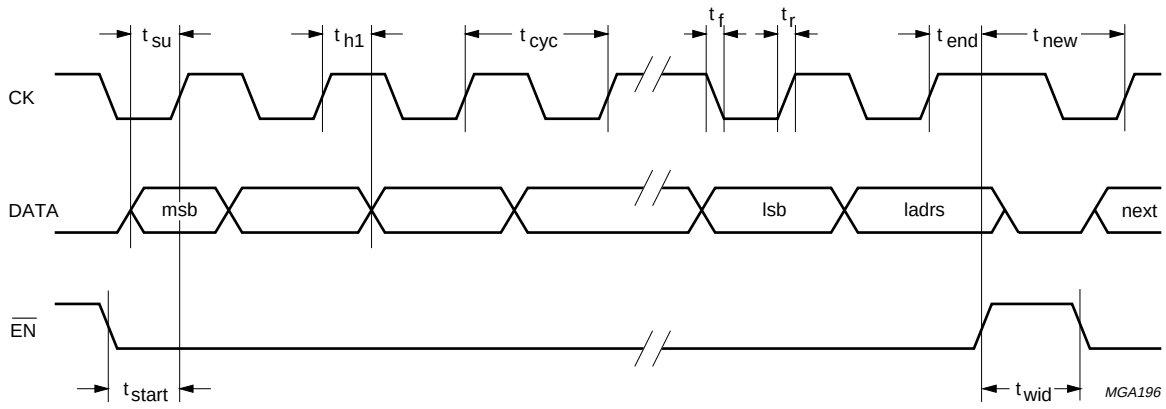


Fig.5 Logic interface signals.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage range		–0.2	–	7	V
V_{CC}	analog supply voltage range		–0.2	–	7	V
V_i	input voltage range	to ground	0	–	V_{DD}	V
T_{stg}	storage temperature range		–55	–	125	°C
T_{amb}	operating ambient temperature		–10	–	70	°C

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

TIMING CHARACTERISTICS

V_{DD} and V_{CC} = 5 V; T_{amb} = –10 to +70 °C; unless otherwise specified; typical values measured at V_{CC} and V_{DD} = 5 V; T_{amb} = 25 °C; note 1.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock (pin 10)					
f_{ck}	clock frequency	0.01	4	5	MHz
t_r	rise time	–	5	50	ns
t_f	fall time		5	50	ns
T_{cy}	clock period	200	–	–	ns
Enable programming (pin 11)					
t_{start}	delay to rising clock edge	30	–	–	ns
t_{end}	delay from last clock edge	0	–	–	ns
t_{width}	minimum inactive pulse width	200	–	–	ns
t_{new}	delay from $\overline{EN}$ inactive to new data	300	–	–	ns
Register serial input data (pin 9)					
t_{su}	input data to CK set-up time	10	–	–	ns
t_{h1}	input data to CK hold time	10	–	–	ns

Note

1. Minimum and maximum values are for maximum clock speed.

CHARACTERISTICS

V_{DD} and V_{CC} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply						
V_{DD}	digital voltage supply	$V_{CC} = V_{DD}$	4.5	5	5.5	V
V_{CC}	analog voltage supply		4.5	5	5.5	V
I_{DD}	digital supply current	V_{DD} = 5.5 V; REFCK off	–	10.1	10.8	mA
I_{CC}	analog supply current	V_{CC} = 5.5 V; pump off	–	1.9	2.1	mA
$I_{DD(pd)}$	digital supply current in power-down mode		–	0.8	1.5	mA
RF divider input (RFI)						
f_{vco}	RF frequency range	T_{amb} = –10 to +70°C	500	–	800	MHz
		T_{amb} = 0 to +70°C	500	–	1000	MHz
$V_{rf(rms)}$	input signal voltage level (RMS value)		50	–	200	mV
R_{iRF}	input resistance	RF = 1 GHz	–	350	–	Ω
C_{iRF}	input capacitance	indicative; not tested	–	1.5	–	pF
N	main divider division ratio		512	–	8191	
Oscillator and reference divider (RO1, RO2)						
f_{ref}	oscillator frequency range	$R_{ref(ck)}$ used	3	–	16	MHz
$V_{osc(rms)}$	sinusoidal input level at pin 1 (RMS value)		0.1	–	0.5	V
C_{o1}	parasitic capacitance at pin 1	indicative; not tested	–	5	–	pF
Z_{o2}	output impedance at pin 2	indicative; not tested	–	2	–	kΩ
C_{o2}	output capacitance	indicative; not tested	–	5	–	pF
Phase comparator and charge pump output (CP)						
f_{cp}	phase detector frequency range		70	250	1000	kHz
$I_{cp(source)}$	charge pump source current	V_{CC} = 4.5 to 5.5 V	–2.2	–1.75	–1.3	mA
$I_{cp(sink)}$	charge pump sink current	V_{CC} = 4.5 to 5.5 V	1.3	1.75	2.2	mA
$I_{cp(leak)}$	charge pump off leakage current		–10	–	+10	nA
V_{cp}	charge pump voltage compliance range	I_{cp} within specified range	0.5	–	V_{CC} – 0.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels (HPDN, EN, DATA, CK, Tx/$\overline{Rx}$)						
V_{IH}	HIGH level input voltage	all inputs	3	–	V_{DD} + 0.3	V
$V_{IL(PD)}$	LOW level input voltage	HPDN	–0.3	–	0.6	V
V_{IL}	LOW level input voltage	except HPDN	–0.3	–	1	V
I_{bias}	input bias current	logic 1	–	–	5	μA
		logic 0	–5	–	–	μA
C_i	input capacitance	indicative; not tested	–	3	–	pF
Oscillator buffered logic output signal (REFCK)						
V_{oh}	HIGH level driven output voltage	V_{DD} = 5 V	3.5	4.0	V_{DD} – 0.5	V
V_{ol}	LOW level driven output voltage		0	–	0.4	V
$I_{o(sink)}$	output sink current	V_{CL} = 0.5 V	–0.4	–	–	mA
t_r	reference clock output rise time	C_l = 25 pF	–	50	–	ns
t_f	reference clock output fall time	C_L = 25 pF	–	50	–	ns

APPLICATION INFORMATION

In a typical single-synthesizer application, the circuit is connected as shown in Fig.6. Both analog and digital supplies are decoupled to ground with HF and LF filter capacitors. Correct oscillator operation requires capacitors both to ground and to provide feedback across the amplifier. Five signals are shown fed from a microcontroller to provide serial programming, control TDD frequency selection and initiate the power-down mode. Other system logic may also be clocked by a crystal frequency output from the synthesizer.

A passive 2nd-order loop filter giving a 3rd-order system response is shown in Fig.6. Indicated values are intended for rapid frequency switching (500 μs), 200 kHz channel spacing (reference ÷27) and breakthrough levels below −60 dB. The VCO output shows a power splitter supplying both the synthesizer RF input and drive buffer for other system components (RF amplifier in transmit mode, input mixer in receive mode). The minimizing of loop filter node leakage currents requires careful board layout.

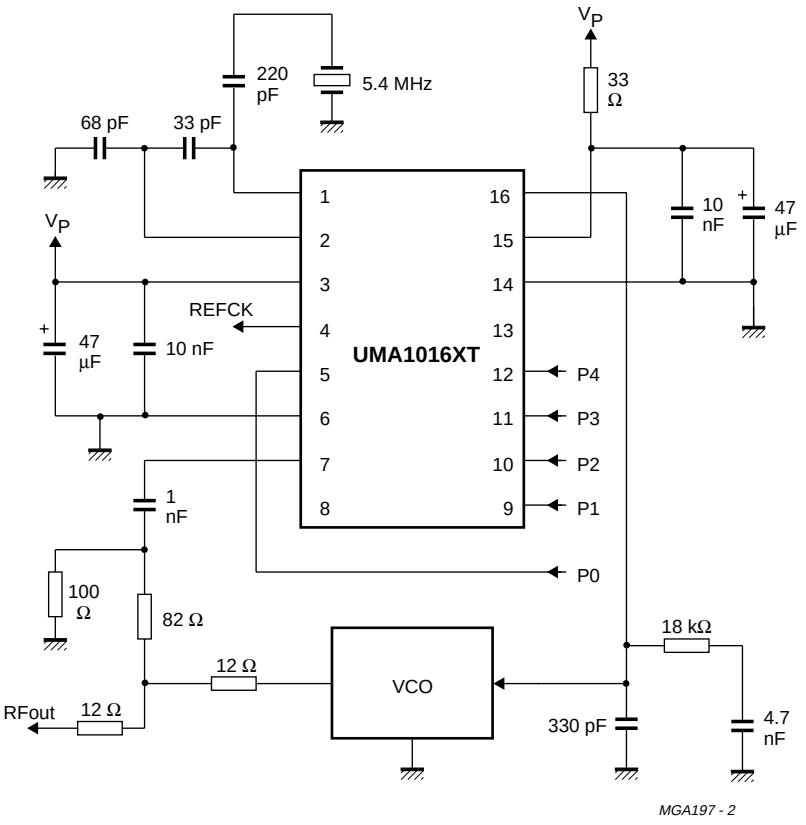
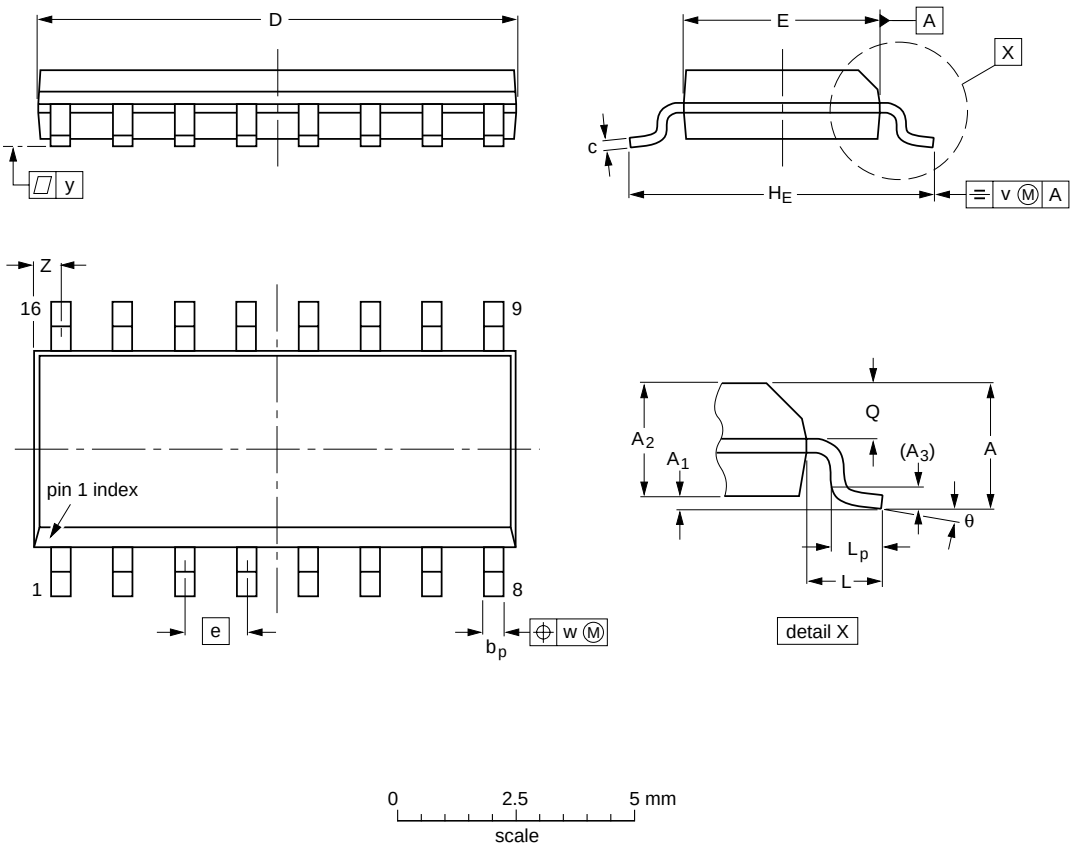


Fig.6 Application diagram.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~95-01-23~~ 97-05-22

SOLDERING SO or SSOP

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these cases reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO and SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

SO

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

SSOP

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

METHOD (SO OR SSOP)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds at 270 to 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	

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